



SBOS141C – JANUARY 1984 – REVISED SEPTEMBER 2009

PRECISION VOLTAGE-TO-CURRENT CONVERTER/TRANSMITTER

FEATURES

- 4mA TO 20mA TRANSMITTER
- SELECTABLE INPUT/OUTPUT RANGES:
0V to +5V, 0V to +10V Inputs
0mA to 20mA, 5mA to 25mA Outputs
Other Ranges
- 0.005% MAX NONLINEARITY, 14 BIT
- PRECISION +10V REFERENCE OUTPUT
- SINGLE-SUPPLY OPERATION
- WIDE SUPPLY RANGE: 13.5V to 40V

DESCRIPTION

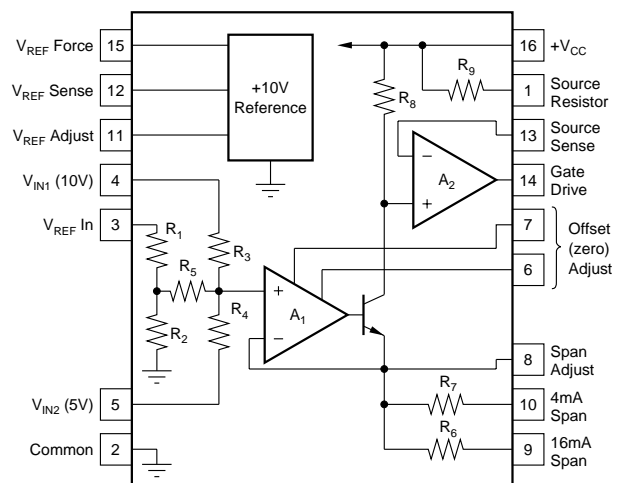
The XTR110 is a precision voltage-to-current converter designed for analog signal transmission. It accepts inputs of 0 to 5V or 0 to 10V and can be connected for outputs of 4mA to 20mA, 0mA to 20mA, 5mA to 25mA, and many other commonly used ranges.

A precision on-chip metal film resistor network provides input scaling and current offsetting. An internal 10V voltage reference can be used to drive external circuitry.

The XTR110 is available in 16-pin plastic DIP, ceramic DIP and SOL-16 surface-mount packages. Commercial and industrial temperature range models are available.

APPLICATIONS

- INDUSTRIAL PROCESS CONTROL
- PRESSURE/TEMPERATURE TRANSMITTERS
- CURRENT-MODE BRIDGE EXCITATION
- GROUNDED TRANSDUCER CIRCUITS
- CURRENT SOURCE REFERENCE FOR DATA ACQUISITION
- PROGRAMMABLE CURRENT SOURCE FOR TEST EQUIPMENT
- POWER PLANT/ENERGY SYSTEM MONITORING



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

All trademarks are the property of their respective owners.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

| | |
|--|---|
| Power Supply, $+V_{CC}$ | 40V |
| Input Voltage, V_{IN1} , V_{IN2} , $V_{REF IN}$ | $+V_{CC}$ |
| See text regarding safe negative input voltage range. | |
| Storage Temperature Range: A, B | -55°C to $+125^{\circ}\text{C}$ |
| K, U | -40°C to $+85^{\circ}\text{C}$ |
| Output Short-Circuit Duration, Gate Drive and V_{REF} Force | Continuous to common and $+V_{CC}$ |
| Output Current Using Internal 50Ω Resistor | 40mA |

NOTE: (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability.



ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

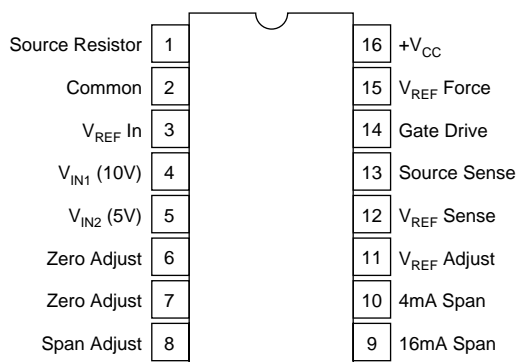
PACKAGE/ORDERING INFORMATION⁽¹⁾

| PRODUCT | PACKAGE-LEAD | PACKAGE DESIGNATOR | TEMPERATURE RANGE |
|----------|----------------------|--------------------|--|
| XTR110AG | DIP-16 Ceramic | JD | -40°C to $+85^{\circ}\text{C}$ |
| XTR110BG | DIP-16 Ceramic | JD | -40°C to $+85^{\circ}\text{C}$ |
| XTR110KP | DIP-16 Plastic | N | 0°C to $+70^{\circ}\text{C}$ |
| XTR110KU | SOL-16 Surface-Mount | DW | 0°C to $+70^{\circ}\text{C}$ |

NOTE: (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

PIN CONFIGURATION

TOP VIEW



ELECTRICAL CHARACTERISTICS

At $T_A = +25^\circ\text{C}$ and $V_{CC} = +24\text{V}$ and $R_L = 250\Omega^{**}$, unless otherwise specified.

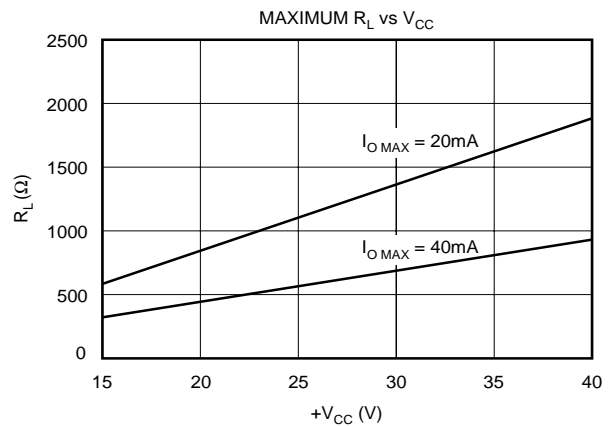
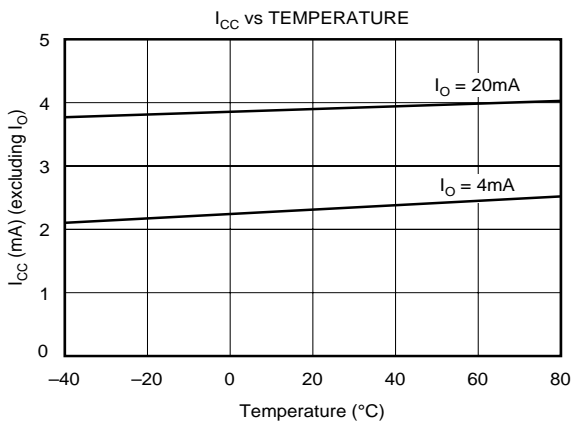
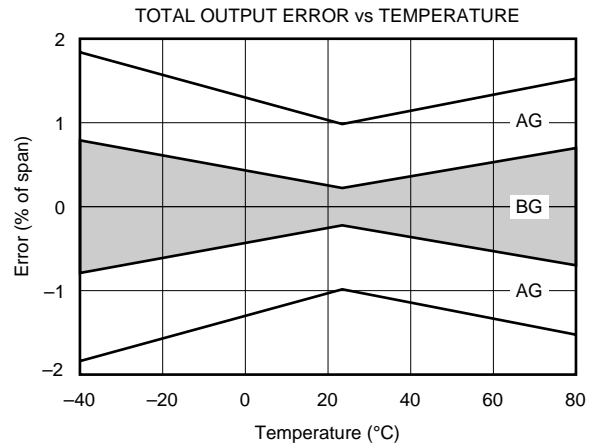
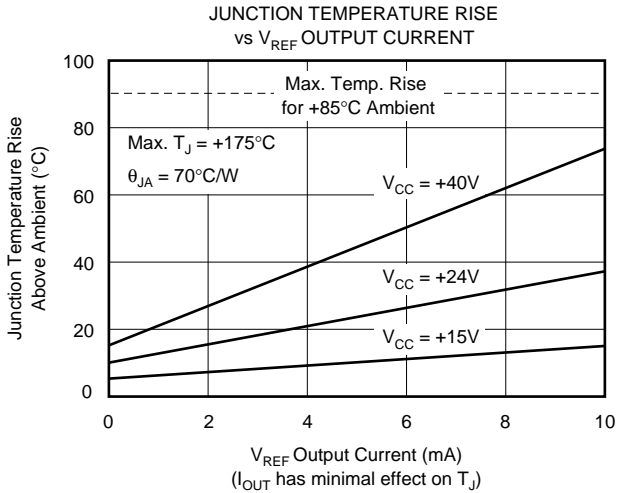
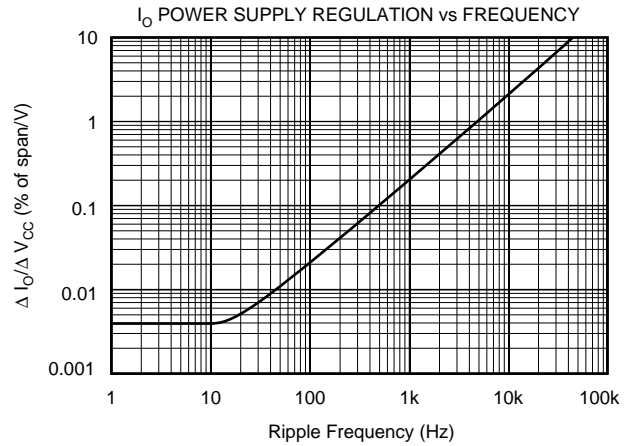
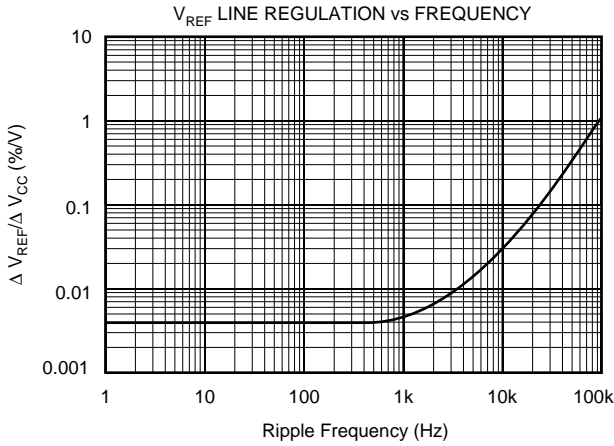
| PARAMETER | CONDITIONS | XTR110AG, KP, KU | | | XTR110BG | | | UNITS |
|---|---------------------------------------|------------------|--|--------|----------|--------|--------|-----------------------------|
| | | MIN | TYP | MAX | MIN | TYP | MAX | |
| TRANSMITTER | | | | | | | | |
| Transfer Function | | | $I_O = 10 [(V_{REF} \ln/16) + (V_{IN1}/4) + (V_{IN2}/2)] / R_{SPAN}$ | | | | | |
| Input Range: $V_{IN1}^{(5)}$ V_{IN2} | Specified Performance | 0 | | +10 | * | | * | V |
| | Specified Performance | 0 | | +5 | * | | * | V |
| Current, I_O | Specified Performance ⁽¹⁾ | 4 | | 20 | * | | * | mA |
| | Derated Performance ⁽¹⁾ | 0 | | 40 | * | | * | mA |
| Nonlinearity | 16mA/20mA Span ⁽²⁾ | | 0.01 | 0.025 | | 0.002 | 0.005 | % of Span |
| Offset Current, I_{OS} | $I_O = 4\text{mA}^{(1)}$ | | | | | | | |
| Initial | (1) | | 0.2 | 0.4 | | 0.02 | 0.1 | % of Span |
| vs Temperature | (1) | | 0.0003 | 0.005 | | * | 0.003 | % of Span/ $^\circ\text{C}$ |
| vs Supply, V_{CC} | (1) | | 0.0005 | 0.005 | | * | * | % of Span/V |
| Span Error | $I_O = 20\text{mA}$ | | | | | | | |
| Initial | (1) | | 0.3 | 0.6 | | 0.05 | 0.2 | % of Span |
| vs Temperature | (1) | | 0.0025 | 0.005 | | 0.0009 | 0.003 | % of Span/ $^\circ\text{C}$ |
| vs Supply, V_{CC} | (1) | | 0.003 | 0.005 | | * | * | % of Span/V |
| Output Resistance | From Drain of FET ($Q_{EXT}^{(3)}$) | | 10×10^9 | | | * | * | Ω |
| Input Resistance | V_{IN1} | | 27 | | | * | * | k Ω |
| | V_{IN2} | | 22 | | | * | * | k Ω |
| | $V_{REF} \ln$ | | 19 | | | * | * | k Ω |
| Dynamic Response | | | | | | | | |
| Settling Time | To 0.1% of Span | | 15 | | | * | * | μs |
| | To 0.01% of Span | | 20 | | | * | * | μs |
| Slew Rate | | | 1.3 | | | * | * | mA/ μs |
| VOLTAGE REFERENCE | | | | | | | | |
| Output Voltage | | +9.95 | +10 | +10.05 | +9.98 | * | +10.02 | V |
| vs Temperature | | | 35 | 50 | | 15 | 30 | ppm/ $^\circ\text{C}$ |
| vs Supply, V_{CC} | Line Regulation | | 0.0002 | 0.005 | | * | * | %/V |
| vs Output Current | Load Regulation | | 0.0005 | 0.01 | | * | * | %/mA |
| vs Time | | | 100 | | | * | * | ppm/1k hrs |
| Trim Range | | -0.100 | | +0.25 | * | | * | V |
| Output Current | Specified Performance | 10 | | | * | | | mA |
| POWER SUPPLY | | | | | | | | |
| Input Voltage, V_{CC} | | +13.5 | | +40 | * | | * | V |
| Quiescent Current | Excluding I_O | | 3 | 4.5 | | * | * | mA |
| TEMPERATURE RANGE | | | | | | | | |
| Specification: AG, BG | | -40 | | +85 | * | | * | $^\circ\text{C}$ |
| KP, KU | | 0 | | +70 | | | | $^\circ\text{C}$ |
| Operating: AG, BG | | -55 | | +125 | * | | * | $^\circ\text{C}$ |
| KP, KU | | -25 | | +85 | | | | $^\circ\text{C}$ |

* Specifications same as AG/KP grades. ** Specifications apply to the range of R_L shown in Typical Performance Curves.

NOTES: (1) Including internal reference. (2) Span is the change in output current resulting from a full-scale change in input voltage. (3) Within compliance range limited by $(+V_{CC} - 2V) + V_{DS}$ required for linear operation of the FET. (4) For V_{REF} adjustment circuit see Figure 3. (5) For extended I_{REF} drive circuit see Figure 4. (5) Unit may be damaged. See *Input Voltage Range* section.

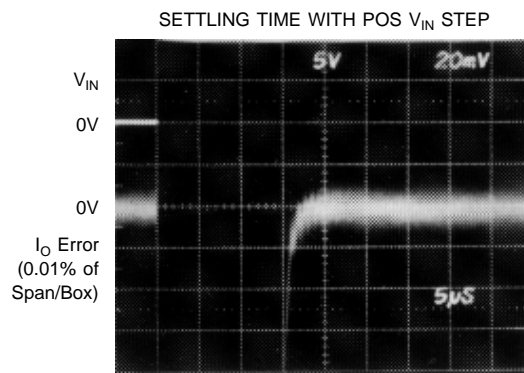
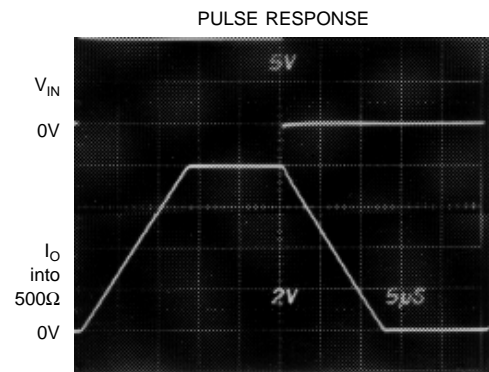
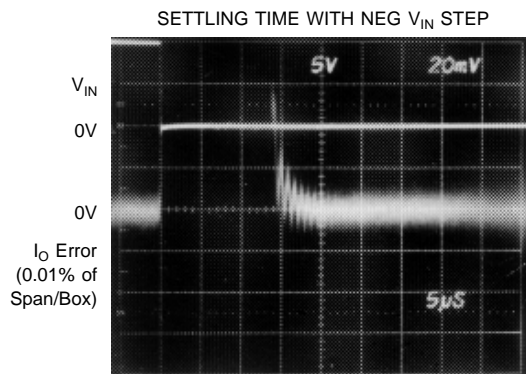
TYPICAL PERFORMANCE CURVES

$T_A = +25^\circ\text{C}$, $V_{CC} = 24\text{VDC}$, $R_L = 250\Omega$, unless otherwise noted.



TYPICAL PERFORMANCE CURVES (Continued)

At $T_A = +25^\circ\text{C}$, $V_{CC} = 24\text{VDC}$, $R_L = 250\Omega$, unless otherwise noted.



APPLICATIONS INFORMATION

Figure 1 shows the basic connections required for 0V to 10V input and 4ma to 20mA output. Other input voltage and output current ranges require changes in connections of pins 3, 4, 5, 9 and 10 as shown in the table of Figure 1.

The complete transfer function of the XTR110 is:

$$I_O = \frac{10 \left[\frac{(V_{REF IN})}{16} + \frac{(V_{IN1})}{4} + \frac{(V_{IN2})}{2} \right]}{R_{SPAN}} \quad (1)$$

R_{SPAN} is the total impedance seen at the emitter of the internal NPN transistor. This impedance varies depending on how pins 8, 9 and 10 are configured. Typical operating region configurations are shown in Figure 1. An external R_{SPAN} can be connected for different output current ranges as described later.

EXTERNAL TRANSISTOR

An external pass transistor, Q_{EXT} , is required as shown in Figure 1. This transistor conducts the output signal current. A P-channel MOSFET transistor is recommended. It must

have a voltage rating equal or greater than the maximum power supply voltage. Various recommended types are shown in Table I.

| MANUFACTURER | PART NO. | BV _{DSS} ⁽¹⁾ | BV _{GS} ⁽¹⁾ | PACKAGE |
|-------------------------|----------|----------------------------------|---------------------------------|---------|
| Ferranti | ZVP1304A | 40V | 20V | TO-92 |
| | ZVP1304B | 40V | 20V | TO-39 |
| | ZVP1306A | 60V | 20V | TO-92 |
| | ZVP1306B | 60V | 20V | TO-39 |
| International Rectifier | IRF9513 | 60V | 20V | TO-220 |
| Motorola | MTP8P08 | 80V | 20V | TO-220 |
| RCA | RFL1P08 | 80V | 20V | TO-39 |
| | RFT2P08 | 80V | 20V | TO-220 |
| Siliconix (preferred) | VP0300B | 30V | 40V | TO-39 |
| | VP0300L | 30V | 40V | TO-92 |
| | VP0300M | 30V | 40V | TO-237 |
| | VP0808B | 80V | 40V | TO-39 |
| | VP0808L | 80V | 40V | TO-92 |
| | VP0808M | 80V | 40V | TO-237 |
| Supertex | VP1304N2 | 40V | 20V | TO-220 |
| | VP1304N3 | 40V | 20V | TO-92 |
| | VP1306N2 | 60V | 20V | TO-220 |
| | VP1306N3 | 60V | 20V | TO-92 |

NOTE: (1) BV_{DSS}—Drain-source breakdown voltage. BV_{GS}—Gate-source breakdown voltage.

TABLE I. Available P-Channel MOSFETs.

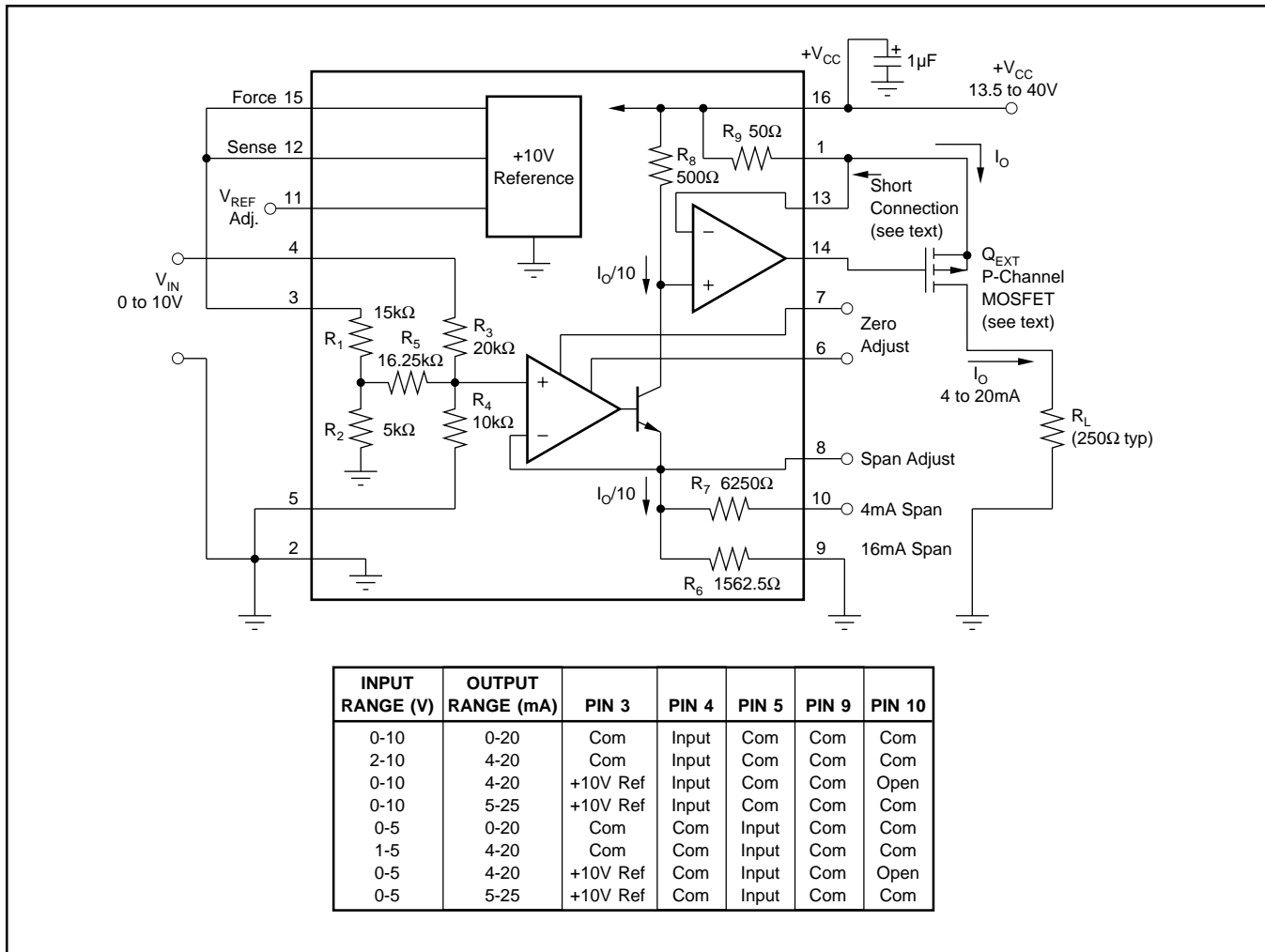


FIGURE 1. Basic Circuit Connection.

If the supply voltage, $+V_{CC}$, exceeds the gate-to-source breakdown voltage of Q_{EXT} , and the output connection (drain of Q_{EXT}) is broken, Q_{EXT} could fail. If the gate-to-source breakdown voltage is lower than $+V_{CC}$, Q_{EXT} can be protected with a 12V zener diode connected from gate to source.

Two PNP discrete transistors (Darlington-connected) can be used for Q_{EXT} —see Figure 2. Note that an additional capacitor is required for stability. Integrated Darlington transistors are not recommended because their internal base-emitter resistors cause excessive error.

TRANSISTOR DISSIPATION

Maximum power dissipation of Q_{EXT} depends on the power supply voltage and full-scale output current. Assuming that the load resistance is low, the power dissipated by Q_{EXT} is:

$$P_{MAX} = (+V_{CC}) I_{FS} \quad (2)$$

The transistor type and heat sinking must be chosen according to the maximum power dissipation to prevent overheating. See Table II for general recommendations.

| PACKAGE TYPE | ALLOWABLE POWER DISSIPATION |
|--------------|---|
| TO-92 | Lowest: Use minimum supply and at +25°C. |
| TO-237 | Acceptable: Trade-off supply and temperature. |
| TO-39 | Good: Adequate for majority of designs. |
| TO-220 | Excellent: For prolonged maximum stress. |
| TO-3 | Use if hermetic package is required. |

TABLE II. External Transistor Package Type and Dissipation.

INPUT VOLTAGE RANGE

The internal op amp A_1 can be damaged if its non-inverting input (an internal node) is pulled more than 0.5V below common (0V). This could occur if input pins 3, 4 or 5 were driven with an op amp whose output could swing negative under abnormal conditions. The voltage at the input of A_1 is:

$$V_{A1} = \frac{(V_{REF IN})}{16} + \frac{(V_{IN1})}{4} + \frac{(V_{IN2})}{2} \quad (3)$$

This voltage should not be allowed to go more negative than $-0.5V$. If necessary, a clamp diode can be connected from the negative-going input to common to clamp the input voltage.

COMMON (Ground)

Careful attention should be directed toward proper connection of the common (grounds). All commons should be joined at one point as close to pin 2 of the XTR110 as possible. The exception is the I_{OUT} return. It can be returned to any point where it will not modulate the common at pin 2.

VOLTAGE REFERENCE

The reference voltage is accurately regulated at pin 12 ($V_{REF SENSE}$). To preserve accuracy, any load including pin

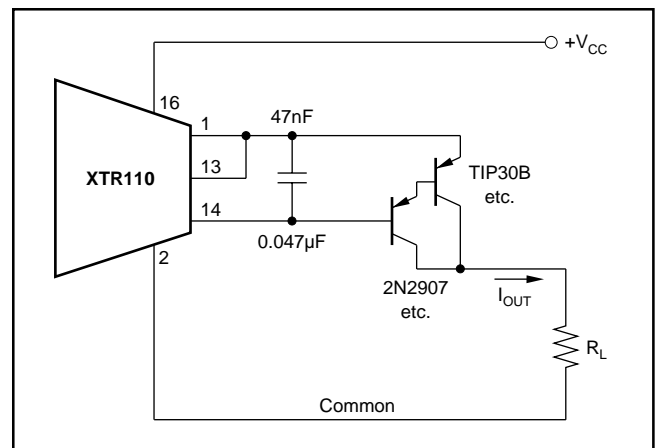


FIGURE 2. Q_{EXT} Using PNP Transistors.

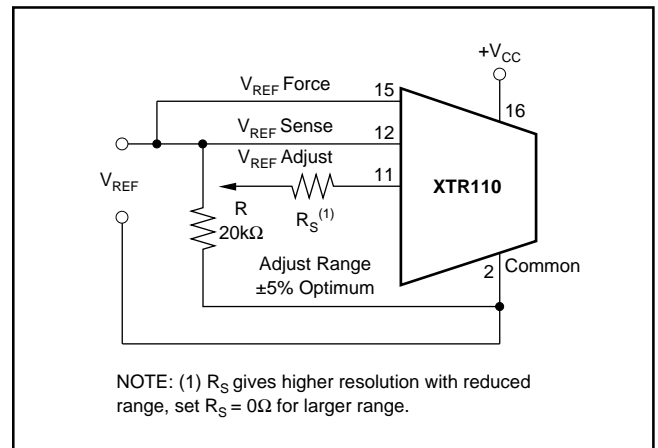


FIGURE 3. Optional Adjustment of Reference Voltage.

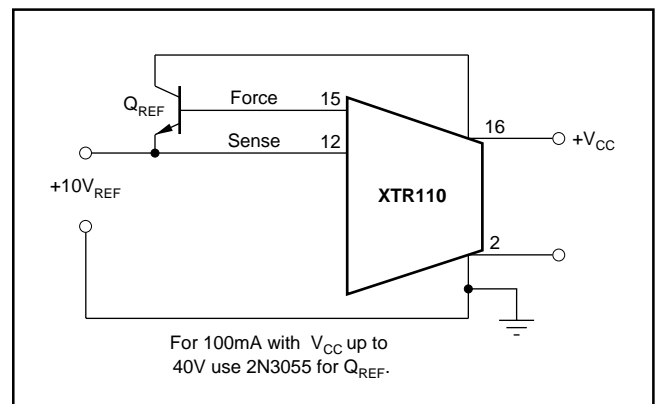


FIGURE 4. Increasing Reference Current Drive.

3 should be connected to this point. The circuit in Figure 3 shows adjustment of the voltage reference.

The current drive capability of the XTR110's internal reference is 10mA. This can be extended if desired by adding an external NPN transistor shown in Figure 4.

OFFSET (ZERO) ADJUSTMENT

The offset current can be adjusted by using the potentiometer, R_1 , shown in Figure 5. Set the input voltage to zero and then adjust R_1 to give 4mA at the output. For spans starting

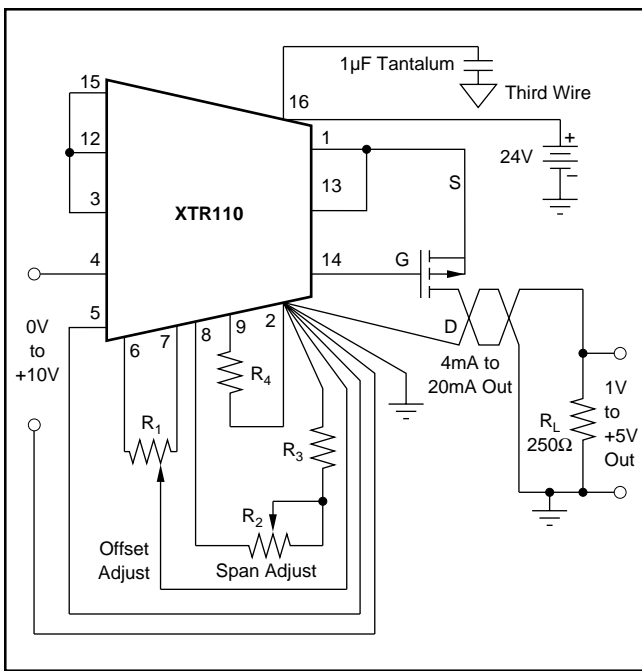


FIGURE 5. Offset and Span Adjustment Circuit for 0V to +10V Input, 4mA to 20mA Output.

at 0mA, the following special procedure is recommended: set the input to a small nonzero value and then adjust R_1 to the proper output current. When the input is zero the output will be zero. Figures 6 and 7 show graphically how offset is adjusted.

SPAN ADJUSTMENT

The span is adjusted at the full-scale output current using the potentiometer, R_2 , shown in Figure 5. This adjustment is interactive with the offset adjustment, and a few iterations may be necessary. For the circuit shown, set the input voltage to +10V full scale and adjust R_2 to give 20mA full-scale output. Figures 6 and 7 show graphically how span is adjusted.

The values of R_2 , R_3 , and R_4 for adjusting the span are determined as follows: choose R_4 in series to slightly decrease the span; then choose R_2 and R_3 to increase the span to be adjustable about the center value.

LOW TEMPERATURE COEFFICIENT OPERATION

Although the precision resistors in the XTR110 track within 1ppm/°C, the output current depends upon the absolute temperature coefficient (TC) of any one of the resistors, R_6 , R_7 , R_8 , and R_9 . Since the absolute TC of the output current can have 20ppm/°C, maximum, the TC of the output current can have 20ppm/°C drift. For low TC operation, zero TC resistors can be substituted for either the span resistors (R_6 or R_7) or for the source resistor (R_9) but not both.

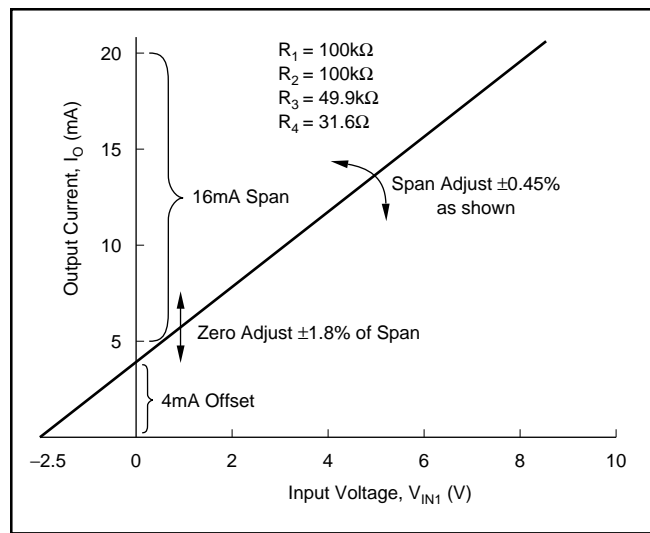


FIGURE 6. Zero and Span of 0V to +10V Input, 4mA to 20mA Output Configuration (see Figure 5).

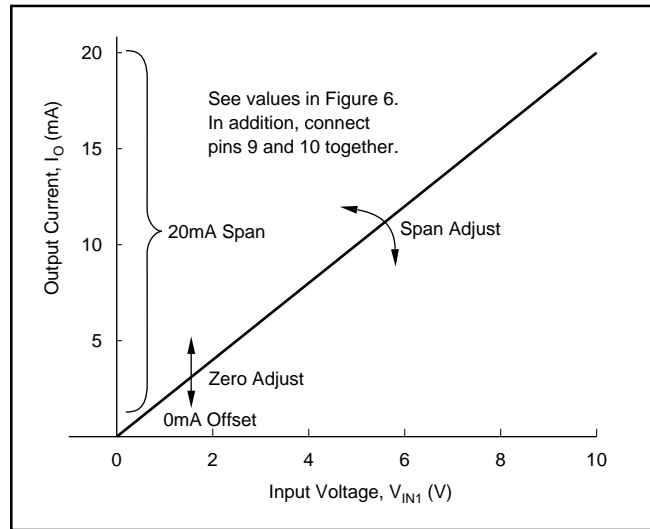


FIGURE 7. Zero and Span of 0V to +10V_{IN}, 0mA to 20mA Output Configuration (see Figure 5).

EXTENDED SPAN

For spans beyond 40mA, the internal 50Ω resistor (R_9) may be replaced by an external resistor connected between pins 13 and 16.

Its value can be calculated as follows:

$$R_{EXT} = R_9 (\text{Span}_{OLD} / \text{Span}_{NEW})$$

Since the internal thin-film resistors have a 20% absolute value tolerance, measure R_9 before determining the final value of R_{EXT} . Self-heating of R_{EXT} can cause nonlinearity. Therefore, choose one with a low TC and adequate power rating. See Figure 10 for application.

TYPICAL APPLICATIONS

The XTR110 is ideal for a variety of applications requiring high noise immunity current-mode signal transmission. The precision +10V reference can be used to excite bridges and transducers. Selectable ranges make it very useful as a precision programmable current source. The compact design

and low price of the XTR110 allow versatility with a minimum of external components and design engineering expense.

Figures 8 through 10 show typical applications of the XTR110.

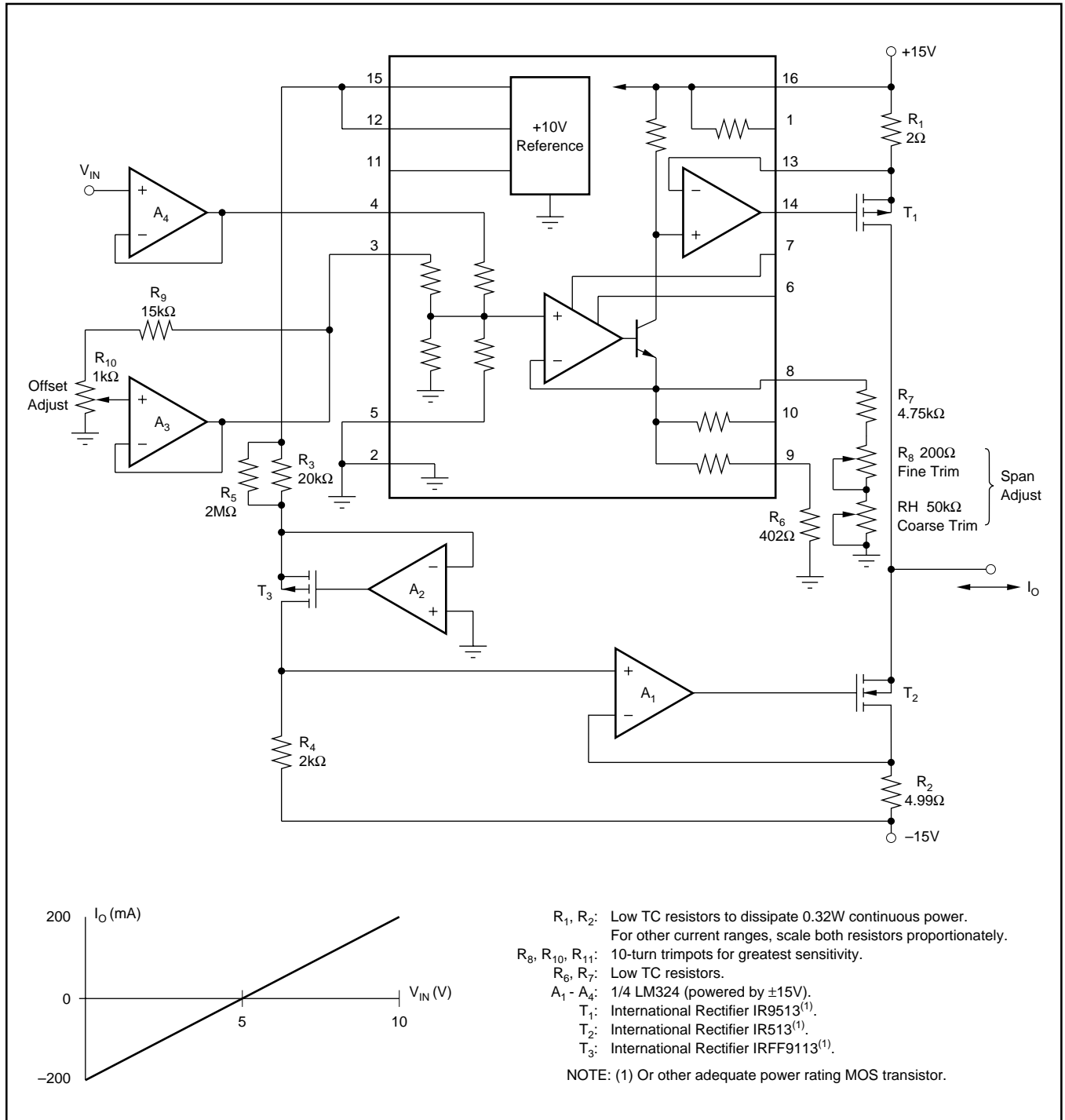


FIGURE 8. $\pm 200mA$ Current Pump.

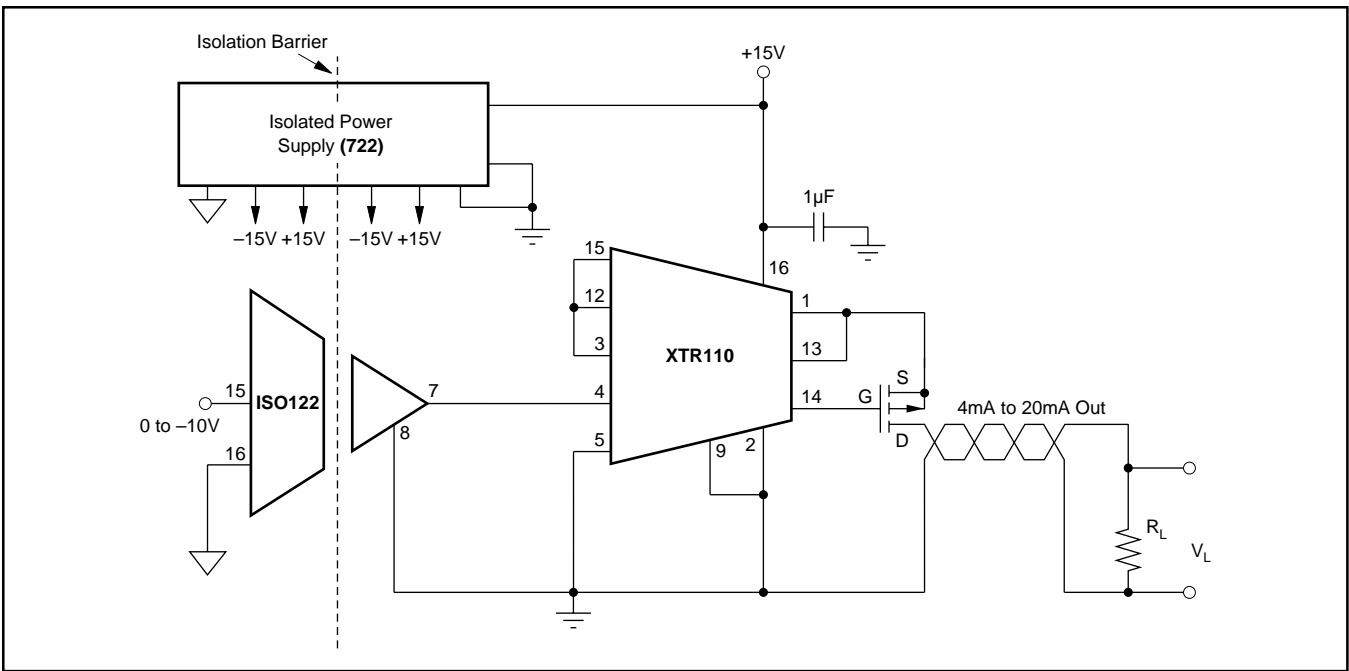


FIGURE 9. Isolated 4mA to 20mA Channel.

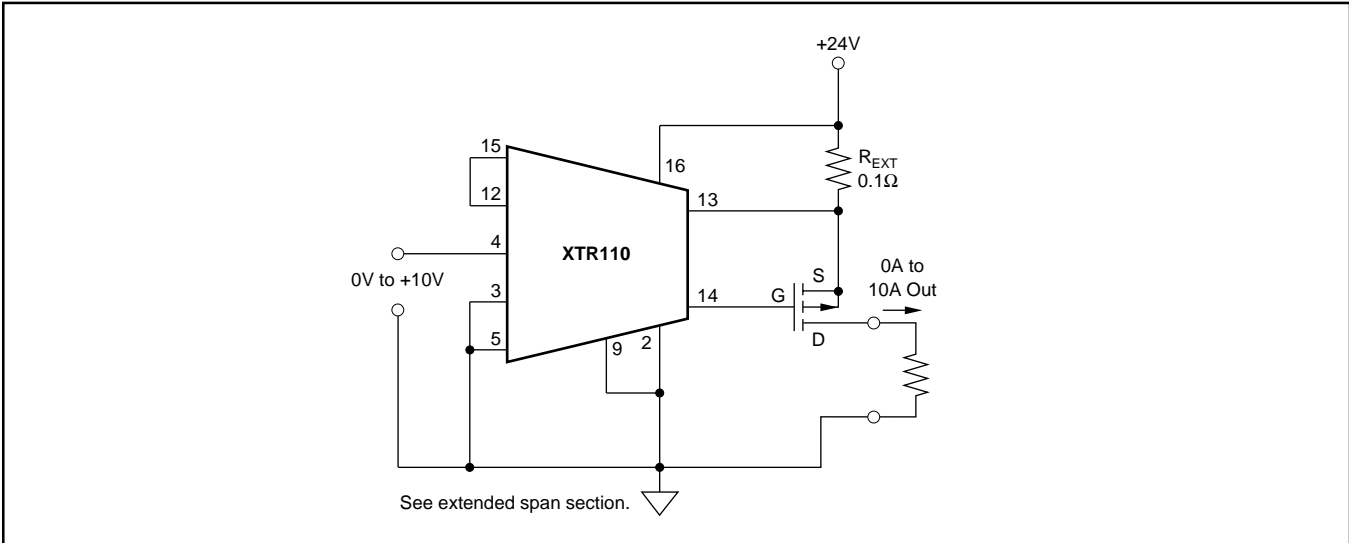


FIGURE 10. 0A to 10A Output Voltage-to-Current Converter.

Revision History

| DATE | REVISION | PAGE | SECTION | DESCRIPTION |
|------|----------|------|--------------------------|--|
| 9/09 | C | 6 | Front Page | Changed front page to standard format. |
| | | | Applications Information | Changed text in third paragraph. |

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| XTR110AG | ACTIVE | CDIP SB | JD | 16 | 24 | RoHS & Green | Call TI | N / A for Pkg Type | -40 to 85 | XTR110AG | Samples |
| XTR110BG | ACTIVE | CDIP SB | JD | 16 | 24 | RoHS & Green | Call TI | N / A for Pkg Type | -40 to 85 | XTR110BG | Samples |
| XTR110KP | ACTIVE | PDIP | N | 16 | 25 | RoHS & Green | NIPDAU | N / A for Pkg Type | -40 to 85 | XTR110KP | Samples |
| XTR110KU | ACTIVE | SOIC | DW | 16 | 40 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 85 | XTR110KU | Samples |
| XTR110KU/1K | ACTIVE | SOIC | DW | 16 | 1000 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 85 | XTR110KU | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| XTR110KU/1K | SOIC | DW | 16 | 1000 | 330.0 | 16.4 | 10.75 | 10.7 | 2.7 | 12.0 | 16.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|-------------|--------------|-----------------|------|------|-------------|------------|-------------|
| XTR110KU/1K | SOIC | DW | 16 | 1000 | 356.0 | 356.0 | 35.0 |

TUBE

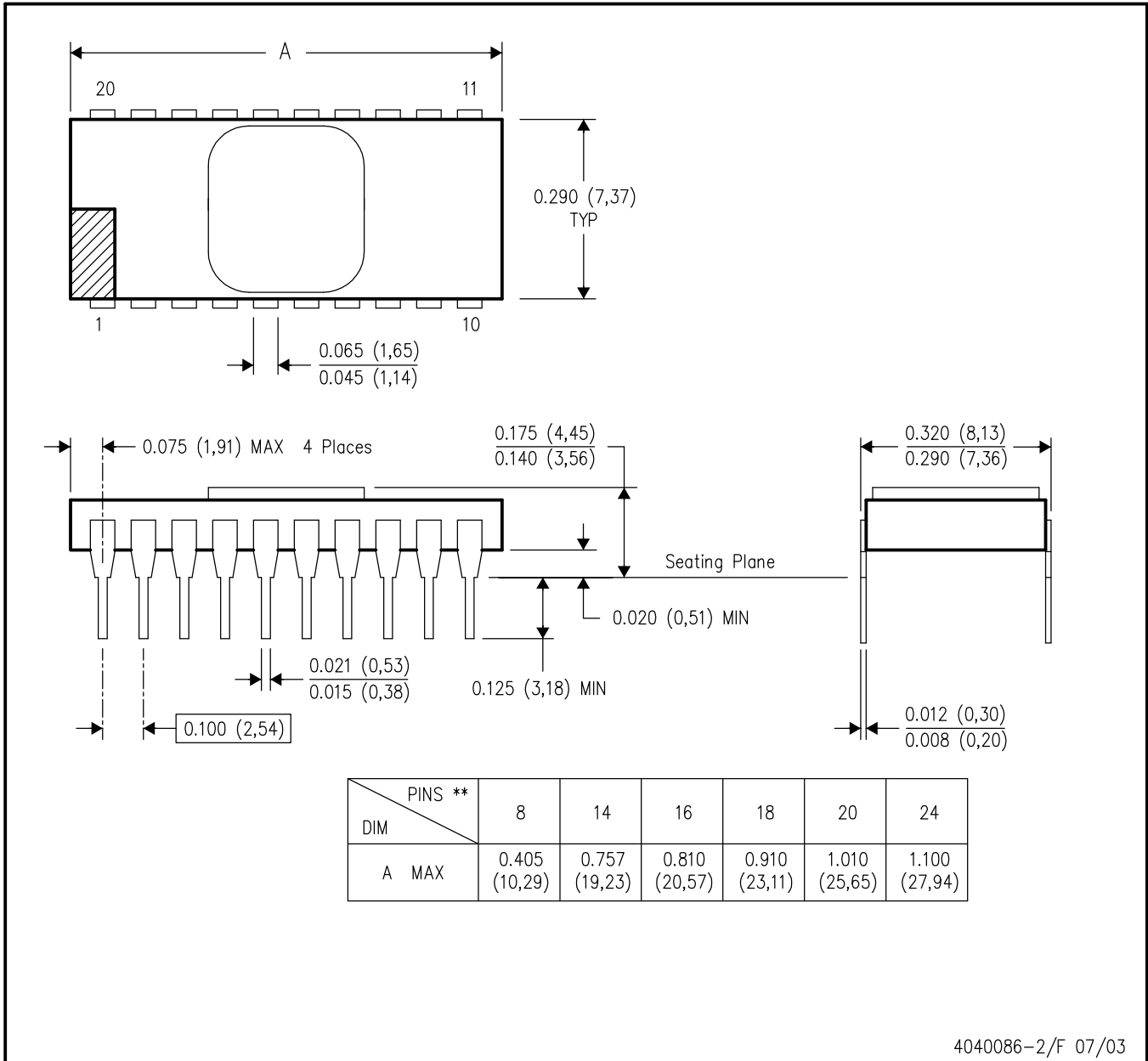

*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|----------|--------------|--------------|------|-----|--------|--------|--------|--------|
| XTR110AG | JD | CDIP SB | 16 | 24 | 506.98 | 15.24 | 12290 | NA |
| XTR110BG | JD | CDIP SB | 16 | 24 | 506.98 | 15.24 | 12290 | NA |
| XTR110KP | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| XTR110KU | DW | SOIC | 16 | 40 | 507 | 12.83 | 5080 | 6.6 |

JD (R-CDIP-T**)

CERAMIC SIDE-BRAZE DUAL-IN-LINE PACKAGE

20 PINS SHOWN



4040086-2/F 07/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package is hermetically sealed with a metal lid.
 - D. The terminals are gold plated.
 - E. Falls within MIL STD 1835 CDIP2 - T8, T14, T16, T18, T20 and T24 respectively.

GENERIC PACKAGE VIEW

DW 16

SOIC - 2.65 mm max height

7.5 x 10.3, 1.27 mm pitch

SMALL OUTLINE INTEGRATED CIRCUIT

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224780/A

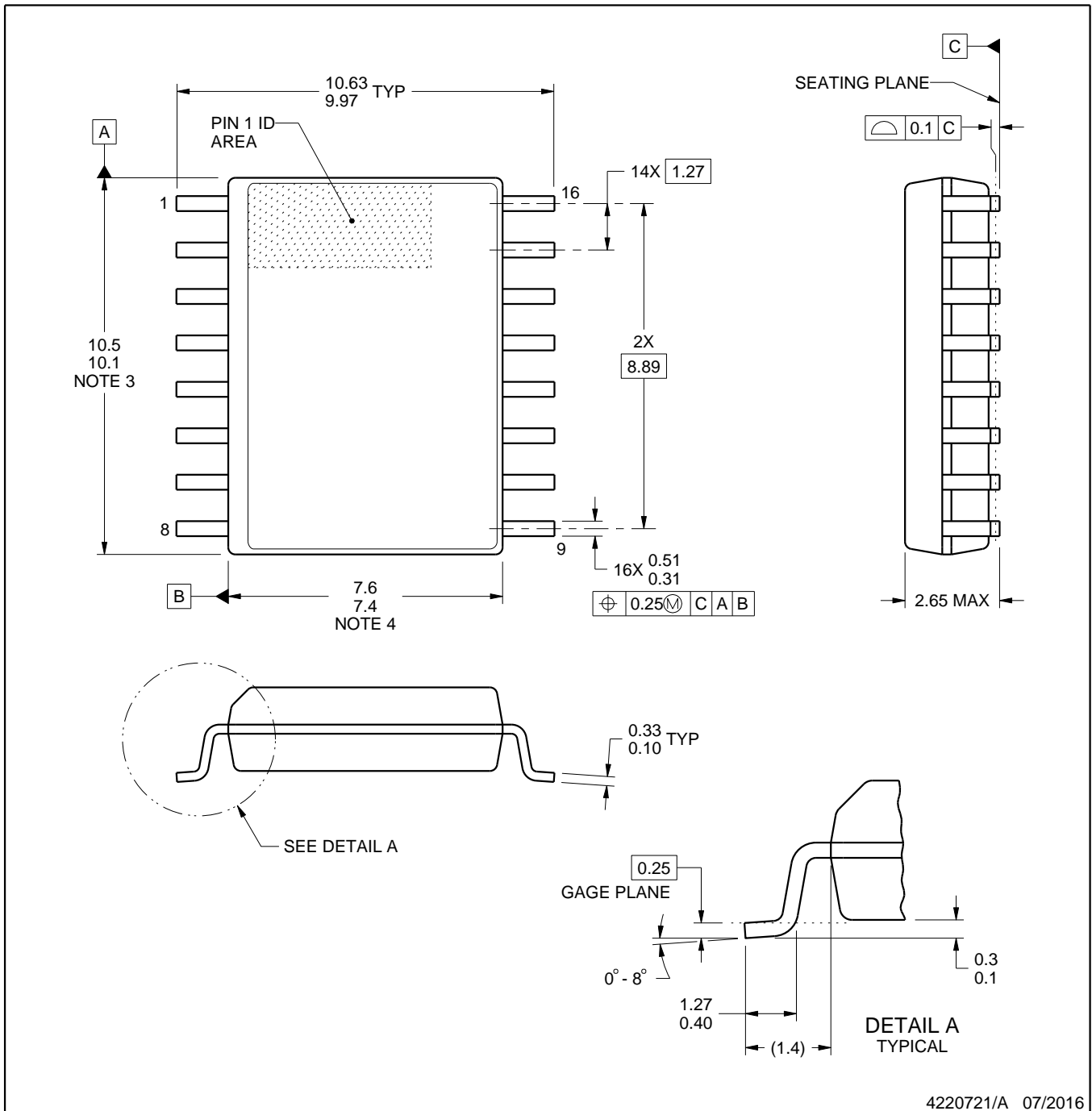


DW0016A

PACKAGE OUTLINE

SOIC - 2.65 mm max height

SOIC



4220721/A 07/2016

NOTES:

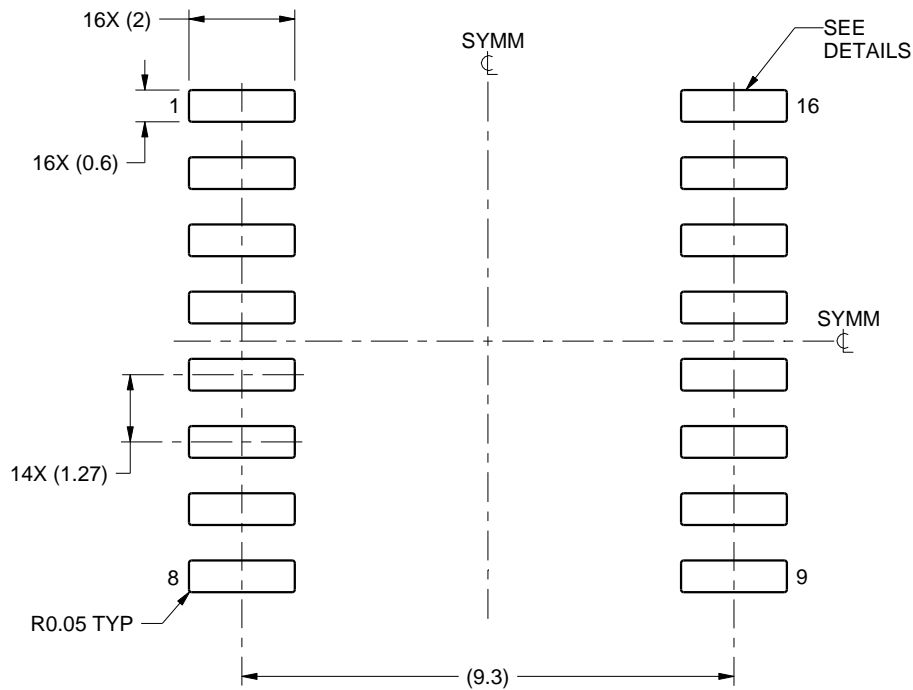
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.

EXAMPLE BOARD LAYOUT

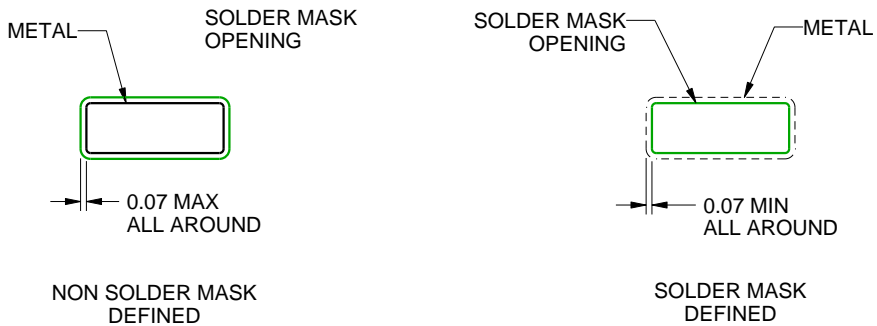
DW0016A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE
SCALE:7X



SOLDER MASK DETAILS

4220721/A 07/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

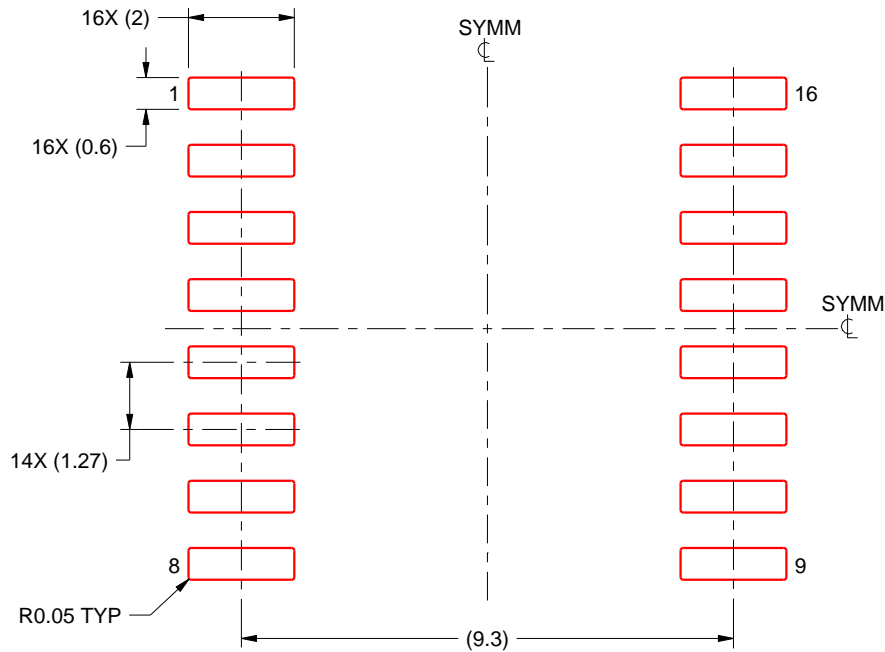
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0016A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220721/A 07/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - $\triangle C$ Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - $\triangle D$ The 20 pin end lead shoulder width is a vendor option, either half or full width.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](https://www.ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2024, Texas Instruments Incorporated