

TRSF3232E 3V TO 5.5V Two-Channel RS-232 1Mbit/s Line Driver and Receiver with $\pm 15\text{kV}$ IEC ESD Protection in Small Package

1 Features

- Operates with 3V to 5.5V V_{CC} supply
- Operates up to 1Mbit/s
- Low supply current: 300 μA typical
- External capacitors: 4 \times 0.1 μF
- Accept 5V logic input with 3.3V supply
- Latch-up performance exceeds 100mA Per JESD 78, class II
- ESD protection for RS-232 pins
 - $\pm 15\text{kV}$ Human-Body Model (HBM)
 - $\pm 15\text{kV}$ IEC 61000-4-2 air-gap discharge
 - $\pm 8\text{kV}$ IEC 61000-4-2 contact discharge
- Available in near chip scale QFN (3mm \times 3mm) package (85% smaller than SOIC-16)

2 Applications

- [Industrial PCs](#)
- [Wired networking](#)
- [Data center and enterprise computing](#)
- [Battery-powered systems](#)
- [PDAs](#)
- [Notebooks](#)
- [Palmtop PCs](#)
- [Hand-held equipment](#)

3 Description

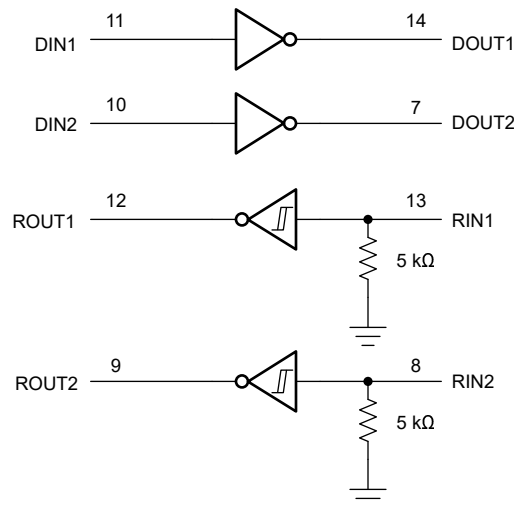
The TRSF3232E consists of two line drivers, two line receivers, and a dual charge-pump circuit with $\pm 15\text{kV}$ ESD protection pin to pin (serial-port connection pins, including GND). This device provides the electrical interface between an asynchronous communication controller and the serial-port connector. The charge pump and four small external capacitors allow operation from a single 3V to 5.5V supply. The TRSF3232E operates at data signaling rates up to 1Mbit/s and a driver output slew rate of 14V/ μs to 150V/ μs .

Package Information

| PART NUMBER | PACKAGE ⁽¹⁾ | PACKAGE SIZE ⁽²⁾ |
|-------------|------------------------|-----------------------------|
| TRSF3232E | D (SOIC) | 9.9mm x 6mm |
| | DB (SSOP) | 6.2mm x 7.8mm |
| | DW (SOIC) | 10.3 mm x 10.3mm |
| | PW (TSSOP) | 5mm x 6.4mm |
| | RGT (VQFN) | 3mm x 3mm |
| | SOT-23-THN (DYY, 16) | 4.2mm \times 2mm |

(1) For more information, see [Section 11](#).

(2) The package size (length \times width) is a nominal value and includes pins, where applicable.



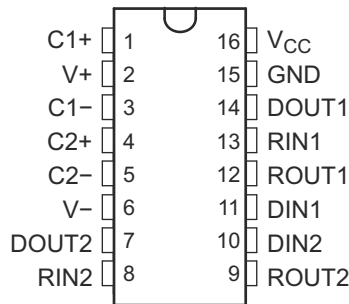
Logic Diagram (Positive Logic)



Table of Contents

| | | | |
|--|----|--|----|
| 1 Features | 1 | 7.1 Overview..... | 10 |
| 2 Applications | 1 | 7.2 Functional Block Diagram..... | 10 |
| 3 Description | 1 | 7.3 Feature Description..... | 10 |
| 4 Pin Configuration and Functions | 3 | 7.4 Device Functional Modes..... | 11 |
| 5 Specifications | 4 | 8 Application and Implementation | 12 |
| 5.1 Absolute Maximum Ratings..... | 4 | 8.1 Application Information..... | 12 |
| 5.2 ESD Ratings..... | 4 | 8.2 Typical Application..... | 12 |
| 5.3 ESD Protection, Driver..... | 4 | 8.3 Power Supply Recommendations..... | 13 |
| 5.4 ESD Protection, Receiver..... | 4 | 8.4 Layout..... | 13 |
| 5.5 Recommended Operating Conditions..... | 5 | 9 Device and Documentation Support | 15 |
| 5.6 Thermal Information..... | 5 | 9.1 Receiving Notification of Documentation Updates.... | 15 |
| 5.7 Electrical Characteristics..... | 5 | 9.2 Support Resources..... | 15 |
| 5.8 Electrical Characteristics, Driver..... | 6 | 9.3 Trademarks..... | 15 |
| 5.9 Electrical Characteristics, Receiver..... | 6 | 9.4 Electrostatic Discharge Caution..... | 15 |
| 5.10 Switching Characteristics, Driver..... | 7 | 9.5 Glossary..... | 15 |
| 5.11 Switching Characteristics, Receiver..... | 7 | 10 Revision History | 15 |
| 5.12 Typical Characteristics..... | 8 | 11 Mechanical, Packaging, and Orderable Information | 16 |
| 6 Parameter Measurement Information | 9 | | |
| 7 Detailed Description | 10 | | |

4 Pin Configuration and Functions



**Figure 4-1. D, DB, DW, PW or DYY Package
16-Pin SSOP, TSSOP, or SOT-23-THN
(Top View)**

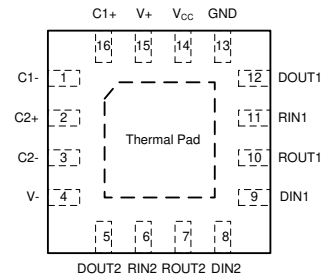


Figure 4-2. RGT, VQFN Package (Top View)

Table 4-1. Pin Functions

| NAME | PIN | | TYPE ⁽¹⁾ | DESCRIPTION |
|-----------------|----------------------|-------------|---------------------|--|
| | D, DB, DW, PW or DYY | RGT | | |
| C1+ | 1 | 16 | - | Positive lead of C1 capacitor |
| V+ | 2 | 15 | O | Positive charge pump output for storage capacitor only |
| C1- | 3 | 1 | - | Negative lead of C1 capacitor |
| C2+ | 4 | 2 | - | Positive lead of C2 capacitor |
| C2- | 5 | 3 | - | Negative lead of C2 capacitor |
| V- | 6 | 4 | O | Negative charge pump output for storage capacitor only |
| DOUT2 | 7 | 5 | O | RS232 line data output (to remote RS232 system) |
| RIN2 | 8 | 6 | I | RS232 line data input (from remote RS232 system) |
| ROUT2 | 9 | 7 | O | Logic data output (to UART) |
| DIN2 | 10 | 8 | I | Logic data input (from UART) |
| DIN1 | 11 | 9 | I | Logic data input (from UART) |
| ROUT1 | 12 | 10 | O | Logic data output (to UART) |
| RIN1 | 13 | 11 | I | RS232 line data input (from remote RS232 system) |
| DOUT1 | 14 | 12 | O | RS232 line data output (to remote RS232 system) |
| GRD | 15 | 13 | - | Ground |
| V _{CC} | 16 | 14 | - | Supply Voltage, Connect to external 3-V to 5.5-V power supply |
| Thermal Pad | - | Thermal Pad | - | Exposed thermal pad. Can be connected to GND or left floating. |

(1) Signal Types: I = Input, O = Output, I/O = Input or Output.

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) see note ⁽¹⁾

| | | MIN | MAX | UNIT | |
|------------------|---|-----------|-------|-----------------------|---|
| V _{CC} | Supply voltage range ⁽²⁾ | -0.3 | 6 | V | |
| V+ | Positive-output supply voltage range ⁽²⁾ | -0.3 | 7 | V | |
| V- | Negative-output supply voltage range ⁽²⁾ | 0.3 | -7 | V | |
| V+ – V- | Supply voltage difference ⁽²⁾ | | 13 | V | |
| V _I | Input voltage range | Drivers | -0.3 | 6 | V |
| | | Receivers | -25 | 25 | |
| V _O | Output voltage range | Drivers | -13.2 | 13.2 | V |
| | | Receivers | -0.3 | V _{CC} + 0.3 | |
| T _J | Operating virtual junction temperature | | 150 | °C | |
| T _{stg} | Storage temperature range | -65 | 150 | °C | |

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages are with respect to network GND.

5.2 ESD Ratings

| | | VALUE | UNIT | |
|--------------------|-------------------------|--|-------|---|
| V _(ESD) | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ¹ . | ±3000 | V |
| | | Charged-device model (CDM), per JEDEC specification JESD22-C101 ² | ±1500 | |

5.3 ESD Protection, Driver

| PIN NAME | TEST CONDITIONS | TYP | UNIT |
|-----------------------------|--|-----|------|
| DOUT1, DOUT2 ⁽²⁾ | Human-body model (HBM) | ±15 | kV |
| | IEC 61000-4-2 Air-Gap Discharge ⁽¹⁾ | ±15 | |
| | IEC 61000-4-2 Contact Discharge ⁽¹⁾ | ±8 | |

- (1) For RGT, D and PW packages only: A minimum of 1-μF capacitor is needed between V_{CC} and GND to meet the specified IEC ESD level.
- (2) For optimized IEC ESD performance for DYY package, the recommendation is to have series resistor (≥ 50Ω), on all logic inputs directly connected to power or ground, to minimize the transient currents going into or out of the logic pins.

5.4 ESD Protection, Receiver

| PIN NAME | TEST CONDITIONS | TYP | UNIT |
|---------------------------|--|-----|------|
| RIN1, RIN2 ⁽²⁾ | HBM | ±15 | kV |
| | IEC 61000-4-2 Air-Gap Discharge ⁽¹⁾ | ±15 | |
| | IEC 61000-4-2 Contact Discharge ⁽¹⁾ | ±8 | |

- (1) For RGT, D and PW packages only: A minimum of 1-μF capacitor is needed between V_{CC} and GND to meet the specified IEC ESD level.
- (2) For optimized IEC ESD performance for DYY package, the recommendation is to have series resistor (≥ 50Ω), on all logic inputs directly connected to power or ground, to minimize the transient currents going into or out of the logic pins.

5.5 Recommended Operating Conditions

See note ⁽¹⁾

| | | | MIN | NOM | MAX | UNIT |
|----------------|---------------------------------|-------------------------|-------------------------|-----|-----|------|
| Supply voltage | | $V_{CC} = 3.3\text{ V}$ | 3 | 3.3 | 3.6 | V |
| | | $V_{CC} = 5\text{ V}$ | 4.5 | 5 | 5.5 | |
| V_{IH} | Driver high-level input voltage | DIN | $V_{CC} = 3.3\text{ V}$ | | 2 | V |
| | | | $V_{CC} = 5\text{ V}$ | | 2.4 | |
| V_{IL} | Driver low-level input voltage | DIN | | | 0.8 | V |
| V_I | Driver input voltage | DIN | 0 | 5.5 | | V |
| | Receiver input voltage | | -25 | | 25 | |
| T_A | Operating free-air temperature | TRSF3232EI | -40 | | 85 | °C |
| | | TRSF3232EC | 0 | | 70 | |

(1) Test conditions are $C1-C4 = 0.1\ \mu\text{F}$ at $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$; $C1 = 0.047\ \mu\text{F}$, $C2-C4 = 0.33\ \mu\text{F}$ at $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (see [Figure 8-1](#)).

5.6 Thermal Information

| THERMAL METRIC ⁽¹⁾ | | TRSF3232E | | | | | | UNIT |
|-------------------------------|--|------------|----------|-----------|-----------|------------|------------------|------|
| | | PW (TSSOP) | D (SOIC) | DW (SOIC) | DB (SSOP) | RGT (VQFN) | DYY (SOT-23-THN) | |
| | | 16 Pins | 16 Pins | 16 Pins | 16 Pins | 16 Pins | 16 Pins | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 108.2 | 85.9 | 57 | 46 | 48.8 | 106.2 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (bottom) thermal resistance | 39.0 | 43.1 | 33.5 | 36.2 | 55.8 | 47.4 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 54.4 | 44.5 | 37.1 | 43.8 | 23.2 | 44.7 | °C/W |
| Ψ_{JT} | Junction-to-top characterization parameter | 3.3 | 10.1 | 7.5 | 4.2 | 1.7 | 1.7 | °C/W |
| Ψ_{JB} | Junction-to-board characterization parameter | 53.8 | 44.1 | 37.1 | 42.9 | 23.2 | 43.7 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | N/A | N/A | N/A | N/A | 9.0 | N/A | °C/W |

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC package thermal metrics](#) application report.

5.7 Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS ⁽¹⁾ | | MIN | TYP ⁽²⁾ | MAX | UNIT |
|-----------|----------------|--------------------------------|---|-----|--------------------|-----|------|
| I_{CC} | Supply current | No load, | $V_{CC} = 3.3\text{ V}$ or 5 V | | 0.3 | 1 | mA |

(1) Test conditions are $C1-C4 = 0.1\ \mu\text{F}$ at $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$; $C1 = 0.047\ \mu\text{F}$, $C2-C4 = 0.33\ \mu\text{F}$ at $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (see [Figure 8-1](#)).

(2) All typical values are at $V_{CC} = 3.3\text{ V}$ or $V_{CC} = 5\text{ V}$, and $T_A = 25^\circ\text{C}$.

5.8 Electrical Characteristics, Driver

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | TEST CONDITIONS ⁽¹⁾ | MIN | TYP ⁽²⁾ | MAX | UNIT |
|---|---|------------------------|--------------------|-----|------|
| V _{OH} High-level output voltage | DOUT at R _L = 3 kΩ to GND, DIN = GND | 5 | 5.5 | | V |
| V _{OL} Low-level output voltage | DOUT at R _L = 3 kΩ to GND, DIN = V _{CC} | –5 | –5.4 | | V |
| I _{IH} High-level input current | V _I = V _{CC} | | ±0.01 | ±1 | μA |
| I _{IL} Low-level input current | V _I at GND | | ±0.01 | ±1 | μA |
| I _{OS} ⁽³⁾ Short-circuit output current | V _{CC} = 3.6 V, V _O = 0 V | | ±35 | ±60 | mA |
| | V _{CC} = 5.5 V, V _O = 0 V | RGT package only | ±35 | ±60 | |
| | | D, DB, DW, PW packages | ±35 | ±90 | |
| r _o Output resistance | V _{CC} , V+, and V– = 0 V, V _O = ±2 V | 300 | 10M | | Ω |

(1) Test conditions are C1–C4 = 0.1 μF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 μF, C2–C4 = 0.33 μF at V_{CC} = 5 V ± 0.5 V (see Figure 8-1).

(2) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

(3) Short-circuit durations should be controlled to prevent exceeding the device absolute power dissipation ratings, and not more than one output should be shorted at a time.

5.9 Electrical Characteristics, Receiver

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | TEST CONDITIONS ⁽¹⁾ | MIN | TYP ⁽²⁾ | MAX | UNIT |
|--|--------------------------------|-----------------------|-----------------------|-----|------|
| V _{OH} High-level output voltage | I _{OH} = –1 mA | V _{CC} – 0.6 | V _{CC} – 0.1 | | V |
| V _{OL} Low-level output voltage | I _{OL} = 1.6 mA | | | 0.4 | V |
| V _{IT+} Positive-going input threshold voltage | V _{CC} = 3.3 V | | 1.5 | 2.4 | V |
| | V _{CC} = 5 V | | 1.8 | 2.4 | |
| V _{IT–} Negative-going input threshold voltage | V _{CC} = 3.3 V | 0.6 | 1.2 | | V |
| | V _{CC} = 5 V | 0.8 | 1.5 | | |
| V _{hys} Input hysteresis (V _{IT+} – V _{IT–}) | | | 0.3 | | V |
| r _i Input resistance | V _I = ±3 V to ±25 V | 3 | 5 | 7 | kΩ |

(1) Test conditions are C1–C4 = 0.1 μF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 μF, C2–C4 = 0.33 μF at V_{CC} = 5 V ± 0.5 V (see Figure 8-1).

(2) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

5.10 Switching Characteristics, Driver

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| | | TEST CONDITIONS ⁽¹⁾ | | MIN | TYP ⁽²⁾ | MAX | UNIT |
|--|--|--|--|------|--------------------|-----|--------|
| Maximum data rate (see Figure 6-1) | R _L = 3 kΩ, One DOUT switching | C _L = 250 pF, V _{CC} = 3 V to 4.5 V | | 1000 | | | kbit/s |
| | | C _L = 1000 pF, V _{CC} = 3.5 V to 5.5 V | | 1000 | | | |
| t _{sk(p)} Pulse skew ⁽³⁾ | C _L = 1000 pF, R _L = 3 kΩ, V _{CC} = 5 V (see Figure 6-2) | RGT package only | | 70 | | | ns |
| | C _L = 150 pF to 2500 pF, R _L = 3 kΩ to 7 kΩ (see Figure 6-2) | D, DB, DW, PW packages | | 300 | | | |
| SR(tr) Slew rate, transition region (see Figure 6-1) | R _L = 3 kΩ to 7 kΩ, C _L = 150 pF to 1000 pF, V _{CC} = 3.3 V | | | 14 | | 150 | V/μs |

(1) Test conditions are C1–C4 = 0.1 μF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 μF, C2–C4 = 0.33 μF at V_{CC} = 5 V ± 0.5 V (see Figure 8-1).

(2) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

(3) Pulse skew is defined as |t_{PLH} – t_{PHL}| of each channel of the same device.

5.11 Switching Characteristics, Receiver

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| | | TEST CONDITIONS ⁽¹⁾ | | MIN | TYP ⁽²⁾ | MAX | UNIT |
|--|-------------------------|--------------------------------|--|-----|--------------------|-----|------|
| t _{PLH} Propagation delay time, low- to high-level output | C _L = 150 pF | RGT package | | 85 | | | ns |
| | | D, DB, DW, PW packages | | 300 | | | |
| t _{PHL} Propagation delay time, high- to low-level output | C _L = 150 pF | RGT package | | 110 | | | ns |
| | | D, DB, DW, PW packages | | 300 | | | |
| t _{sk(p)} Pulse skew ⁽³⁾ | RGT package | | | 25 | | | ns |
| | D, DB, DW, PW packages | | | 300 | | | |

(1) Test conditions are C1–C4 = 0.1 μF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 μF, C2–C4 = 0.33 μF at V_{CC} = 5 V ± 0.5 V (see Figure 8-1).

(2) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

(3) Pulse skew is defined as |t_{PLH} – t_{PHL}| of each channel of the same device.

5.12 Typical Characteristics

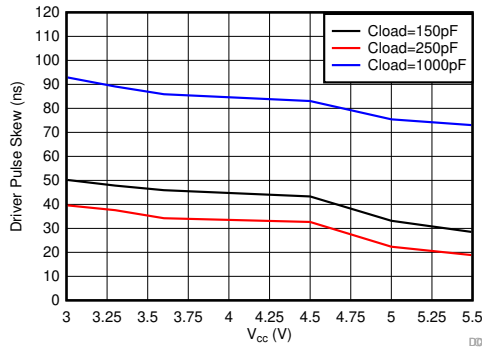


Figure 5-1. Driver pulse skew at $T_A = 25^\circ\text{C}$ (RGT package)

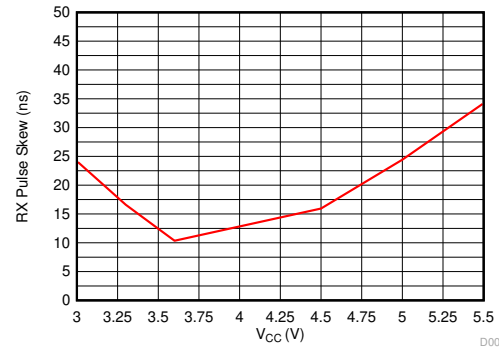


Figure 5-2. Receiver path skew at $T_A = 25^\circ\text{C}$ ($t_{pHL} - t_{pLH}$) (RGT package)

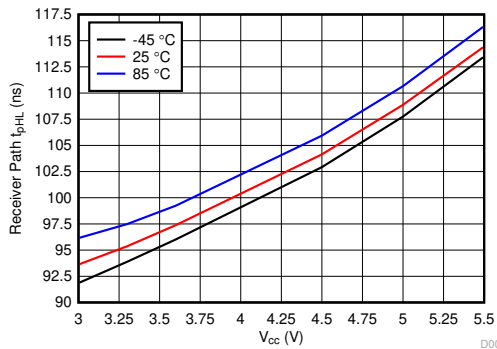


Figure 5-3. Receiver path high-to-low propagation delay, $C_L = 150\text{pF}$ (RGT package)

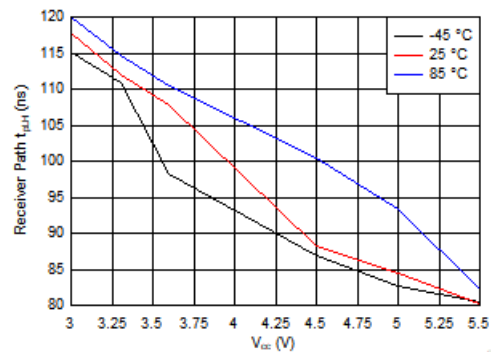
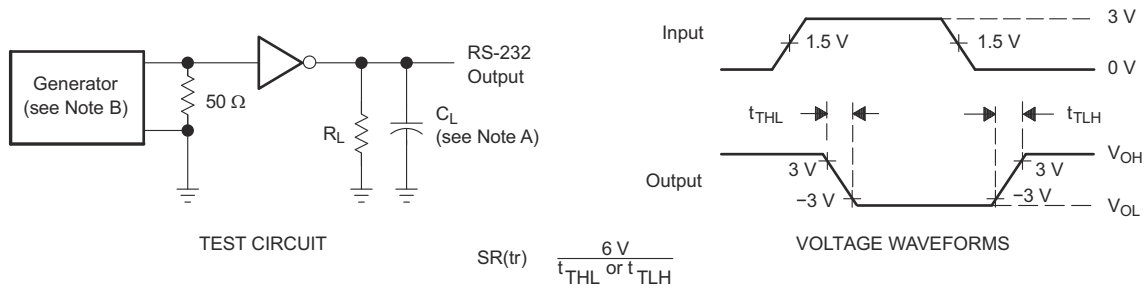


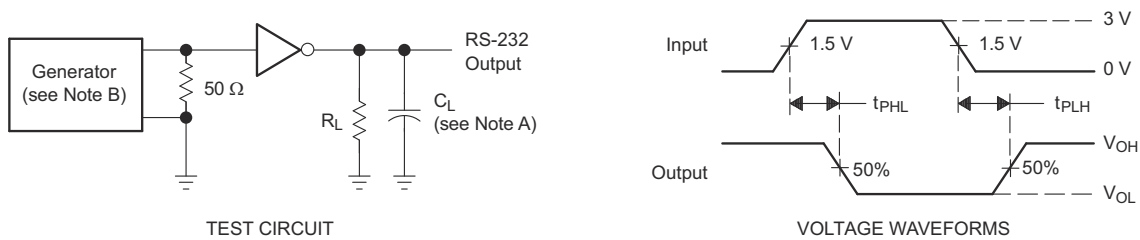
Figure 5-4. Receiver path low-to-high propagation delay, $C_L = 150\text{pF}$ (RGT package)

6 Parameter Measurement Information



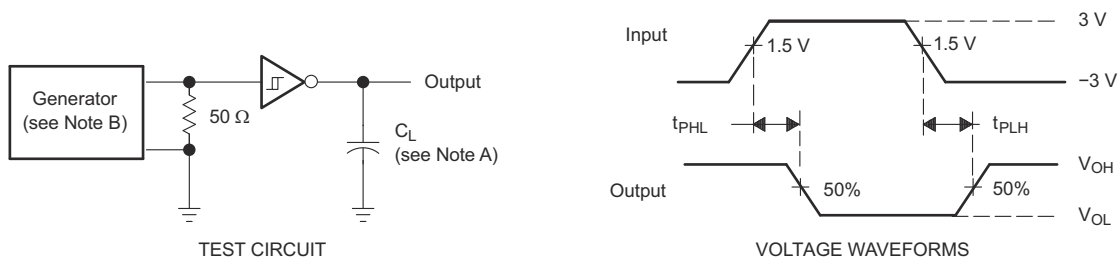
NOTES: A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: PRR = 250 kbit/s, $Z_O = 50\ \Omega$, 50% duty cycle, $t_r \leq 10\text{ ns}$, $t_f \leq 10\text{ ns}$.

Figure 6-1. Driver Slew Rate



NOTES: A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: PRR = 250 kbit/s, $Z_O = 50\ \Omega$, 50% duty cycle, $t_r \leq 10\text{ ns}$, $t_f \leq 10\text{ ns}$.

Figure 6-2. Driver Pulse Skew



NOTES: A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: $Z_O = 50\ \Omega$, 50% duty cycle, $t_r \leq 10\text{ ns}$, $t_f \leq 10\text{ ns}$.

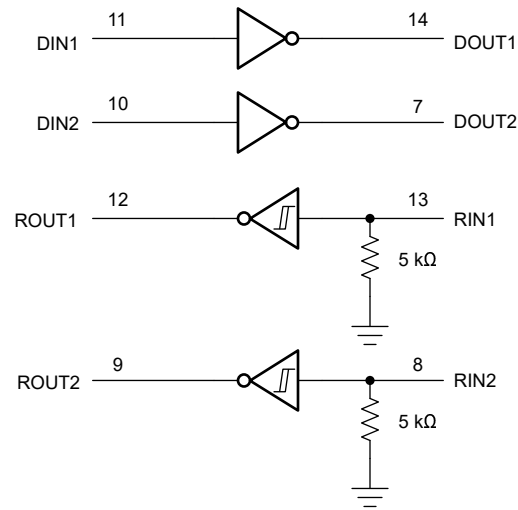
Figure 6-3. Receiver Propagation Delay Times

7 Detailed Description

7.1 Overview

The TRSF3232E device consists of two line drivers, two line receivers, and a dual charge-pump circuit with $\pm 15\text{kV}$ IEC ESD protection between serial-port connection terminals and GND. The device meets the requirements of TIA/EIA-232-F and provides the electrical interface between an asynchronous communication controller and the serial-port connector. The charge pump and four small external capacitors allow operation from one 3V to 5.5V supply. The device operates at data signaling rates up to 1Mbps and a maximum of $150\text{V}/\mu\text{s}$ driver output slew rate. Outputs are protected against shorts to ground.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Power

The power block increases, inverts, and regulates voltage at V+ and V– pins using a charge pump that requires four external capacitors.

7.3.2 RS232 Driver

Two drivers interface the standard logic level to RS232 levels. Both DIN inputs must be valid high or low.

7.3.3 RS232 Receiver

Two receivers interface RS232 levels to standard logic levels. An open input results in a high output on ROUT. Each RIN input includes an internal standard RS232 load.

7.4 Device Functional Modes

Table 7-1. Each Driver

| INPUT DIN ⁽¹⁾ | OUTPUT DOUT |
|--------------------------|-------------|
| L | H |
| H | L |

(1) H = high level, L = low level

Table 7-2. Each Receiver

| INPUT RIN ⁽¹⁾ | OUTPUT ROUT |
|--------------------------|-------------|
| L | H |
| H | L |
| Open | H |

(1) H = high level, L = low level,
Open = input disconnected or connected driver off

7.4.1 V_{CC} Powered by 3V to 5.5V

The device is in normal operation.

7.4.2 V_{CC} Unpowered, $V_{CC} = 0V$

When the TRS3232 device is unpowered, it can be safely connected to an active remote RS232 device.

8 Application and Implementation

Note

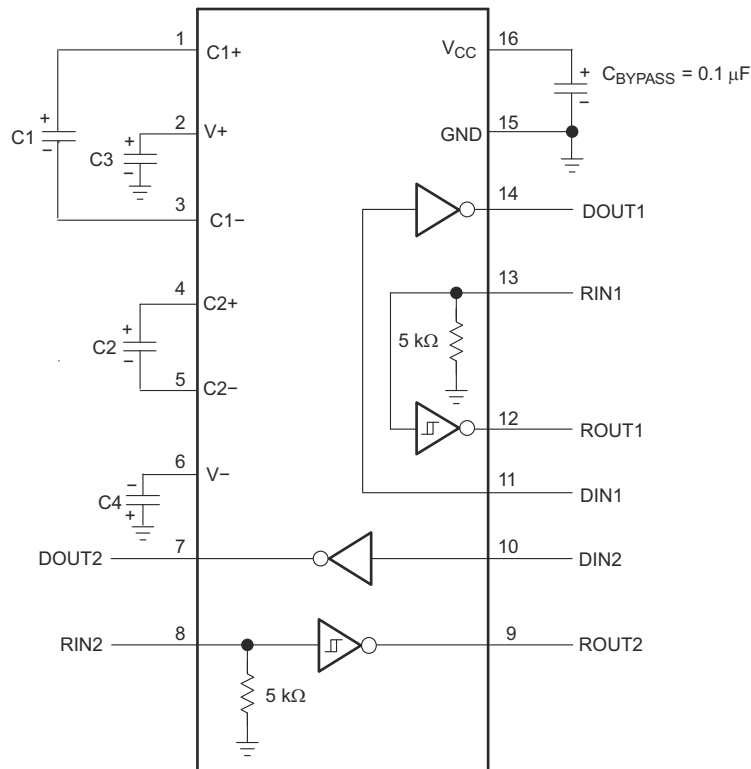
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The TRSF3232E device is designed to convert single-ended signals into RS232-compatible signals, and vice-versa. This device can be used in any application where an RS232 line driver or receiver is required.

ROUT and DIN connect to UART or general-purpose logic lines. RIN and DOUT lines connect to a RS232 connector or cable.

8.2 Typical Application



A. C3 can be connected to V_{CC} or GND.

Figure 8-1. Typical Operating Circuit and Capacitor Values

Table 8-1. VCC vs Capacitor Values

| V_{CC} | C1 | C2, C3, C4 |
|-----------------|---------------|--------------|
| $3.3V \pm 0.3V$ | 0.1 μ F | 0.1 μ F |
| $5V \pm 0.5V$ | 0.047 μ F | 0.33 μ F |
| 3V to 5.5V | 0.1 μ F | 0.47 μ F |

8.2.1 Design Requirements

- Recommended V_{CC} is 3.3V or 5V
 - 3V to 5.5V is also possible
- Maximum recommended bit rate is 250kbites

8.2.2 Detailed Design Procedure

All DIN inputs must be connected to valid low or high logic levels. Select capacitor values based on VCC level for best performance.

8.2.3 Application Performance Plots

VCC must be between 3 V and 5.5 V. Charge pump capacitors must be chosen using [Table 8-1](#)

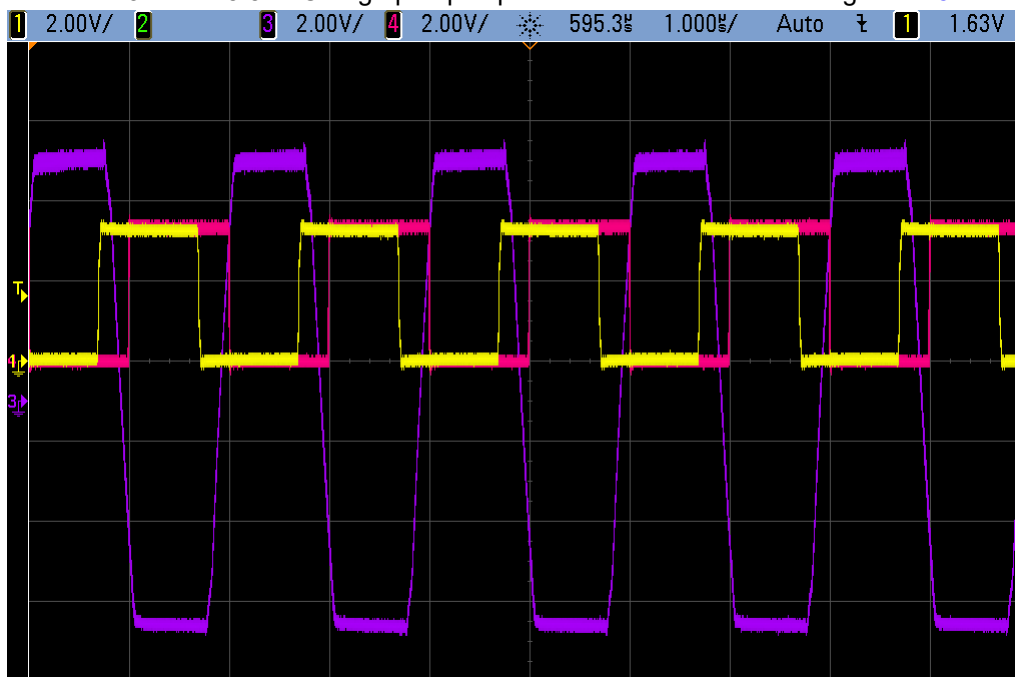


Figure 8-2. 1Mbps timing waveform from driver input to receiver output loopback. DOUT to RIN trace is in purple, DIN trace is in yellow and ROUT trace is in pink

8.3 Power Supply Recommendations

The supply voltage, V_{CC} , should be between 3V and 5.5V. Select the charge-pump capacitors using [Table 8-1](#).

8.4 Layout

8.4.1 Layout Guidelines

Keep the external capacitor traces short, specifically on the C1 and C2 nodes that have the fastest rise and fall times.

8.4.2 Layout Example

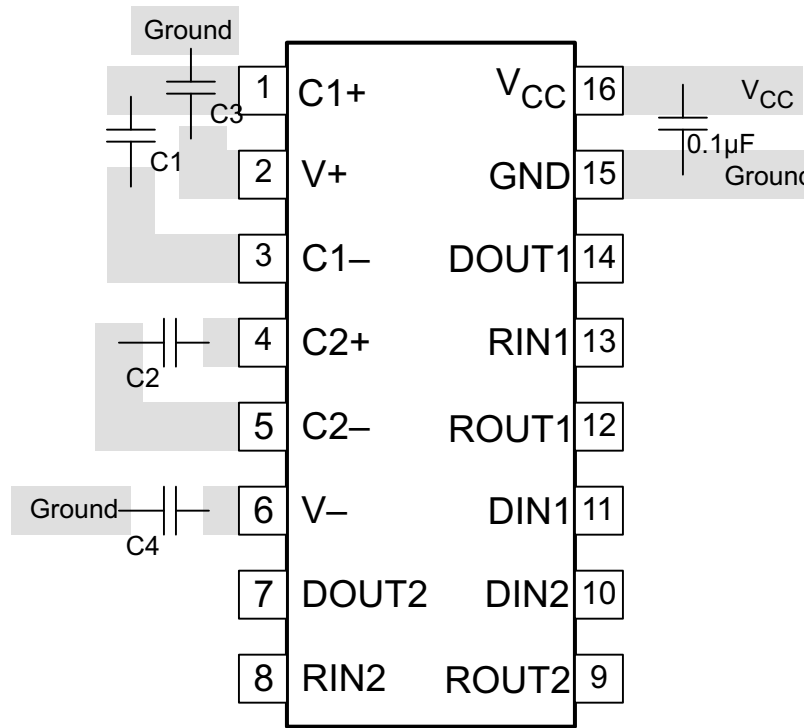


Figure 8-3. Layout Diagram

9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

9.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.2 Support Resources

TI E2E™ [support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

9.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
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9.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.5 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Revision B (June 2021) to Revision C (December 2024) | Page |
|--|-------------|
| • Changed the <i>Device Information</i> table to the <i>Package Information</i> table..... | 1 |
| • Added the SOT-23-THN (DYY) package to the data sheet..... | 1 |
| • Added Note 2 to the <i>ESD Protection, Driver</i> | 4 |
| • Added Note 2 to the <i>ESD Protection, Receiver</i> | 4 |

| Changes from Revision A (December 2020) to Revision B (June 2021) | Page |
|---|-------------|
| • Added <i>Applications</i> : Industrial PCs, Wired networking, and Data center and enterprise computing..... | 1 |
| • Changed the table note in the <i>ESD Protection, Driver</i> table to make it applicable to D and PW packages..... | 4 |
| • Changed the table note in the <i>ESD Protection, Receiver</i> table to make it applicable to D and PW packages.. | 4 |
| • Changed the thermal parameter values for D and PW packages in the <i>Thermal Information</i> table..... | 5 |

| Changes from Revision * (August 2007) to Revision A (December 2020) | Page |
|--|-------------|
| • Added Device Information table, ESD Ratings table, Feature Description section, Device Functional Modes, Application and Implementation section, Power Supply Recommendations section, Layout section, Device and Documentation Support section, and Mechanical, Packaging, and Orderable Information section..... | 1 |
| • Added Note to the <i>ESD Protection, Driver</i> | 4 |

| | |
|--|---|
| • Added Note to the <i>ESD Protection, Receiver</i> | 4 |
| • Added $t_{sk(p)}$ row for RGT package in the <i>Switching Characteristics, Driver</i> | 7 |
| • Added t_{PLH} and t_{PHL} rows for RGT package in the <i>Switching Characteristics, Receiver</i> | 7 |
| • Added $t_{sk(p)}$ row for RGT package in the <i>Switching Characteristics, Receiver</i> | 7 |

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| TRSF3232ECDDBR | ACTIVE | SSOP | DB | 16 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | RT32EC | Samples |
| TRSF3232ECDR | ACTIVE | SOIC | D | 16 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | TRSF3232EC | Samples |
| TRSF3232ECDWR | OBSOLETE | SOIC | DW | 16 | | TBD | Call TI | Call TI | 0 to 70 | TRSF3232EC | |
| TRSF3232ECPWR | ACTIVE | TSSOP | PW | 16 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | RT32EC | Samples |
| TRSF3232EID | OBSOLETE | SOIC | D | 16 | | TBD | Call TI | Call TI | -40 to 85 | TRSF3232EI | |
| TRSF3232EIDBR | ACTIVE | SSOP | DB | 16 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | RT32EI | Samples |
| TRSF3232EIDR | ACTIVE | SOIC | D | 16 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | TRSF3232EI | Samples |
| TRSF3232EIDW | ACTIVE | SOIC | DW | 16 | 40 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | TRSF3232EI | Samples |
| TRSF3232EIDWR | ACTIVE | SOIC | DW | 16 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | TRSF3232EI | Samples |
| TRSF3232EIPWR | ACTIVE | TSSOP | PW | 16 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | RT32EI | Samples |
| TRSF3232EIRGTR | ACTIVE | VQFN | RGT | 16 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | F3232 | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

- (4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.
- (5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.
- (6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

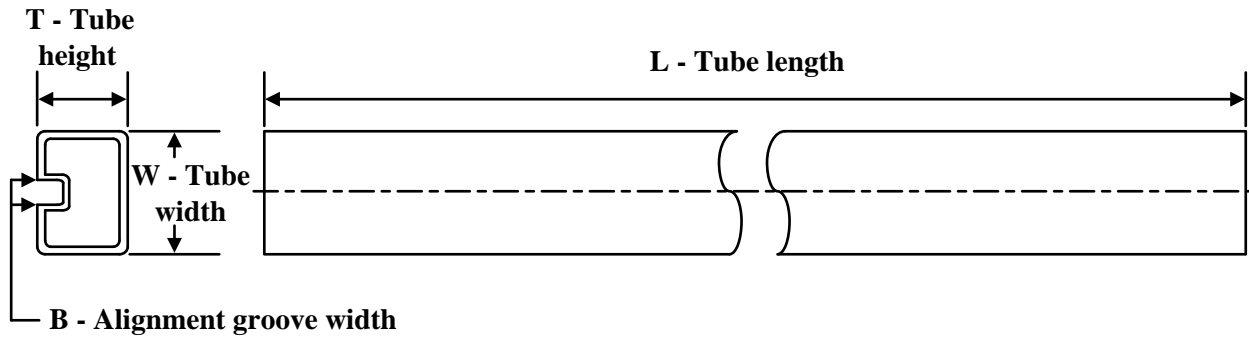

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TRSF3232ECDBR | SSOP | DB | 16 | 2000 | 330.0 | 16.4 | 8.35 | 6.6 | 2.4 | 12.0 | 16.0 | Q1 |
| TRSF3232ECDR | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |
| TRSF3232ECDR | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |
| TRSF3232ECPWR | TSSOP | PW | 16 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| TRSF3232EIDBR | SSOP | DB | 16 | 2000 | 330.0 | 16.4 | 8.35 | 6.6 | 2.4 | 12.0 | 16.0 | Q1 |
| TRSF3232EIDR | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |
| TRSF3232EIDR | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |
| TRSF3232EIDWR | SOIC | DW | 16 | 2000 | 330.0 | 16.4 | 10.75 | 10.7 | 2.7 | 12.0 | 16.0 | Q1 |
| TRSF3232EIPWR | TSSOP | PW | 16 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| TRSF3232EIPWR | TSSOP | PW | 16 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| TRSF3232EIRGTR | VQFN | RGT | 16 | 3000 | 330.0 | 12.4 | 3.3 | 3.3 | 1.1 | 8.0 | 12.0 | Q2 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| TRSF3232ECDBR | SSOP | DB | 16 | 2000 | 356.0 | 356.0 | 35.0 |
| TRSF3232ECDR | SOIC | D | 16 | 2500 | 356.0 | 356.0 | 35.0 |
| TRSF3232ECDR | SOIC | D | 16 | 2500 | 356.0 | 356.0 | 35.0 |
| TRSF3232ECPWR | TSSOP | PW | 16 | 2000 | 356.0 | 356.0 | 35.0 |
| TRSF3232EIDBR | SSOP | DB | 16 | 2000 | 356.0 | 356.0 | 35.0 |
| TRSF3232EIDR | SOIC | D | 16 | 2500 | 356.0 | 356.0 | 35.0 |
| TRSF3232EIDR | SOIC | D | 16 | 2500 | 356.0 | 356.0 | 35.0 |
| TRSF3232EIDWR | SOIC | DW | 16 | 2000 | 350.0 | 350.0 | 43.0 |
| TRSF3232EIPWR | TSSOP | PW | 16 | 2000 | 356.0 | 356.0 | 35.0 |
| TRSF3232EIPWR | TSSOP | PW | 16 | 2000 | 356.0 | 356.0 | 35.0 |
| TRSF3232EIRGTR | VQFN | RGT | 16 | 3000 | 367.0 | 367.0 | 35.0 |

TUBE


*All dimensions are nominal

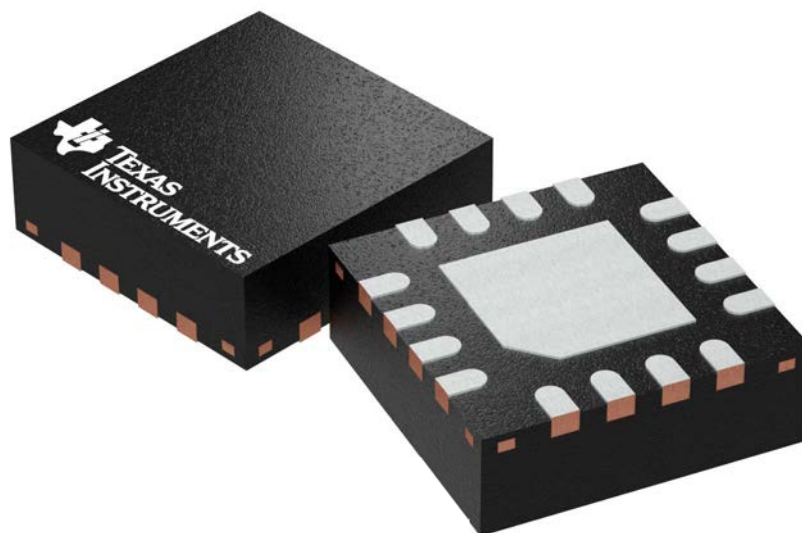
| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|--------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| TRSF3232EIDW | DW | SOIC | 16 | 40 | 506.98 | 12.7 | 4826 | 6.6 |

RGT 16

GENERIC PACKAGE VIEW

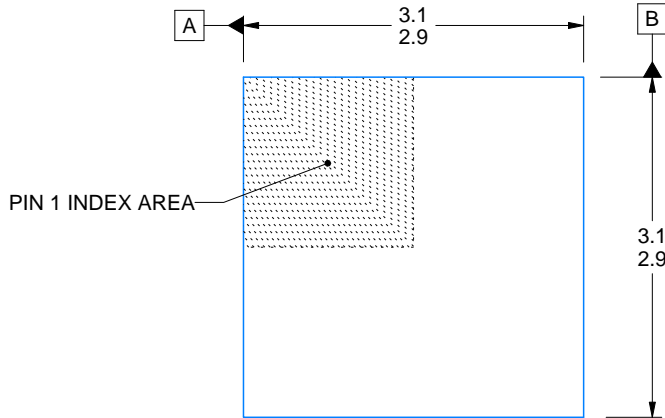
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

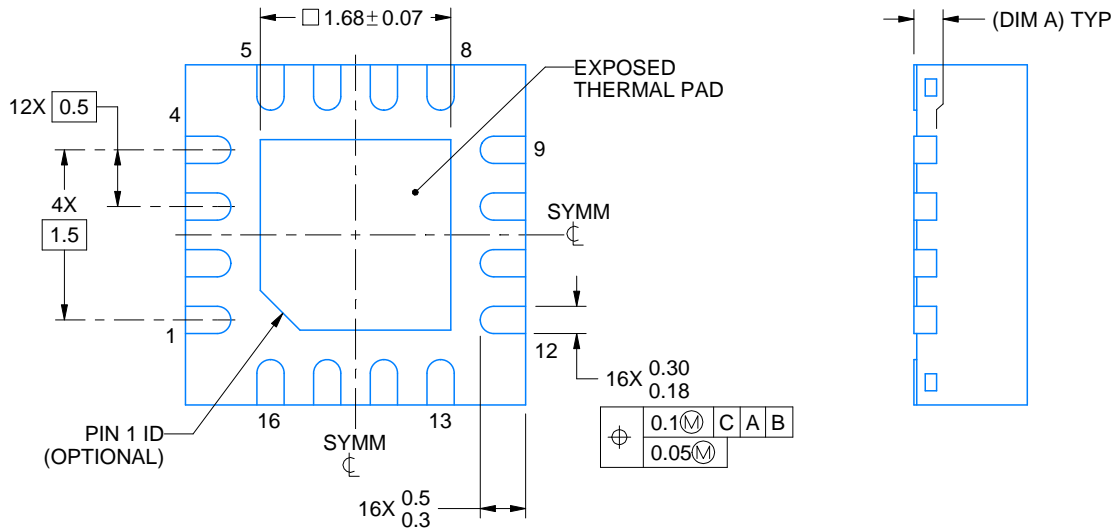


Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4203495/1



| SIDE WALL METAL THICKNESS DIM A | |
|---------------------------------|----------|
| OPTION 1 | OPTION 2 |
| 0.1 | 0.2 |



4222419/D 04/2022

NOTES:

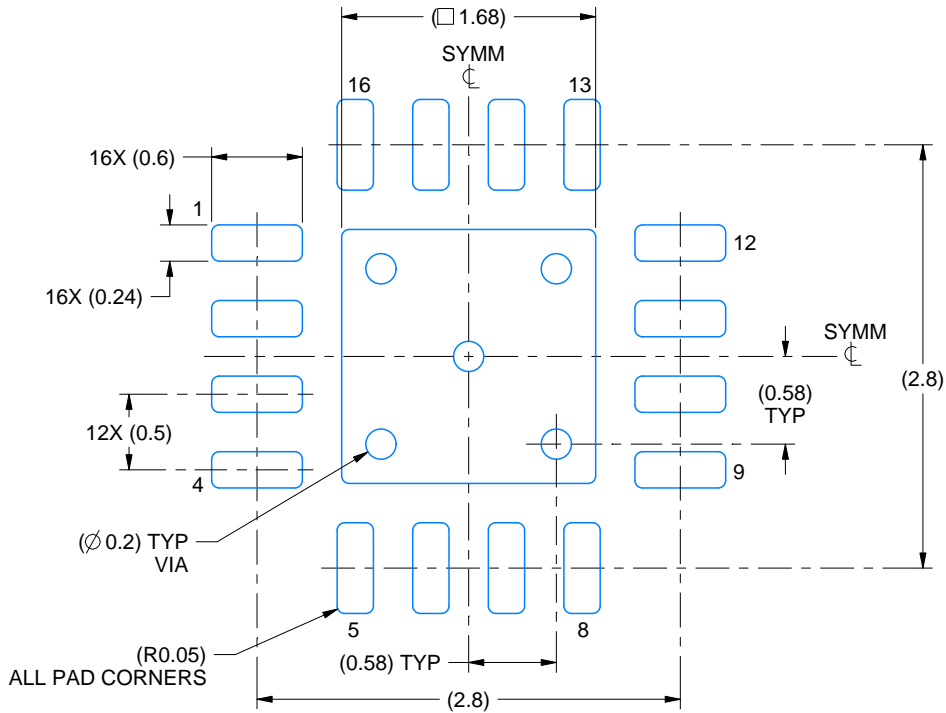
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

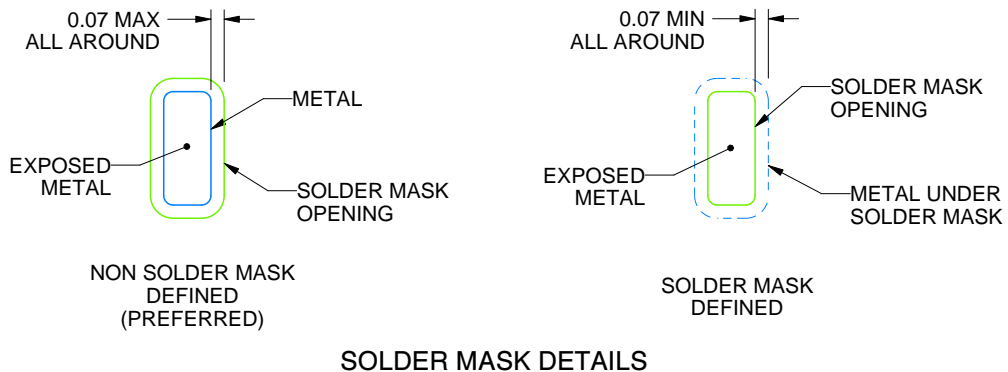
RGT0016C

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



SOLDER MASK DETAILS

4222419/D 04/2022

NOTES: (continued)

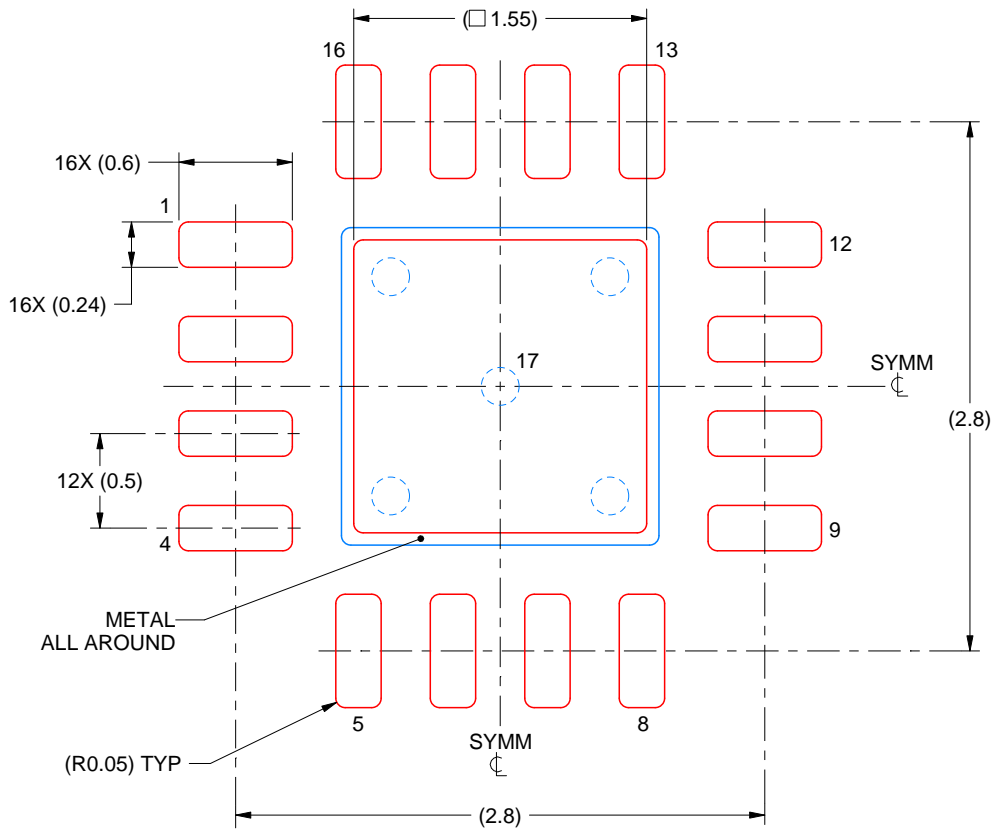
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RGT0016C

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17:
85% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

4222419/D 04/2022

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AC.



4220204/A 02/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

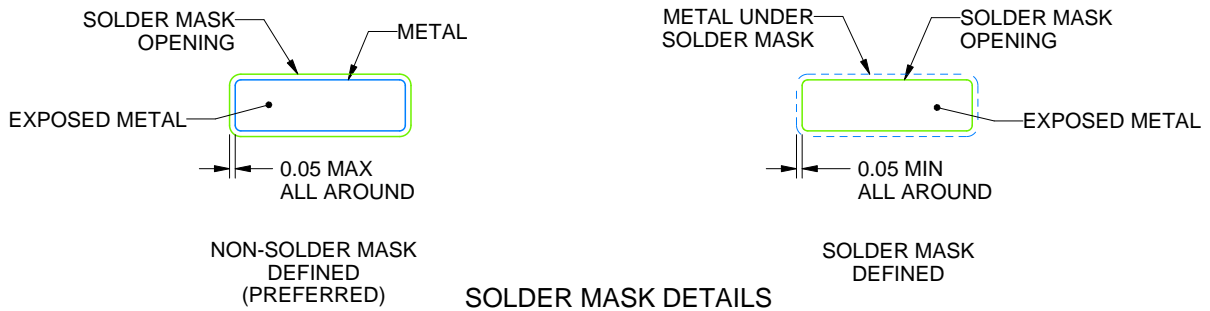
PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4220204/A 02/2017

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DB0016A



PACKAGE OUTLINE

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



4220763/A 05/2022

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-150.

EXAMPLE BOARD LAYOUT

DB0016A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4220763/A 05/2022

NOTES: (continued)

- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DB0016A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220763/A 05/2022

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

DW 16

SOIC - 2.65 mm max height

7.5 x 10.3, 1.27 mm pitch

SMALL OUTLINE INTEGRATED CIRCUIT

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224780/A

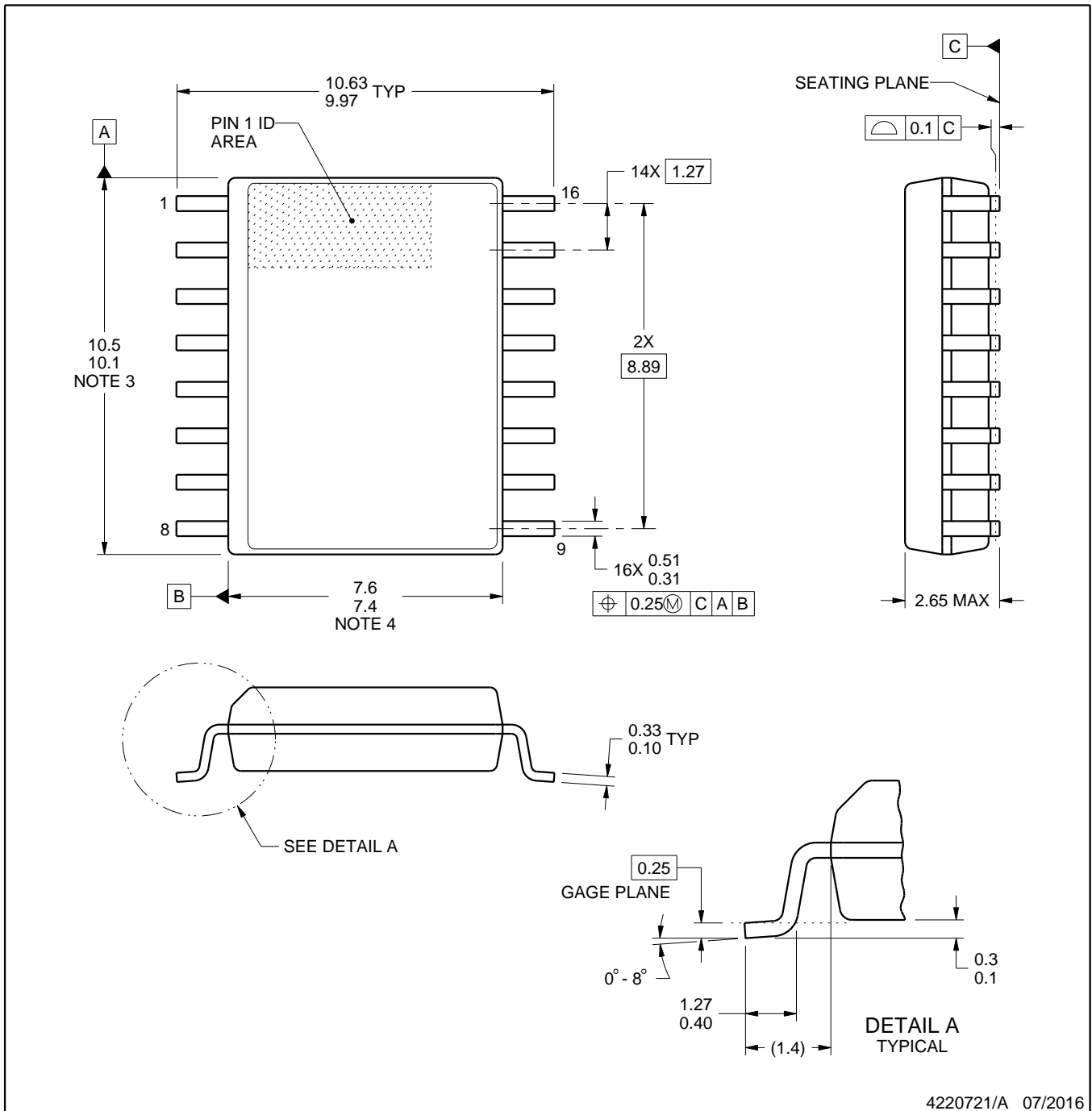


DW0016A

PACKAGE OUTLINE

SOIC - 2.65 mm max height

SOIC



4220721/A 07/2016

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.

EXAMPLE BOARD LAYOUT

DW0016A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE
SCALE:7X



SOLDER MASK DETAILS

4220721/A 07/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0016A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220721/A 07/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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