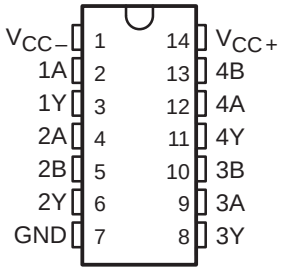
- **Bi-MOS Technology With TTL and CMOS Compatibility**
- **Meets or Exceeds the Requirements of ANSI EIA/TIA-232-E and ITU Recommendation V.28**
- **Very Low Quiescent Current . . . 95 μA Typ $V_{CC\pm}$ = ±12 V**
- **Current-Limited Outputs . . . 10 mA Typ**
- **CMOS-and TTL-Compatible Inputs**
- **On-Chip Slew Rate Limited to 30 V/μs max**
- **Flexible Supply Voltage Range**
- **Characterized at $V_{CC\pm}$ of ±4.5 V and ±15 V**
- **Functionally Interchangeable With Texas Instruments SN75188, Motorola MC1488, and National Semiconductor DS14C88**

D, DB†, OR N PACKAGE
(TOP VIEW)



† The DB package is only avalable left-end taped and reeled, i.e., order device SN75C188DBLE.

description

The SN75C188 is a monolithic, low-power, quadruple line driver that interfaces data terminal equipment with data communications equipment. This device is designed to conform to ANSI Standard EIA/TIA-232-E.

An external diode in series with each supply-voltage terminal is needed to protect the SN75C188 under certain fault conditions to comply with EIA/TIA-232-E.

The SN75C188 is characterized for operation from 0°C to 70°C.

Function Tables

DRIVER 1

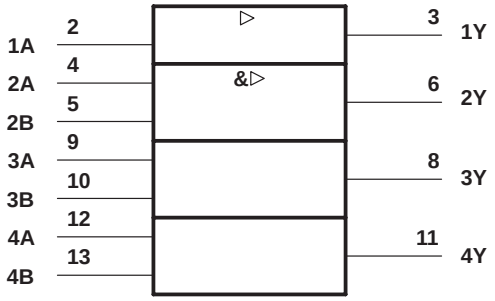
B	Y
H	L
L	H

DRIVERS 2 – 4

A	B	Y
H	H	L
L	X	H
X	L	H

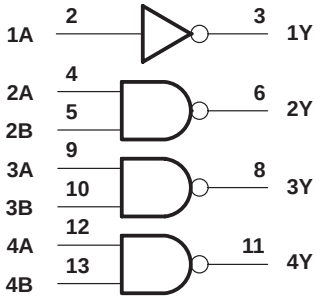
H = high level, L = low level,
X = don't care

logic symbol†



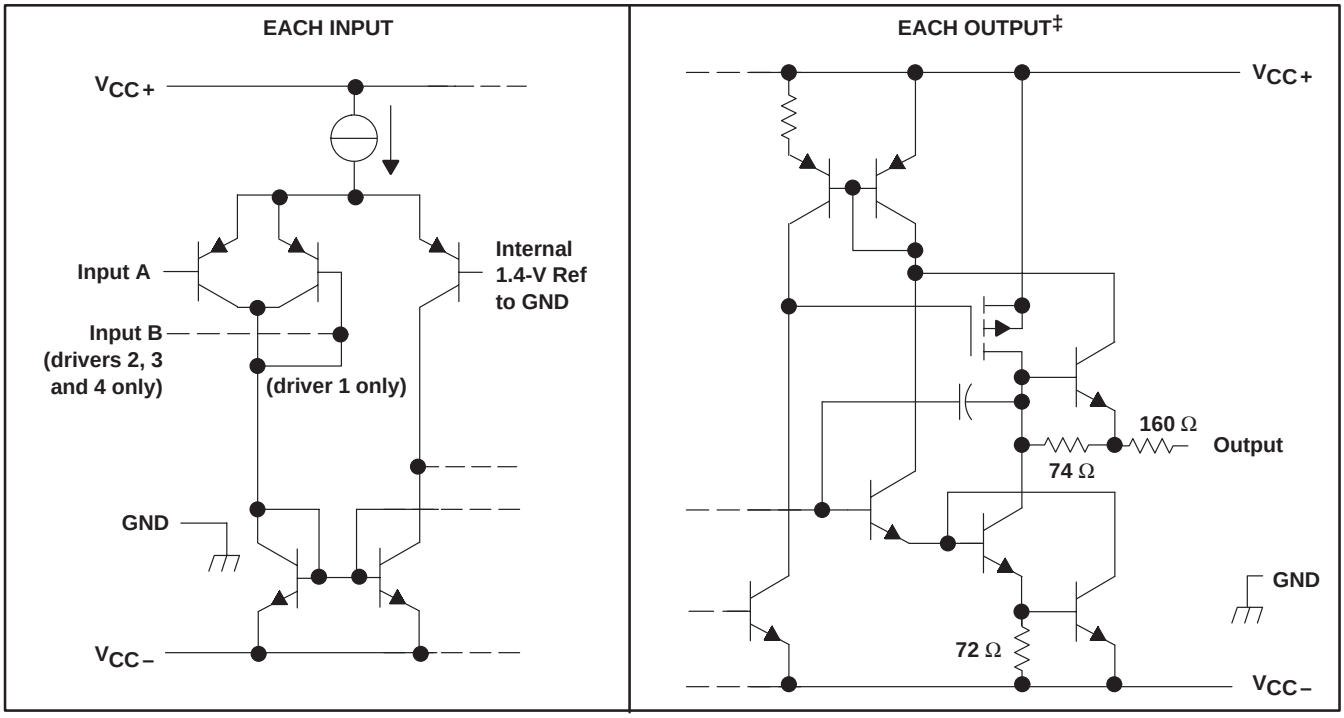
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



positive logic
$Y = \overline{A}$ (driver 1)
$Y = \overline{AB}$ or $\overline{A} + \overline{B}$ (drivers 2 through 4)

schematics of inputs and outputs



‡ All resistor values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC+} (see Note 1) . . . . . 15 V
Supply voltage, V_{CC-} (see Note 1) . . . . . –15 V
Input voltage range, V_I . . . . . V_{CC-} to V_{CC+}
Output voltage range, V_O . . . . . V_{CC-} –6 V to V_{CC+} +6 V
Continuous total power dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range, T_A . . . . . 0°C to 70°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to the network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW
DB	525 mW	4.2 mW/°C	336 mW
N	1150 mW	9.2 mW/°C	736 mW

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC+}	4.5	12	15	V
Supply voltage, V_{CC-}	–4.5	–12	–15	V
Input voltage, V_I	V_{CC-}+2		V_{CC+}	V
High-level Input voltage, V_{IH}	2			V
Low-level Input voltage, V_{IL}			0.8	V
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over operating free-air temperature range, V_{CC+} = 12 V, V_{CC-} = –12 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	V_{IL} = 0.8 V,	R_L = 3 kΩ	V_{CC+} = 5 V, V_{CC-} = –5 V	4			V
				V_{CC+} = 12 V, V_{CC-} = –12 V	10			
V_{OL}	Low-level output voltage (see Note 2)	V_{IH} = 2 V,	R_L = 3 kΩ	V_{CC+} = 5 V, V_{CC-} = –5 V			–4	V
				V_{CC+} = 12 V, V_{CC-} = –12 V			–10	
I_{IH}	High-level input current	V_I = 5 V					10	µA
I_{IL}	Low-level input current	V_I = 0					–10	µA
$I_{OS(H)}$	High-level short-circuit output current‡	V_I = 0.8 V,	V_O = 0 or V_{CC-}		–5.5	–10	–19.5	mA
$I_{OS(L)}$	Low-level short-circuit output current‡	V_I = 2 V,	V_O = 0 or V_{CC+}		5.5	10	19.5	mA
r_O	Output resistance, power off	V_{CC+} = 0,	V_{CC-} = 0,	V_I = –2 V to 2 V	300			Ω
I_{CC+}	Supply current from V_{CC+}	V_{CC+} = 5 V, No load	V_{CC-} = – 5 V,	All inputs at 2 V or 0.8 V		90	160	µA
		V_{CC+} = 12 V, No load	V_{CC-} = –12 V,	All inputs at 2 V or 0.8 V		95	160	
I_{CC-}	Supply current from V_{CC-}	V_{CC+} = 5 V, No load	V_{CC-} = – 5 V,	All inputs at 2 V or 0.8 V		–90	–160	µA
		V_{CC+} = 12 V, No load	V_{CC-} = –12	All inputs at 2 V or 0.8 V		–95	–160	

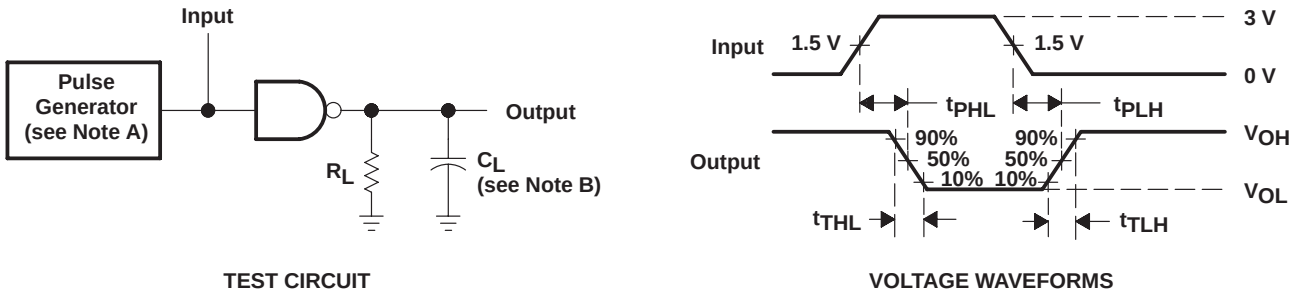
† All typical values are at T_A = 25°C.
‡ Not more than one output should be shorted at a time.
NOTE 2: The algebraic convention, in which the more positive (less negative) limit is designated as maximum, is used in this data sheet for logic levels only; e.g., if –4 V is a maximum, the typical value is a more negative voltage.

switching characteristics, V_{CC+} = 12 V, V_{CC-} = –12 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output§	R_L = 3 kΩ, See Figure 1	C_L = 15 pF,			3	µs
t_{PHL}	Propagation delay time, high- to low-level output§					3.5	µs
t_{TLH}	Transition time, low- to high-level output¶			0.53		3.2	µs
t_{THL}	Transition time, high- to low-level output¶			0.53		3.2	µs
t_{TLH}	Transition time, low- to high-level output#	R_L = 3 kΩ to 7 kΩ, See Figure 1	C_L = 2500 pF,		1.5		µs
t_{THL}	Transition time, high- to low-level output#				1.5		µs
SR	Output slew rate§	R_L = 3 kΩ to 7 kΩ,	C_L = 15 pF	6	15	30	V/µs

§ Measured at the 50% level
¶ Measured between the 10% and 90% points on the output waveform
# Measured between the 3-V and –3-V points on the output waveform (EIA/TIA-232-E conditions), all unused inputs tied either high or low

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT **VOLTAGE WAVEFORMS**

NOTES: A. The pulse generator has the following characteristics: t_W = 25 µs, PRR = 20 kHZ, Z_O = 50 Ω, $t_r = t_f \leq 50$ ns.
B. C_L includes probe and jig capacitance.

Figure 1. Test Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

VOLTAGE TRANSFER CHARACTERISTICS

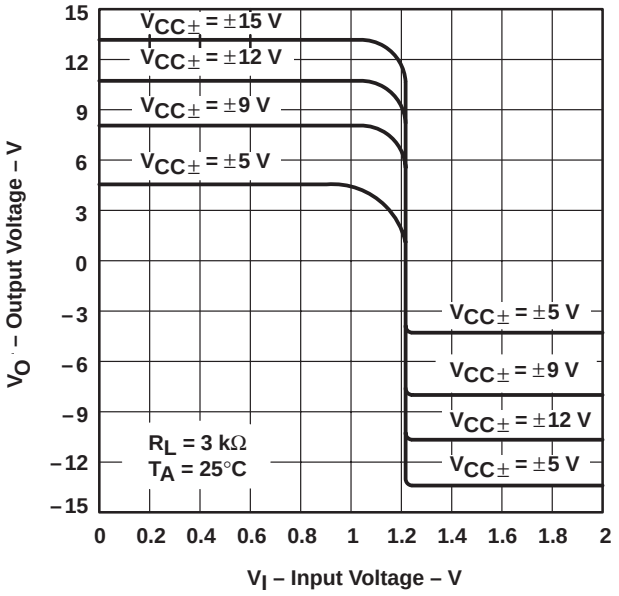


Figure 2

OUTPUT CURRENT
vs
OUTPUT VOLTAGE

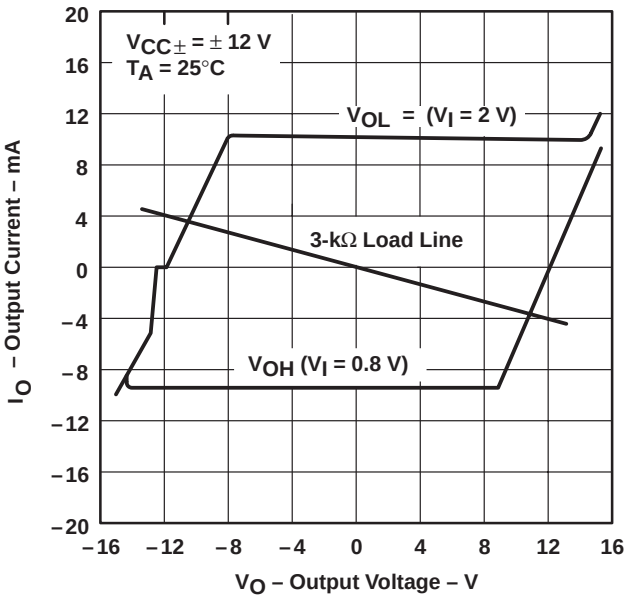


Figure 3

SHORT-CIRCUIT OUTPUT CURRENT
vs
FREE-AIR TEMPERATURE

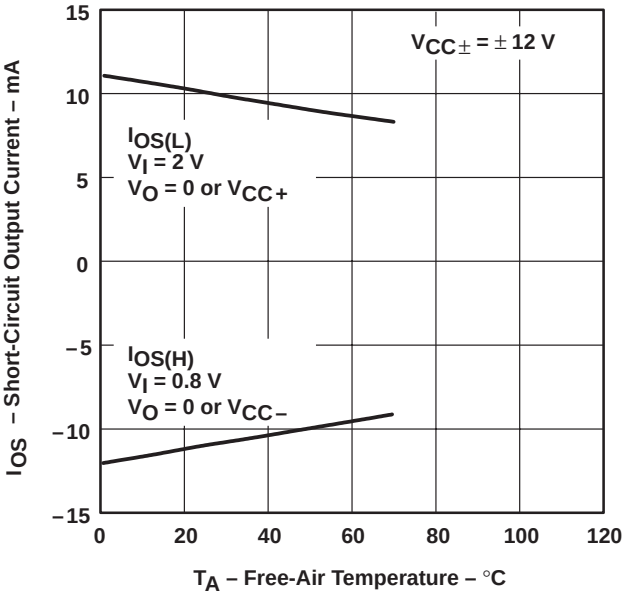


Figure 4

OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

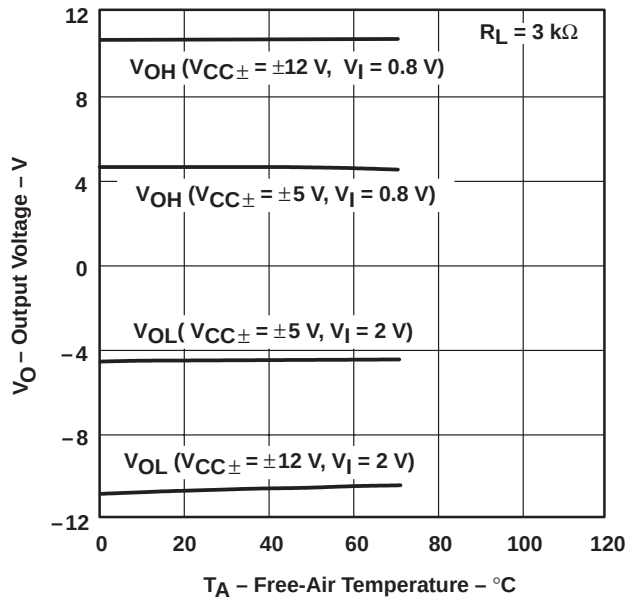


Figure 5

TYPICAL CHARACTERISTICS

INPUT CURRENT vs FREE-AIR TEMPERATURE

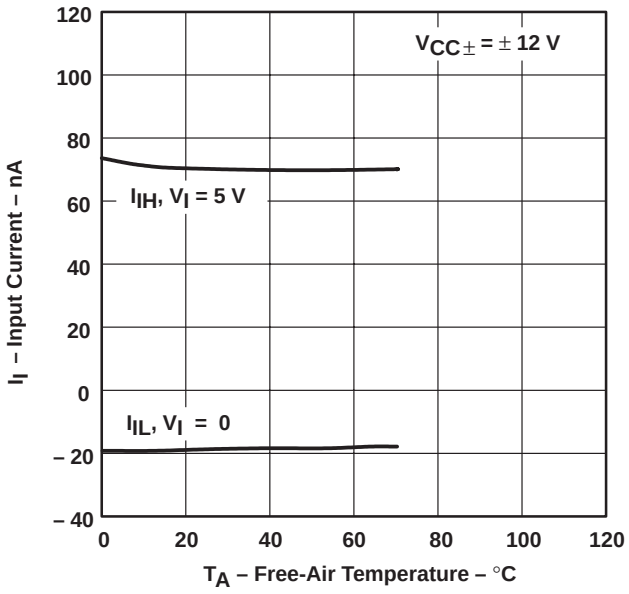


Figure 6

POWER-OFF OUTPUT RESISTANCE vs FREE-AIR TEMPERATURE

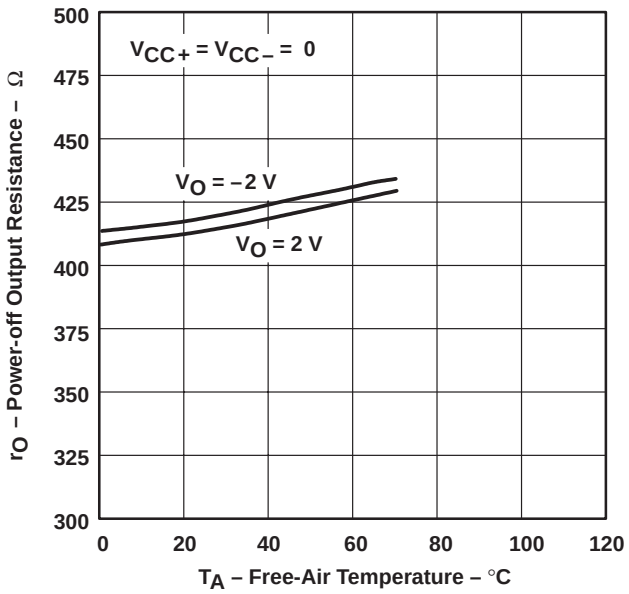


Figure 7

SUPPLY CURRENT vs FREE-AIR TEMPERATURE

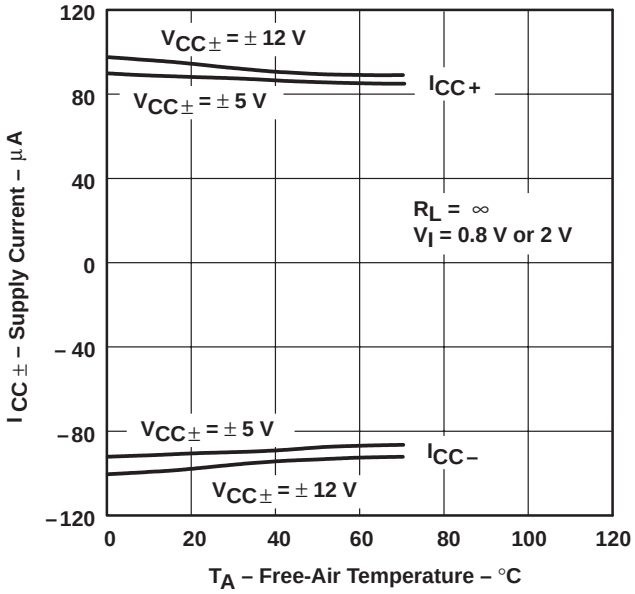


Figure 8

OUTPUT SLEW RATE vs FREE-AIR TEMPERATURE

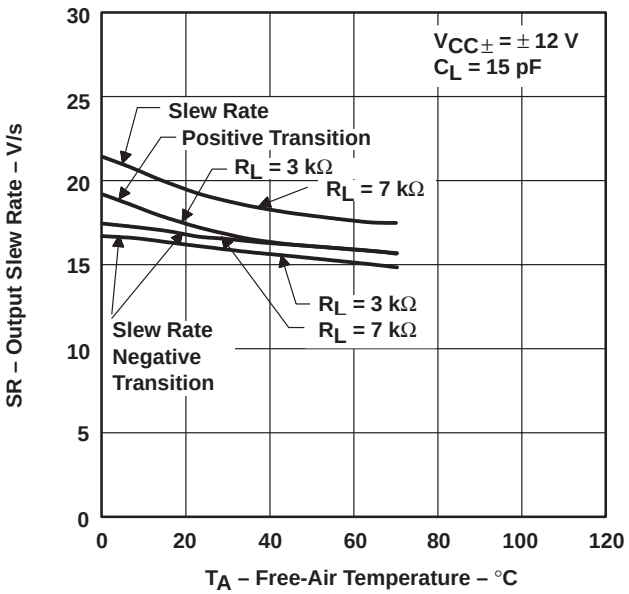


Figure 9

TYPICAL CHARACTERISTICS

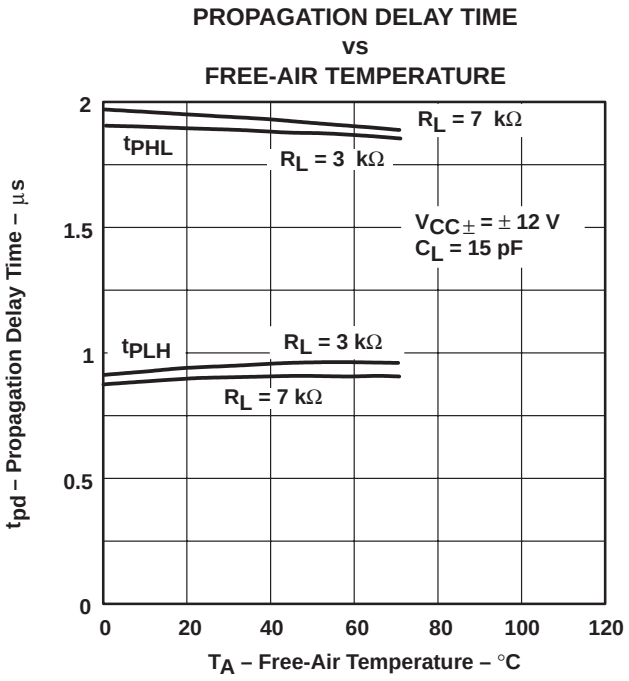


Figure 10

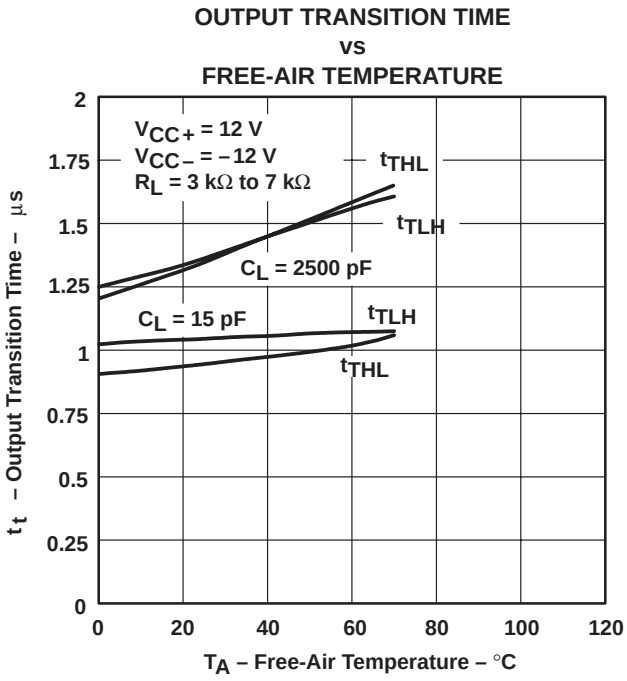


Figure 11

APPLICATION INFORMATION

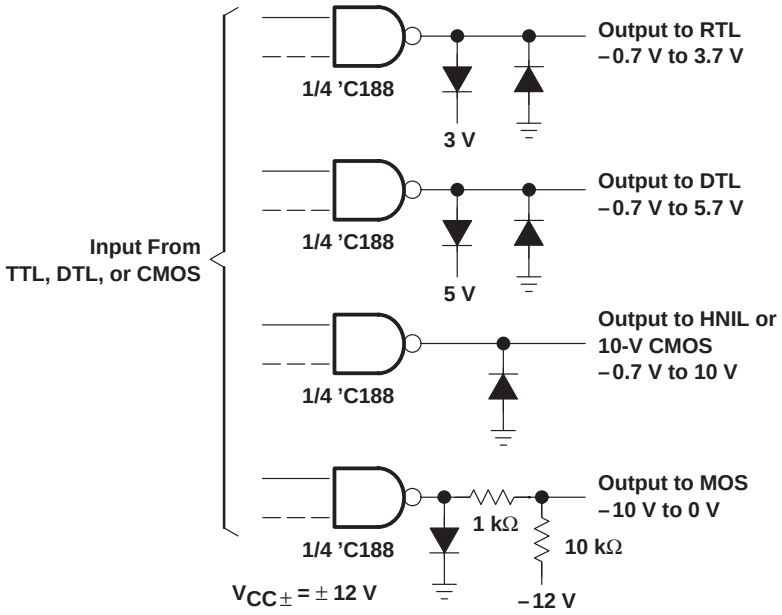
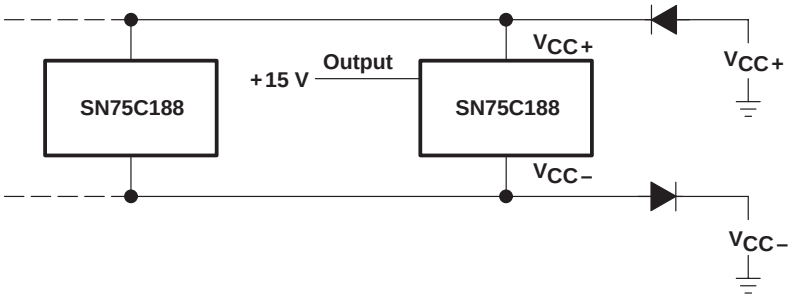


Figure 12. Logic Translator Applications

APPLICATION INFORMATION



NOTE A: External diodes placed in series with the V_{CC+} and V_{CC-} leads protect the SN75C188 in the fault condition where the device outputs are shorted to ±15 V and the power supplies are at low voltage and provide low-impedance paths to GND.

Figure 13. Power Supply Protection to Meet Power-Off Fault Conditions of Standard EIA/TIA-232-E

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN75C188D	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75C188	Samples
SN75C188DBR	ACTIVE	SSOP	DB	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	CA188	Samples
SN75C188DE4	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75C188	Samples
SN75C188DR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75C188	Samples
SN75C188DRE4	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75C188	Samples
SN75C188N	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	SN75C188N	Samples
SN75C188NSR	ACTIVE	SOP	NS	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	75C188	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

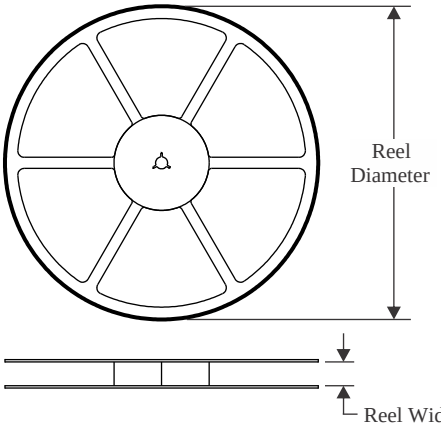
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

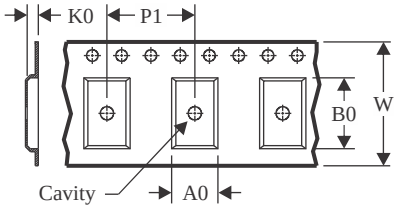
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

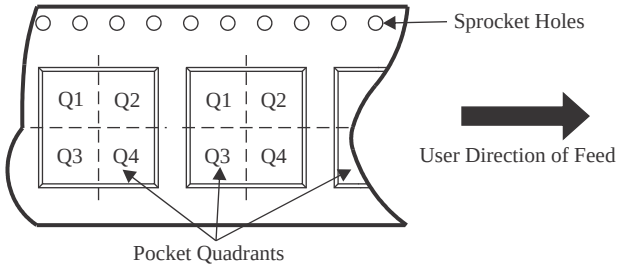


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

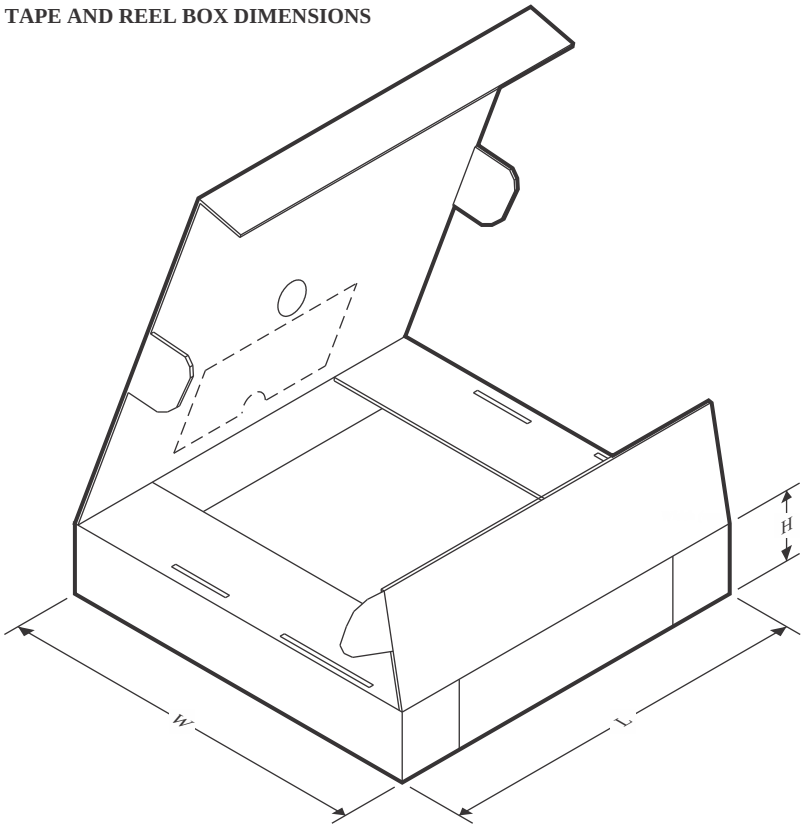
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN75C188DBR	SSOP	DB	14	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
SN75C188DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN75C188NSR	SOP	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1

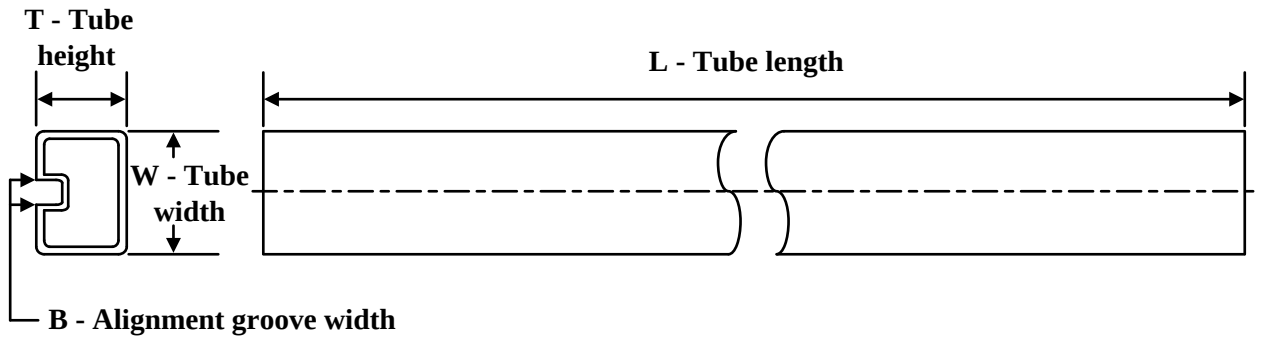
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

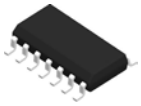
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN75C188DBR	SSOP	DB	14	2000	356.0	356.0	35.0
SN75C188DR	SOIC	D	14	2500	353.0	353.0	32.0
SN75C188NSR	SOP	NS	14	2000	356.0	356.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN75C188D	D	SOIC	14	50	507	8	3940	4.32
SN75C188D	D	SOIC	14	50	506.6	8	3940	4.32
SN75C188DE4	D	SOIC	14	50	506.6	8	3940	4.32
SN75C188DE4	D	SOIC	14	50	507	8	3940	4.32
SN75C188N	N	PDIP	14	25	506	13.97	11230	4.32

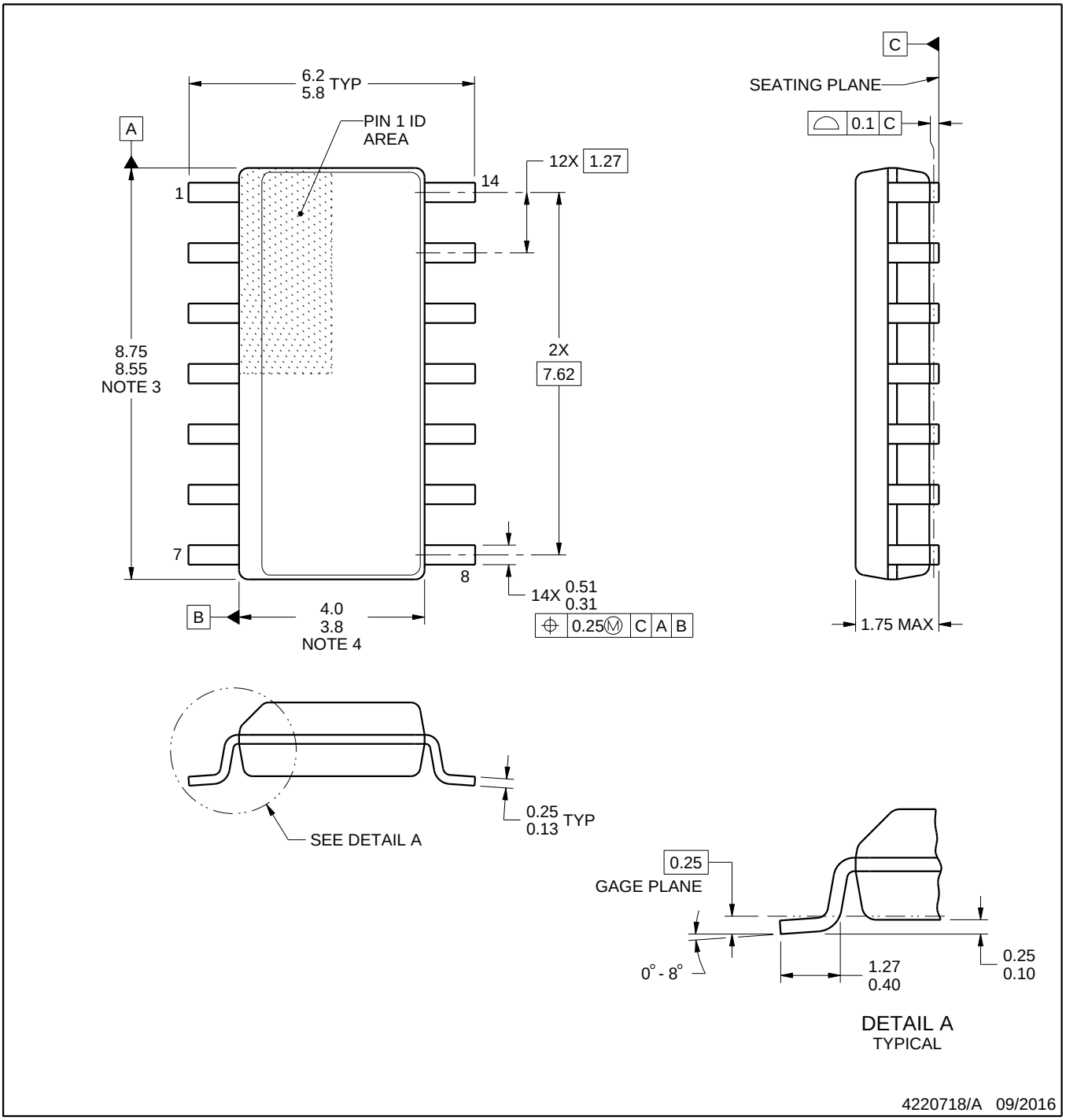


PACKAGE OUTLINE

D0014A

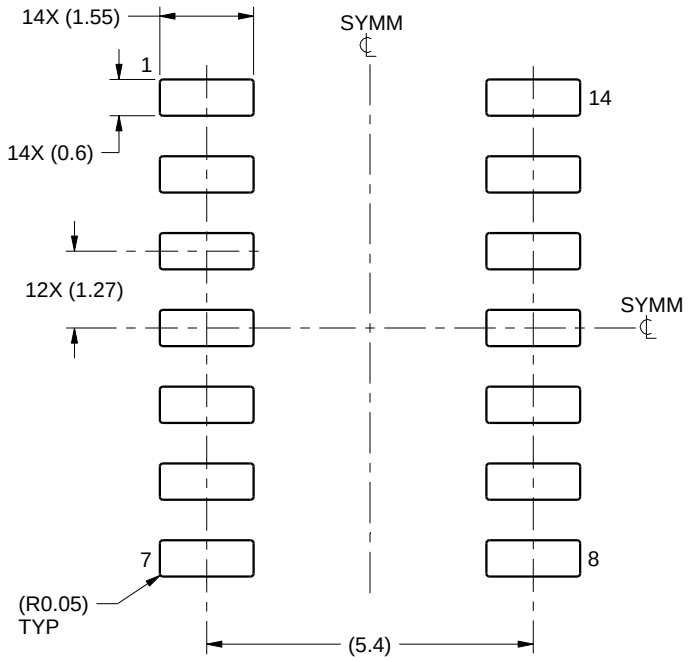
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

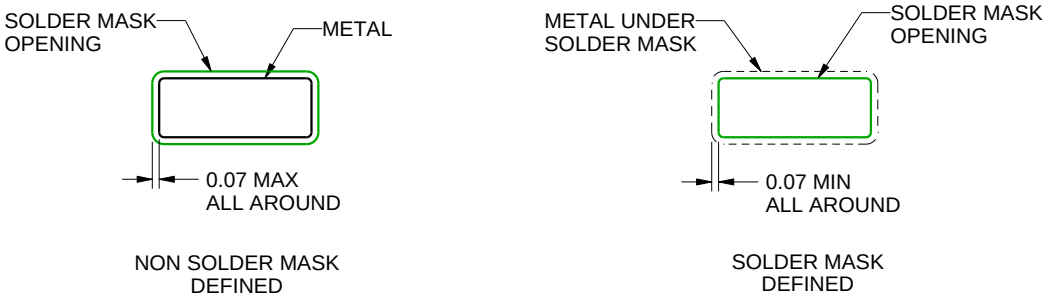


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

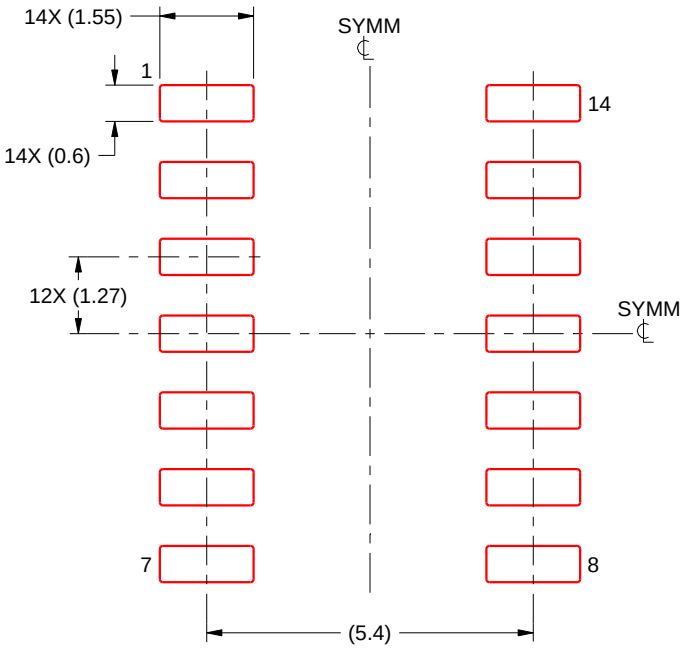
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

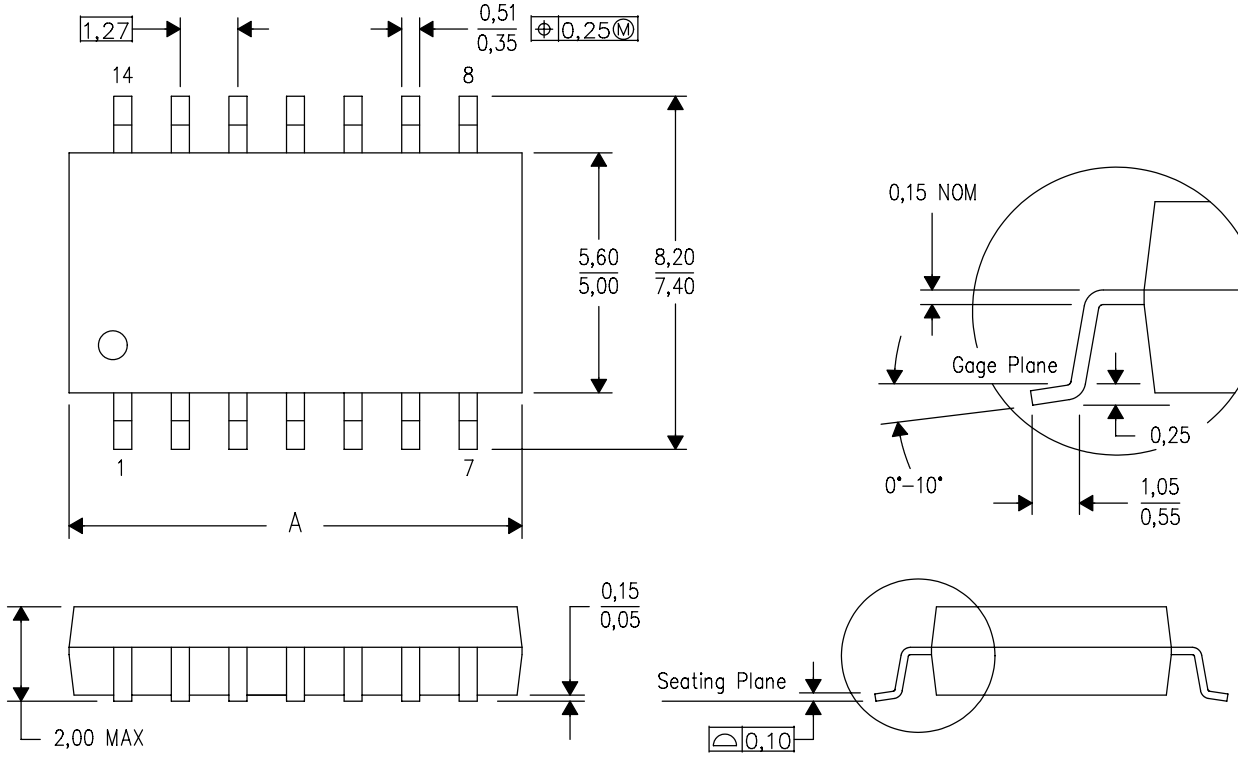
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

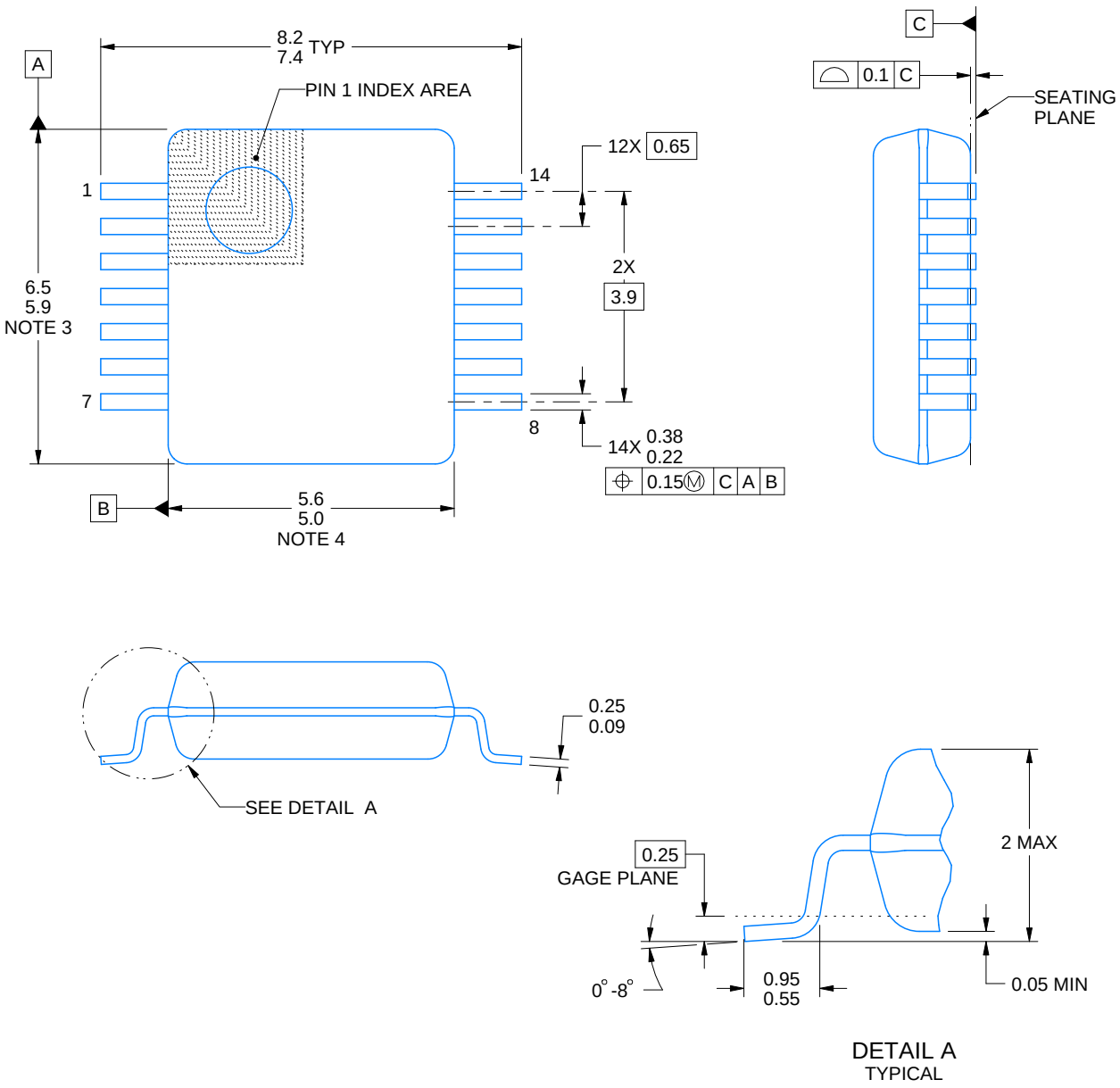
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

PACKAGE OUTLINE

DB0014A

SSOP - 2 mm max height

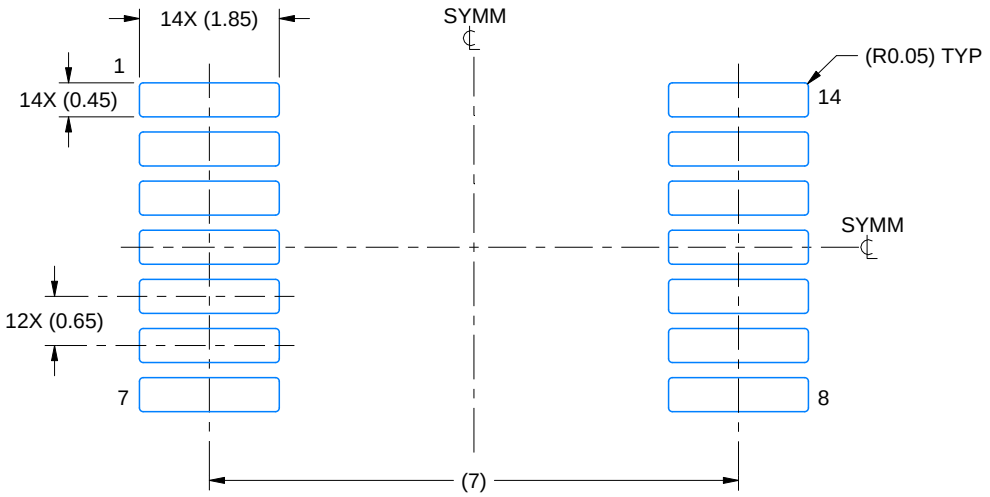
SMALL OUTLINE PACKAGE



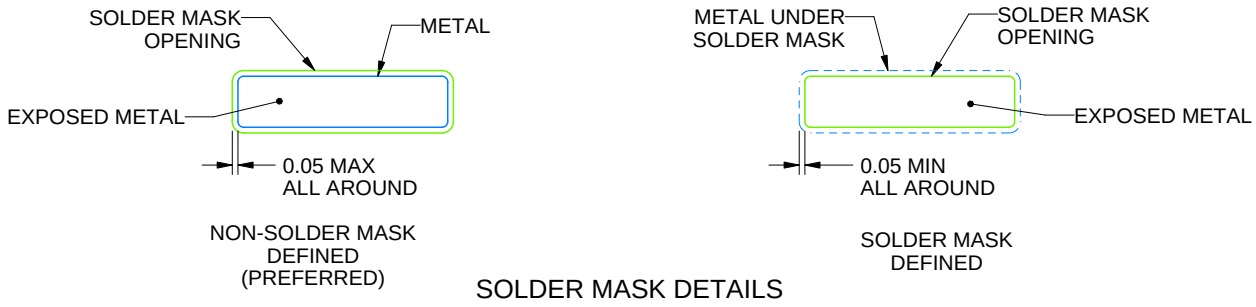
4220762/A 05/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-150.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

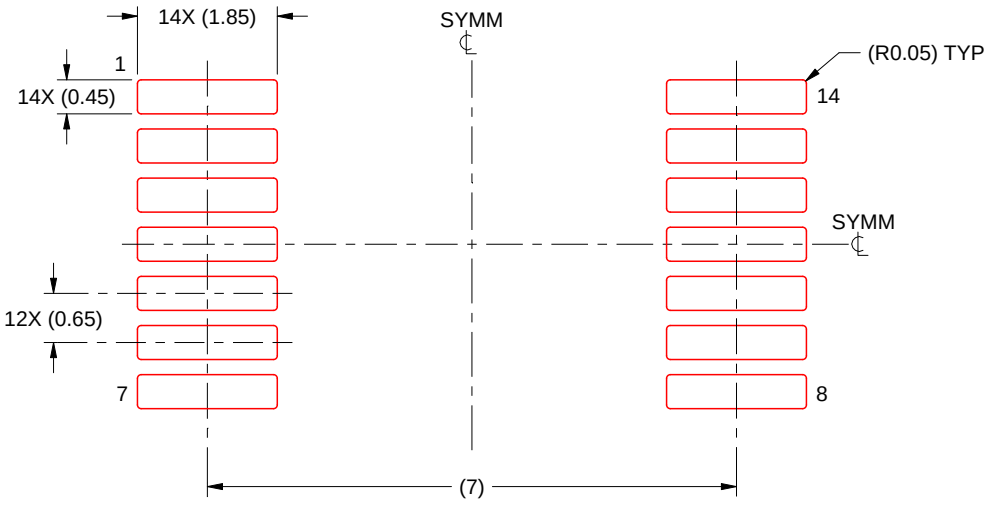


SOLDER MASK DETAILS

4220762/A 05/2024

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220762/A 05/2024

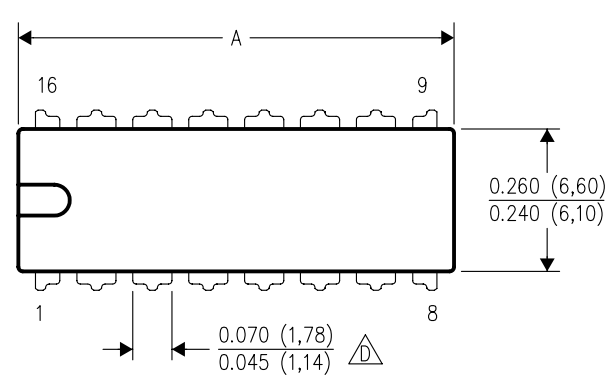
NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

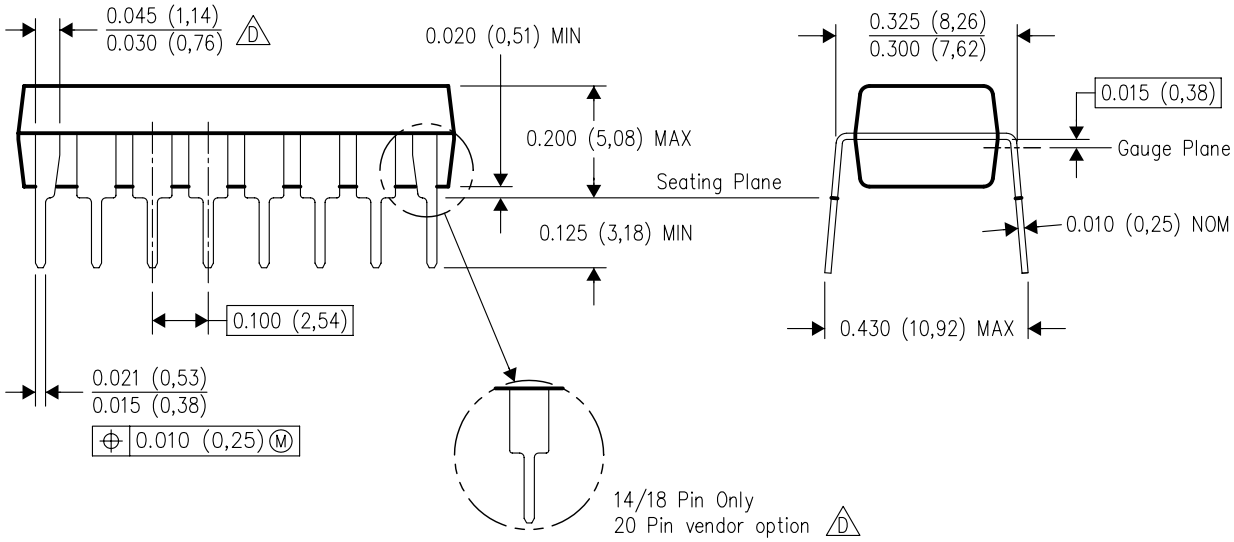
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

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