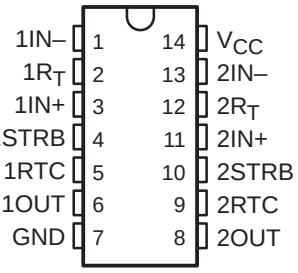
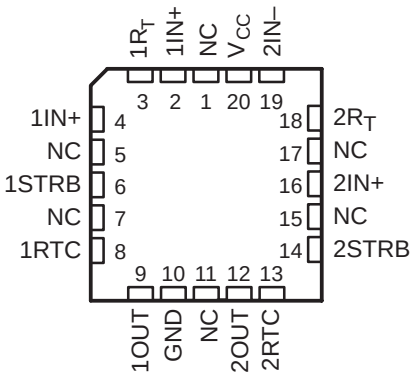
SLLS092D – OCTOBER 1972 – REVISED APRIL 1998

- **Single 5-V Supply**
- **Differential Line Operation**
- **Dual Channels**
- **TTL Compatibility**
- **±15-V Common-Mode Input Voltage Range**
- **±15-V Differential Input Voltage Range**
- **Individual Channel Strobes**
- **Built-In Optional Line-Termination Resistor**
- **Individual Frequency Response Controls**
- **Designed for Use With Dual Differential Drivers SN55183 and SN75183**
- **Designed to Be Interchangeable With National Semiconductor DS7820A and DS8820A**

SN55182 . . . J OR W PACKAGE
SN75182 . . . N PACKAGE
(TOP VIEW)



SN55182 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

THE SN55182 IS NOT RECOMMENDED FOR NEW DESIGNS

description

The SN55182 and SN75182 dual differential line receivers are designed to sense small differential signals in the presence of large common-mode noise. These devices give TTL-compatible output signals as a function of the polarity of the differential input voltage. The frequency response of each channel can be easily controlled by a single external capacitor to provide immunity to differential noise spikes. The output goes to a high level when the inputs are open circuited. A strobe input (STRB) is provided that, when in the low level, disables the receiver and forces the output to a high level.

The receiver is of monolithic single-chip construction, and both halves of the dual circuits use common power-supply and ground terminals.

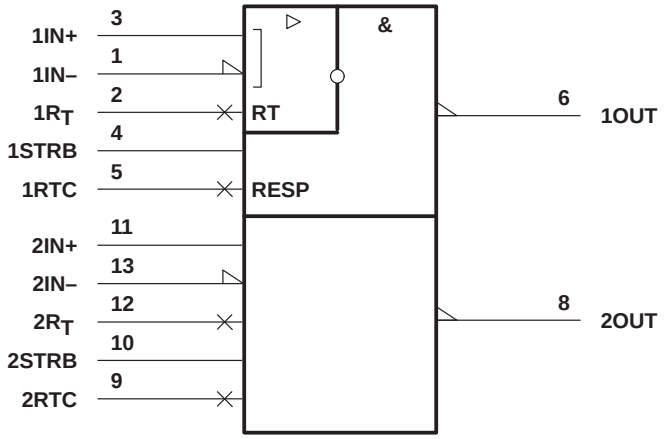
The SN55182 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN75182 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

INPUTS		OUTPUT OUT
STRB	V_{ID}	
L	X	H
H	H	H
H	L	L

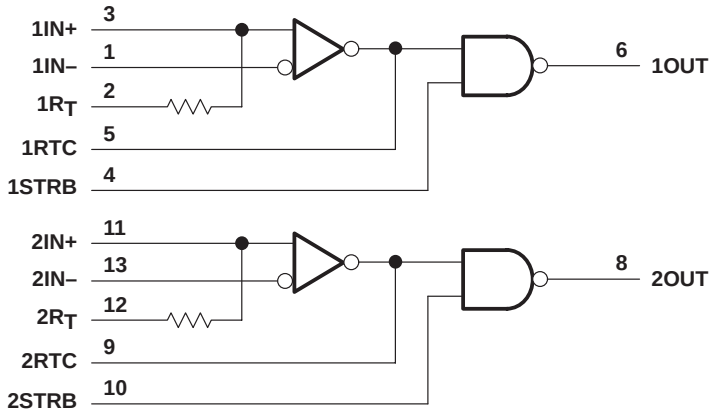
H = $V_I \geq V_{IH}$ min or V_{ID} more positive than V_{TH} max
L = $V_I \leq V_{IL}$ max or V_{ID} more negative than V_{TL} max
X = irrelevant

logic symbol†



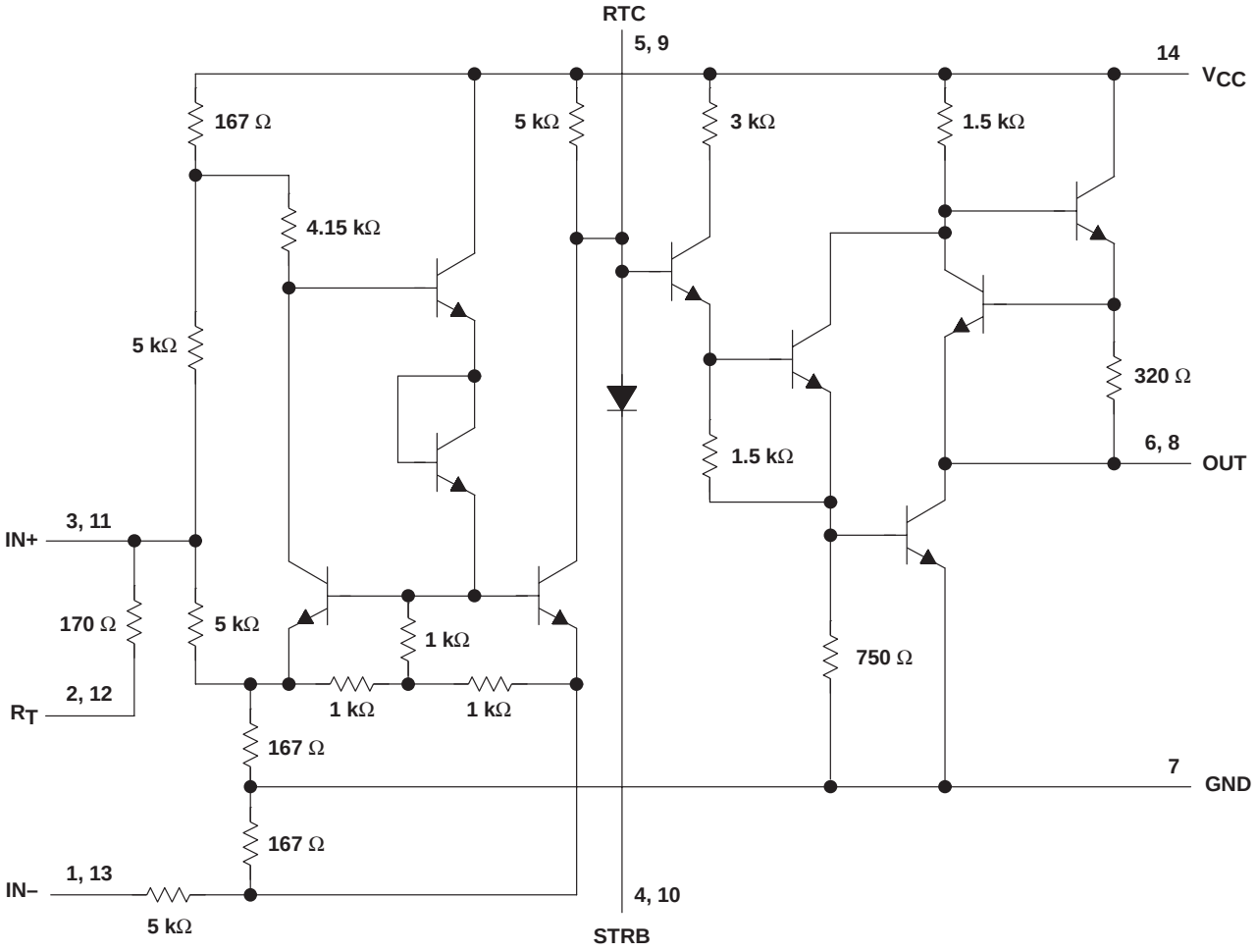
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the J, N, and W packages.

logic diagram (positive logic)



Pin numbers shown are for the J, N, and W packages.

schematic (each receiver)



Resistor values shown are nominal.
Pin numbers shown are for the J, N, and W packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1) . . . . . 8 V
Common-mode input voltage, V_{IC} . . . . . ±20 V
Differential input voltage, V_{ID} (see Note 2) . . . . . ±20 V
Strobe input voltage, $V_{I(STRB)}$ . . . . . 8 V
Output sink current . . . . . 50 mA
Continuous total power dissipation . . . . . See Dissipation Rating Table
Storage temperature range, T_{stg} . . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: N package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J or W package . . . . . 300°C
Case temperature for 60 seconds, T_c: FK package . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential voltages, are with respect to network ground terminal.
2. Differential voltage values are at the noninverting terminal with respect to the inverting terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 125°C$ POWER RATING
FK‡	1375 mW	11.0 mW/°C	880 mW	275 mW
J‡	1375 mW	11.0 mW/°C	880 mW	275 mW
N	1150 mW	9.2 mW/°C	736 mW	–
W‡	1000 mW	8.0 mW/°C	640 mW	200 mW

‡ In the FK, J, and W packages, SN55182 chips are alloy mounted.

recommended operating conditions

	SN55182			SN75182			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.5	5	5.5	V
Common-mode input voltage, V_{IC}			±15			±15	V
High-level strobe input voltage, $V_{IH(STRB)}$	2.1		5.5	2.1		5.5	V
Low-level strobe input voltage, $V_{IL(STRB)}$	0		0.9	0		0.9	V
High-level output current, I_{OH}			–400			–400	µA
Low-level output current, I_{OL}			16			16	mA
Operating free-air temperature, T_A	–55		125	0		70	°C

electrical characteristics over recommended ranges of V_{CC}, V_{IC}, and operating free-air temperature (unless otherwise noted)

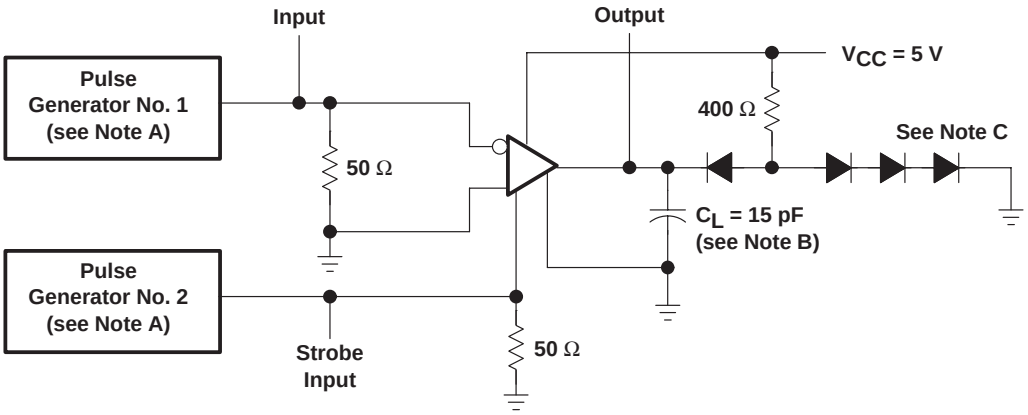
PARAMETER			TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage		V_O = 2.5 V, I_{OH} = –400 µA	V_{IC} = –3 V to 3 V			0.5	V
				V_{IC} = –15 V to 15 V			1	
$V_{IT–}$	Negative-going input threshold voltage		V_O = 0.4 V, I_{OL} = 16 mA	V_{IC} = –3 V to 3 V			–0.5	V
				V_{IC} = –15 V to 15 V			–1	
V_{OH}	High-level output voltage		V_{ID} = 1 V, $V_{(STRB)}$ = 2.1 V, I_{OH} = –400 µA		2.5	4.2	5.5	V
			V_{ID} = –1 V, $V_{(STRB)}$ = 0.4 V, I_{OH} = –400 µA		2.5	4.2	5.5	
V_{OL}	Low-level output voltage		V_{ID} = –1 V, $V_{(STRB)}$ = 2.1 V, I_{OL} = 16 mA			0.25	0.4	V
I_I	Input current	Inverting input	V_{IC} = 15 V			3	4.2	mA
			V_{IC} = 0			0	–0.5	
			V_{IC} = –15 V			–3	–4.2	
		Noninverting input	V_{IC} = 15 V			5	7	
			V_{IC} = 0			–1	–1.4	
			V_{IC} = –15 V			–7	–9.8	
$I_{IH(STRB)}$	High-level strobe input current		$V_{(STRB)}$ = 5.5 V				5	µA
$I_{IL(STRB)}$	Low-level strobe input current		$V_{(STRB)}$ = 0			–1	–1.4	mA
r_i	Input resistance	Inverting input			3.6	5		kΩ
		Noninverting input			1.8	2.5		
	Line-terminating resistance		T_A = 25°C		120	170	250	Ω
I_{OS}	Short-circuit output current		V_{CC} = 5.5 V,	V_O = 0	–2.8	–4.5	–6.7	mA
I_{CC}	Supply current (average per receiver)		V_{IC} = 15 V,	V_{ID} = –1 V		4.2	6	mA
			V_{IC} = 0,	V_{ID} = –0.5 V		6.8	10.2	
			V_{IC} = –15 V,	V_{ID} = –1 V		9.4	14	

† Unless otherwise noted, $V_{(STRB)} \geq 2.1$ V or open.
‡ All typical values are at V_{CC} = 5 V, V_{IC} = 0, and T_A = 25°C.

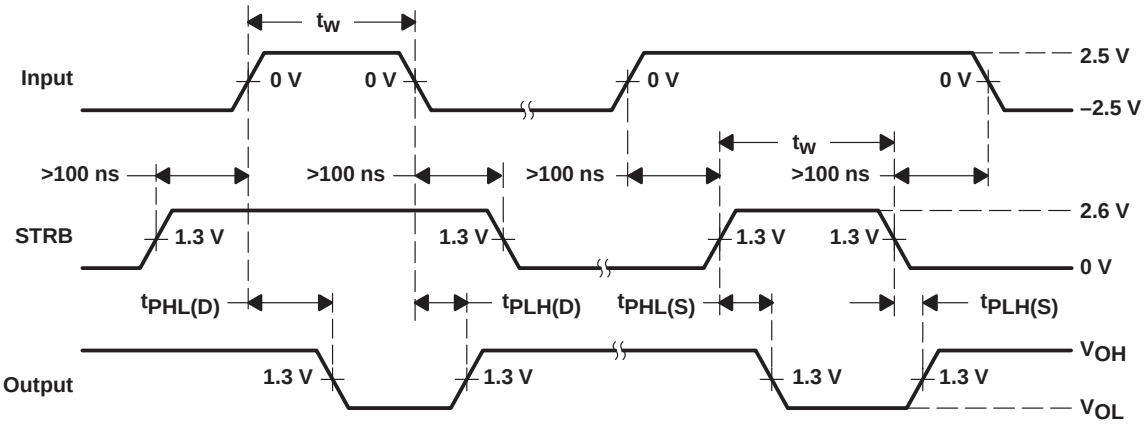
switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{PLH(D)}$	Propagation delay time, low- to high-level output from differential input	R_L = 400 Ω, C_L = 15 pF, see Figure 1		18	40	ns
$t_{PHL(D)}$	Propagation delay time, high- to low-level output from differential input	R_L = 400 Ω, C_L = 15 pF, see Figure 1		31	45	ns
$t_{PLH(S)}$	Propagation delay time, low- to high-level output from STRB input	R_L = 400 Ω, C_L = 15 pF, see Figure 1		9	30	ns
$t_{PHL(S)}$	Propagation delay time, high- to low-level output from STRB input	R_L = 400 Ω, C_L = 15 pF, see Figure 1		15	25	ns

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generators have the following characteristics: Z_O = 50 Ω, $t_r \le 10$ ns, $t_f \le 10$ ns, t_w = 0.5 ±0.1 µs, PRR ≤ 1 MHz.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N3064 or equivalent.

Figure 1. Test Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS†

DIFFERENTIAL INPUT THRESHOLD VOLTAGE vs SUPPLY VOLTAGE

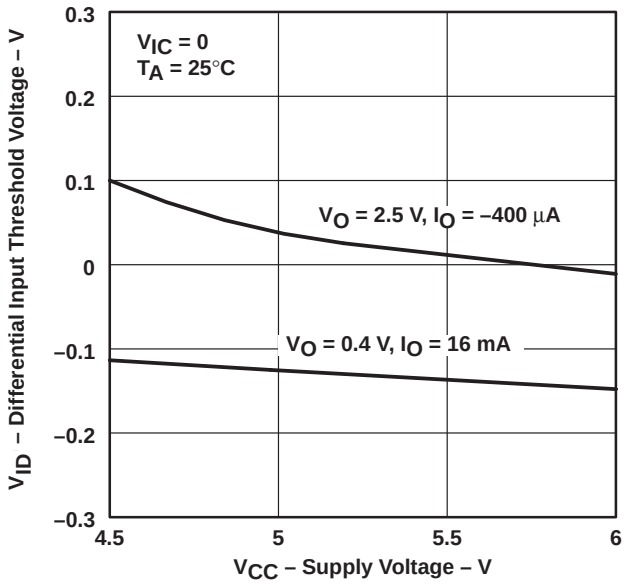


Figure 2

DIFFERENTIAL INPUT THRESHOLD VOLTAGE vs COMMON-MODE INPUT VOLTAGE

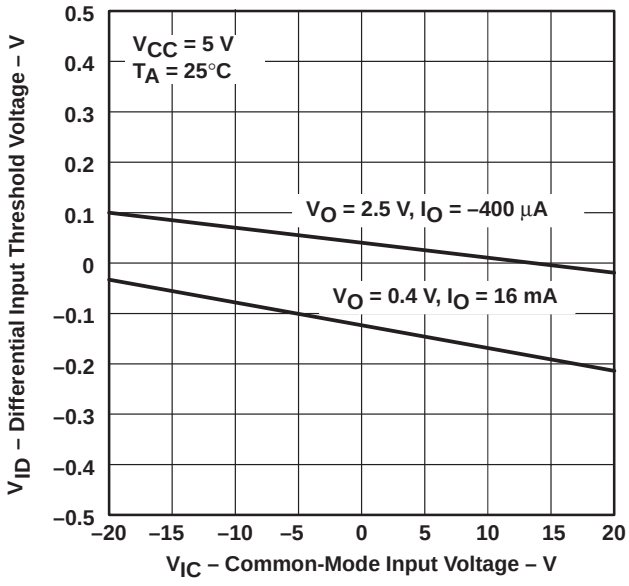


Figure 3

DIFFERENTIAL INPUT THRESHOLD VOLTAGE vs FREE-AIR TEMPERATURE

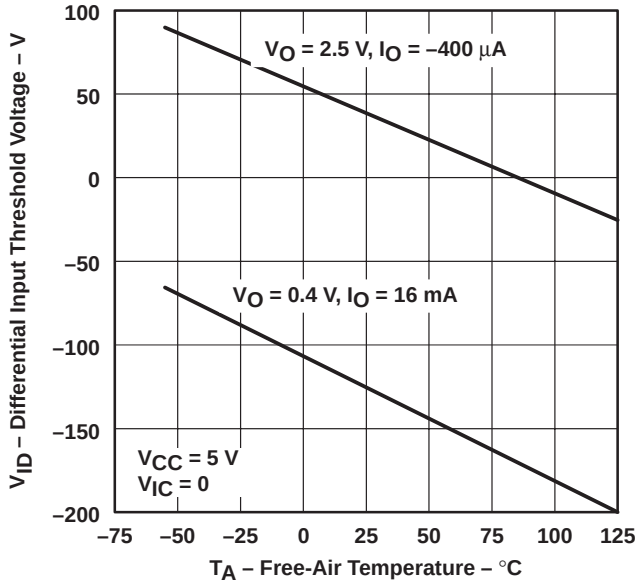


Figure 4

† Operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied.

TYPICAL CHARACTERISTICS†

OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE

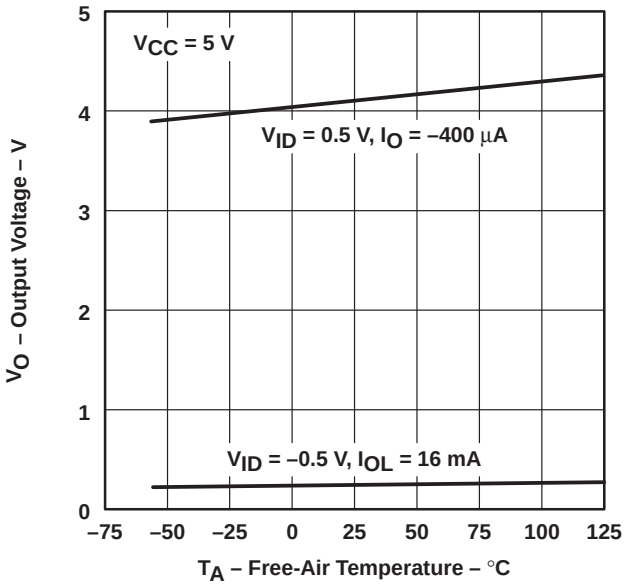


Figure 5

VOLTAGE TRANSFER CHARACTERISTICS

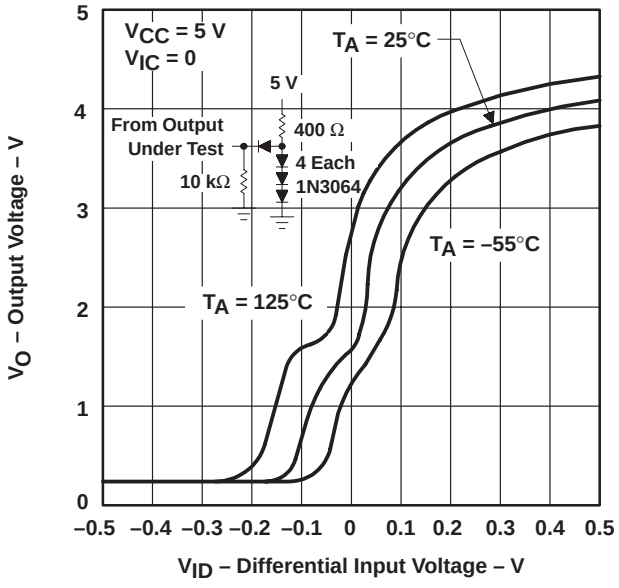


Figure 6

INPUT CURRENT vs INPUT VOLTAGE

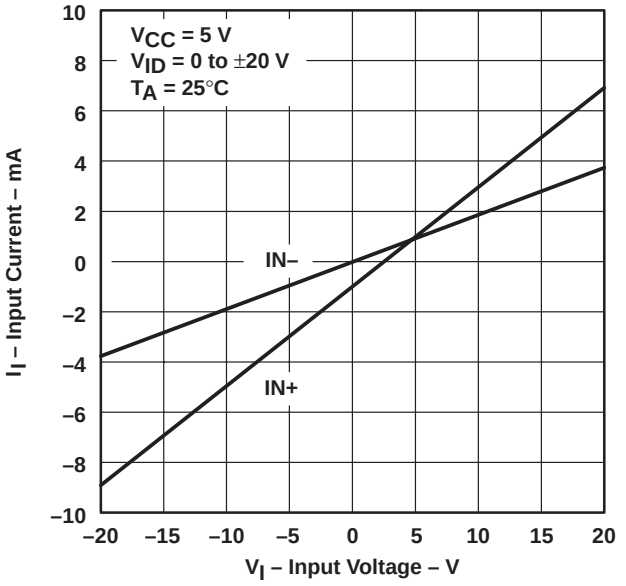


Figure 7

TERMINATING RESISTANCE vs FREE-AIR TEMPERATURE

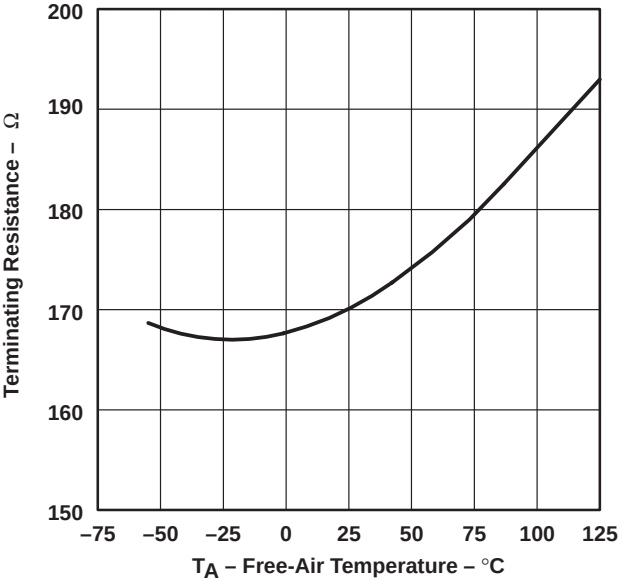


Figure 8

† Operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied.

TYPICAL CHARACTERISTICS†

**SUPPLY CURRENT
(AVERAGE PER RECEIVER)
vs
COMMON-MODE INPUT VOLTAGE**

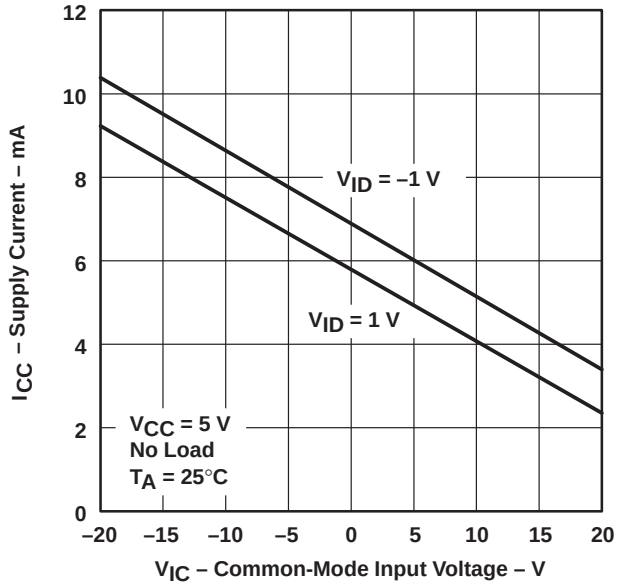


Figure 9

**POWER DISSIPATION
(AVERAGE PER RECEIVER)
vs
COMMON-MODE INPUT VOLTAGE**

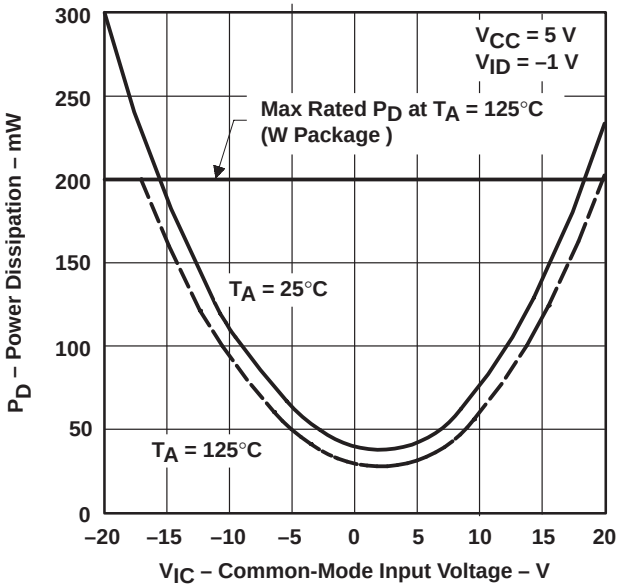
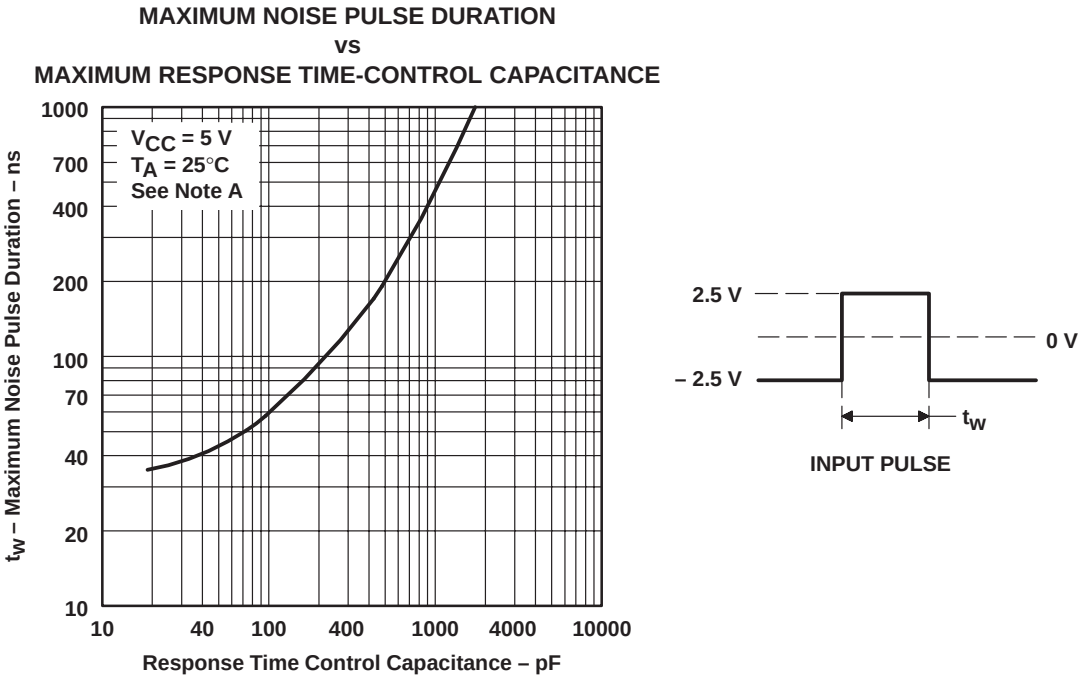


Figure 10

† Operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied.

TYPICAL CHARACTERISTICS†



NOTE A: Figure 11 shows the maximum duration of the illustrated pulse that can be applied differently without the output changing from the low to high level.

Figure 11

† Operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied.

TYPICAL CHARACTERISTICS†

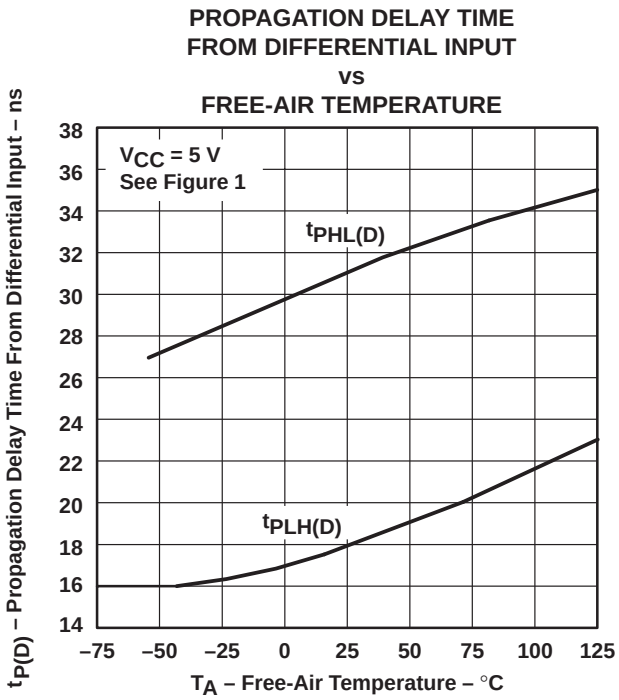


Figure 12

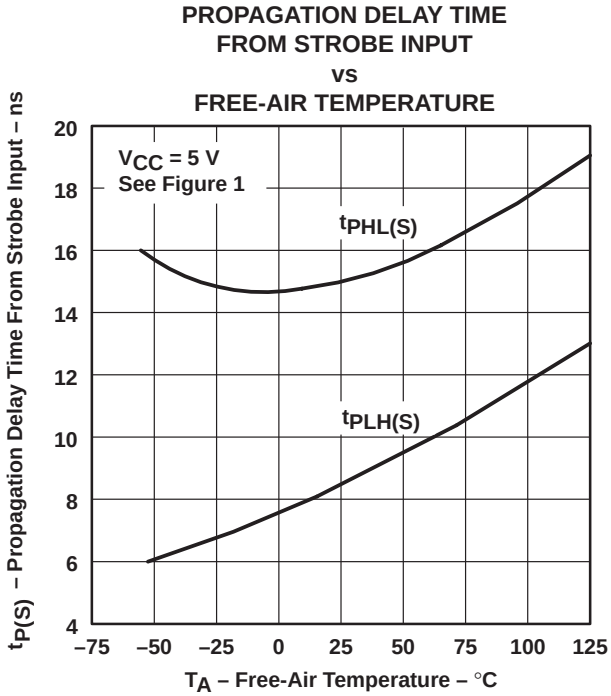
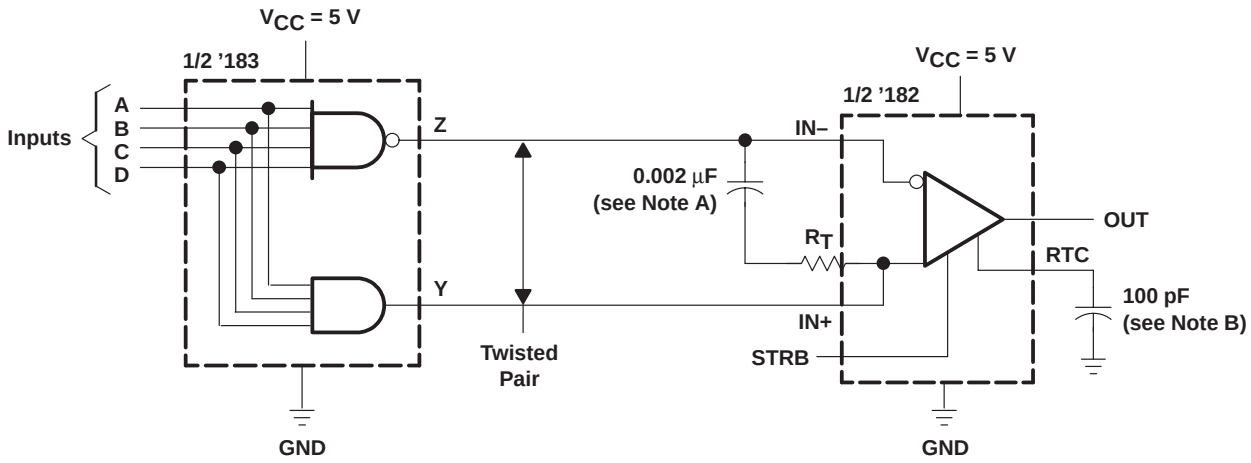


Figure 13

† Operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied.

APPLICATION INFORMATION



NOTES: A. When the inputs are open circuited, the output is high. A capacitor may be used for dc isolation of the line-terminating resistor. At the frequency of operation, the impedance of the capacitor should be relatively small.

Example: let f = 5 MHz
C = 0.002 μF

$$Z_{(C)} = \frac{1}{2\pi fC} = \frac{1}{2\pi(5 \times 10^{6})(0.002 \times 10^{-6})}$$

$$Z_{(C)} \approx 16\Omega$$

B. Use of a capacitor to control response time is optional.

Figure 14. Transmission of Digital Data Over Twisted-Pair Line

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-7900801VCA	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-7900801VCA SNV55182J	Samples
5962-7900801VDA	ACTIVE	CFP	W	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-7900801VDA SNV55182W	Samples
SN75182D	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75182	Samples
SN75182DR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75182	Samples
SN75182N	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	SN75182N	Samples
SN75182NSR	ACTIVE	SOP	NS	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75182	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

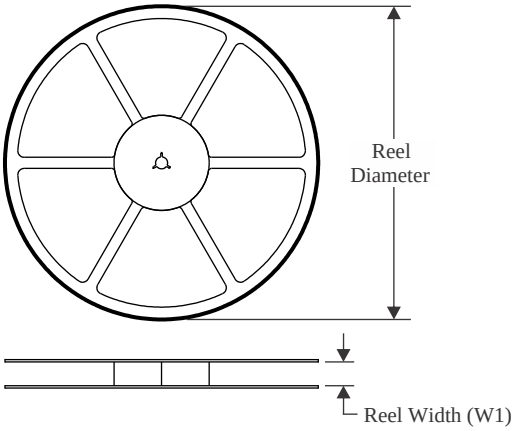
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

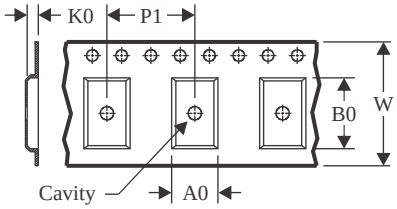
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

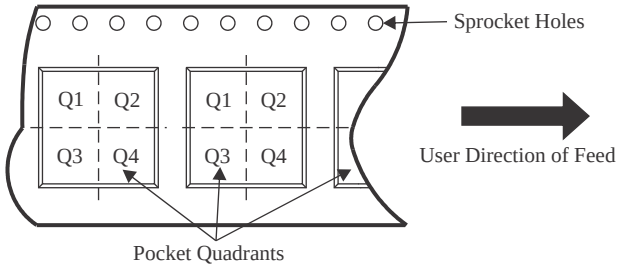


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

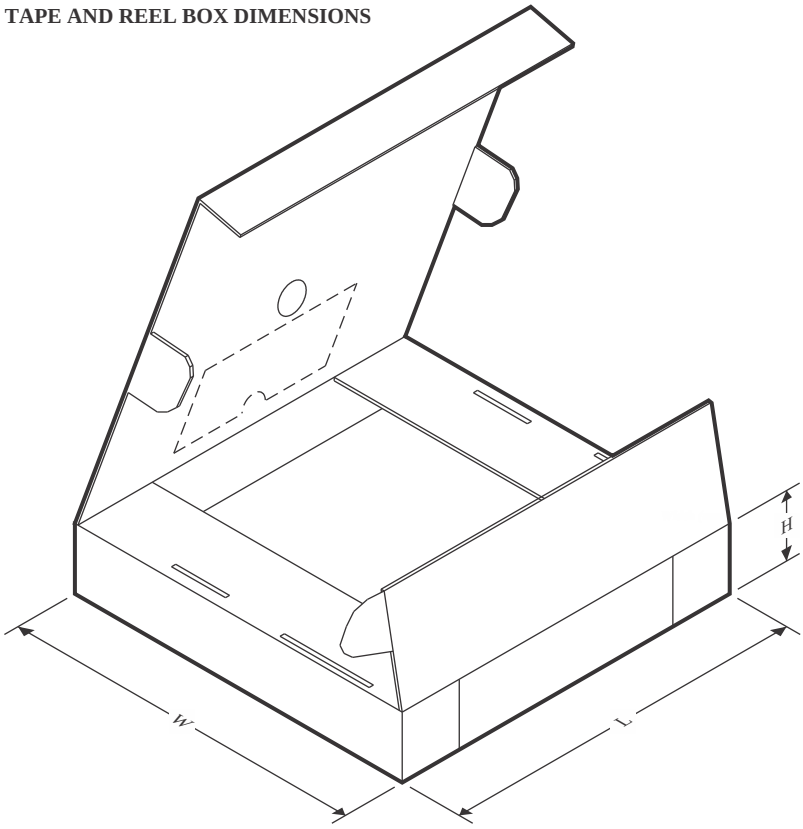
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN75182DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN75182NSR	SOP	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1

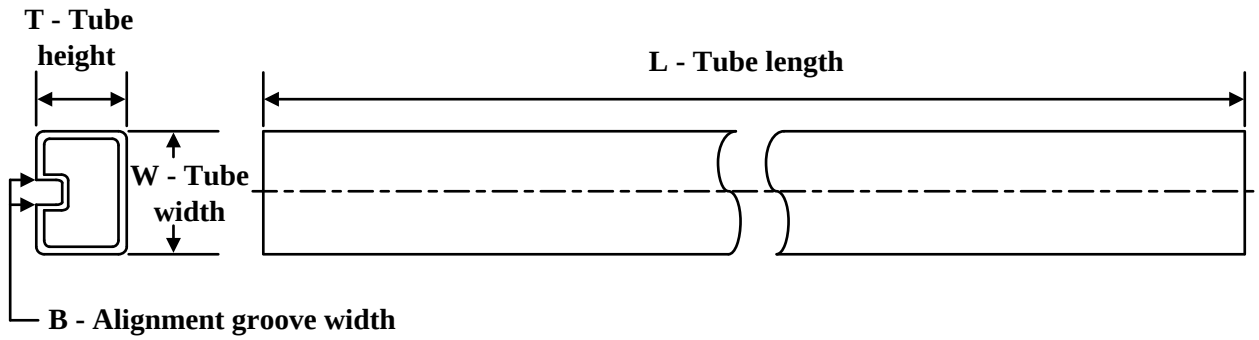
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

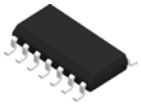
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN75182DR	SOIC	D	14	2500	356.0	356.0	35.0
SN75182NSR	SOP	NS	14	2000	356.0	356.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
5962-7900801VDA	W	CFP	14	25	506.98	26.16	6220	NA
SN75182D	D	SOIC	14	50	506.6	8	3940	4.32
SN75182N	N	PDIP	14	25	506	13.97	11230	4.32

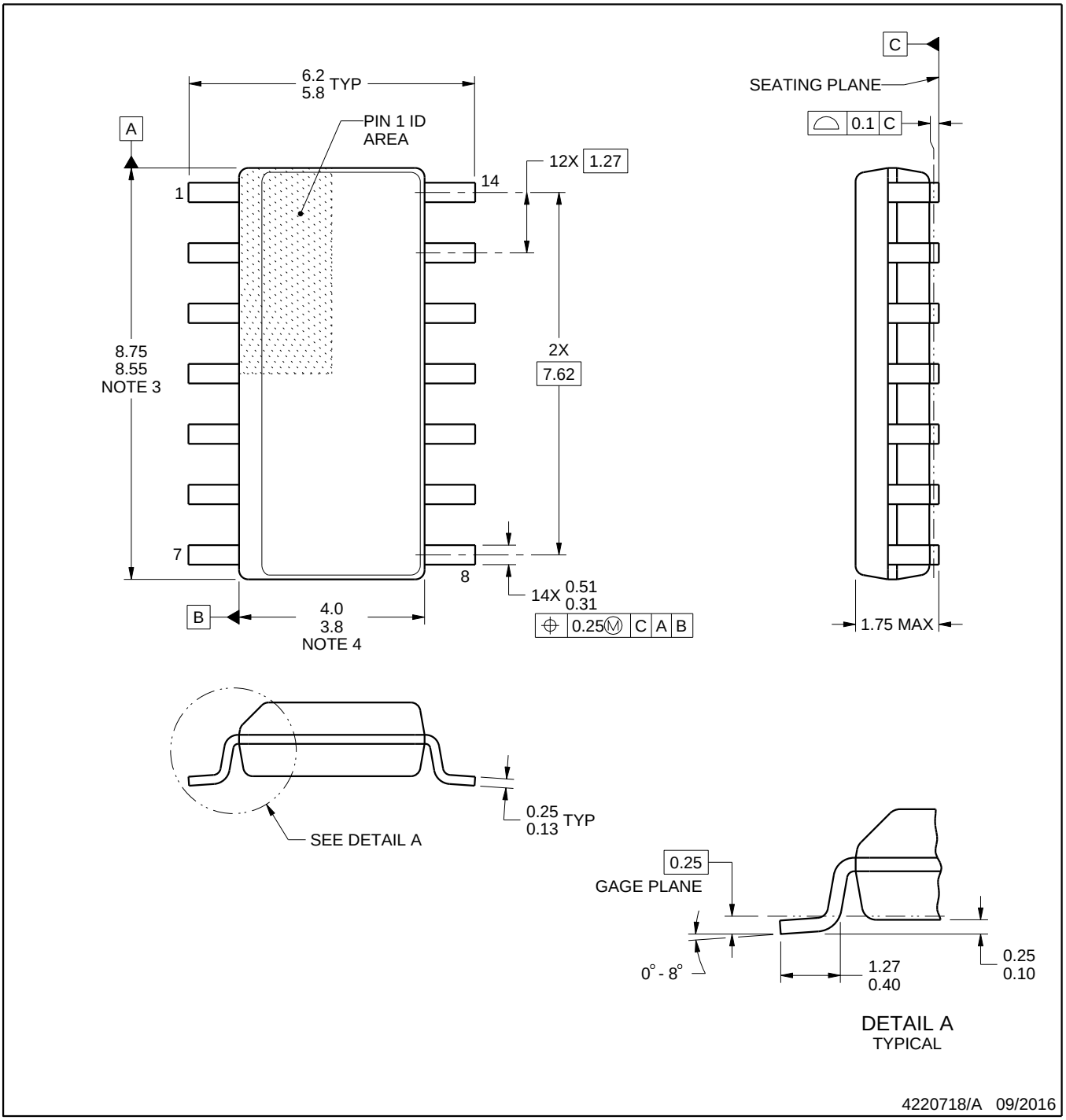


PACKAGE OUTLINE

D0014A

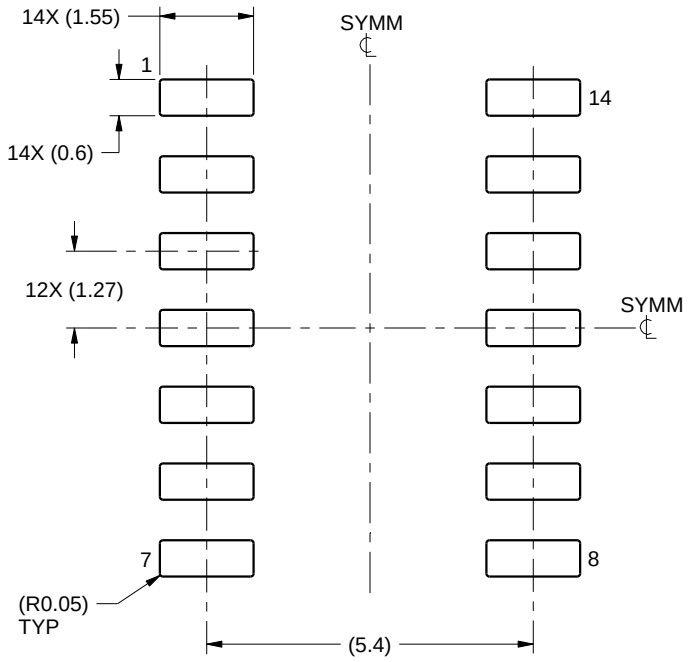
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

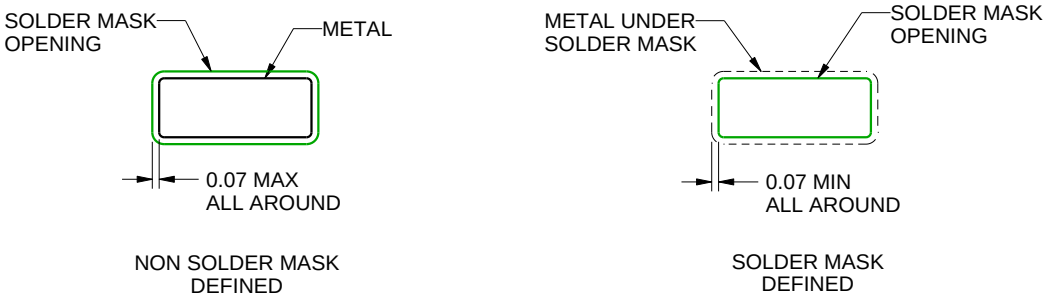


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

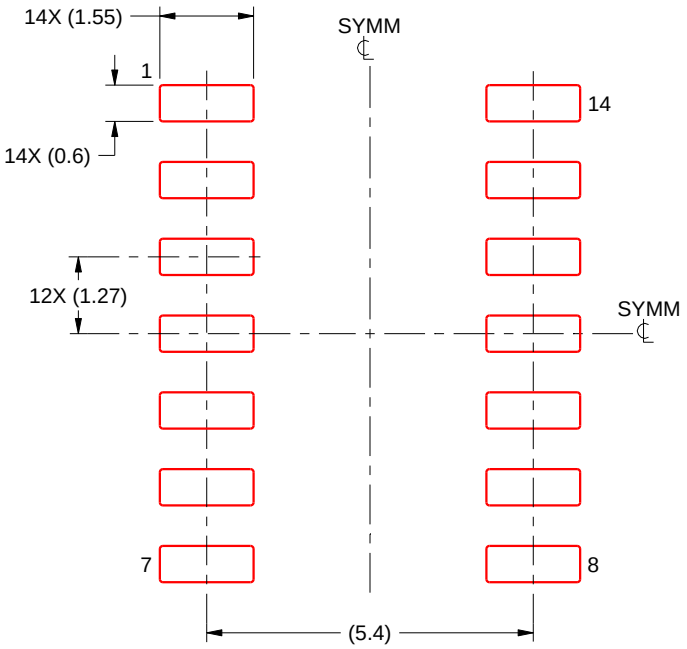
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

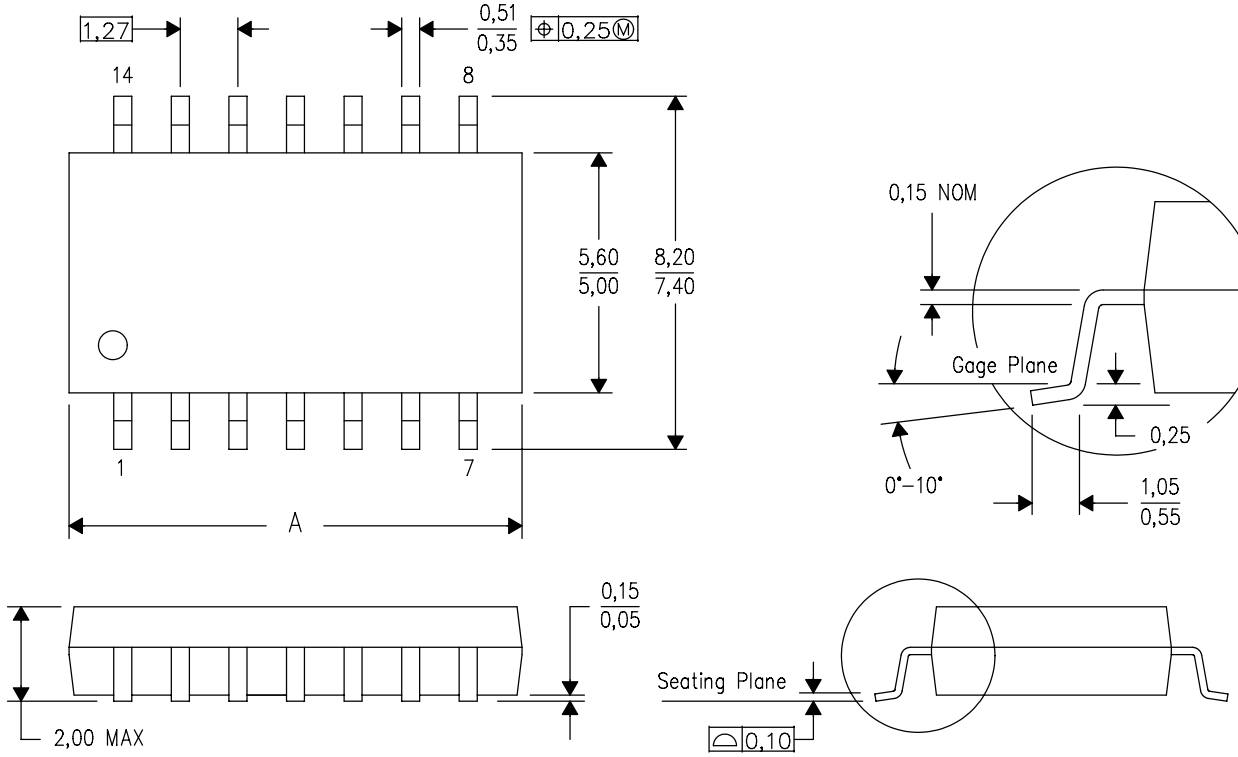
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN

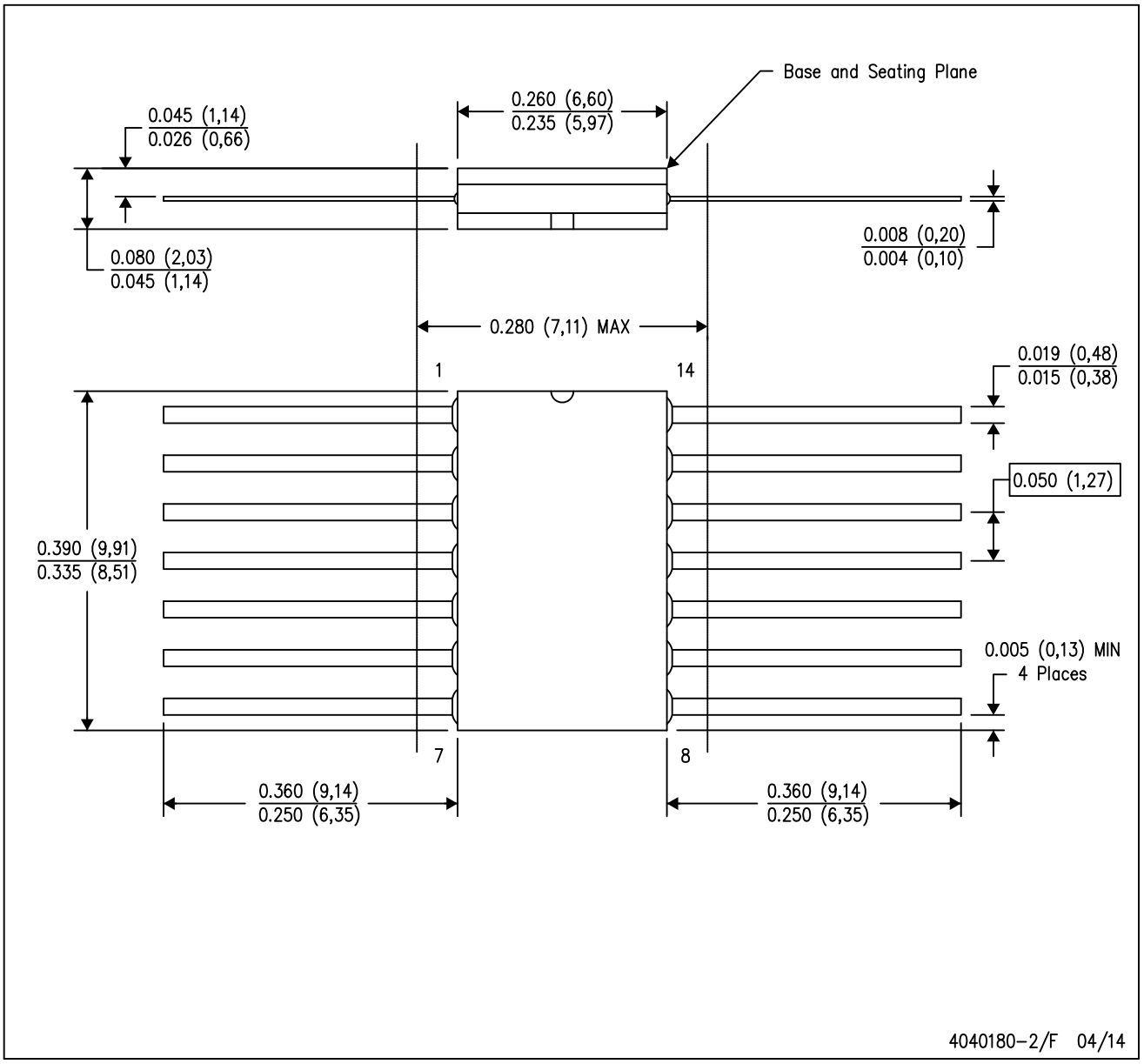


DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

W (R–GDFP–F14) CERAMIC DUAL FLATPACK

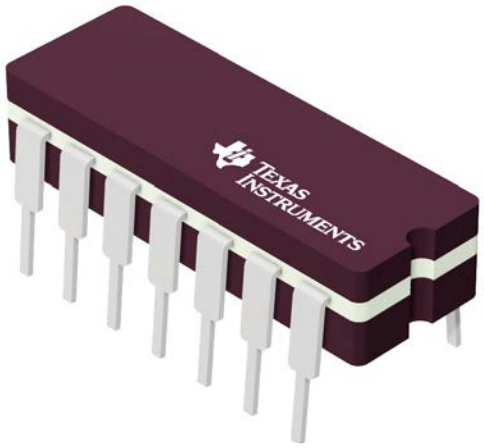


NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within MIL STD 1835 GDFP1–F14

GENERIC PACKAGE VIEW

J 14 CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

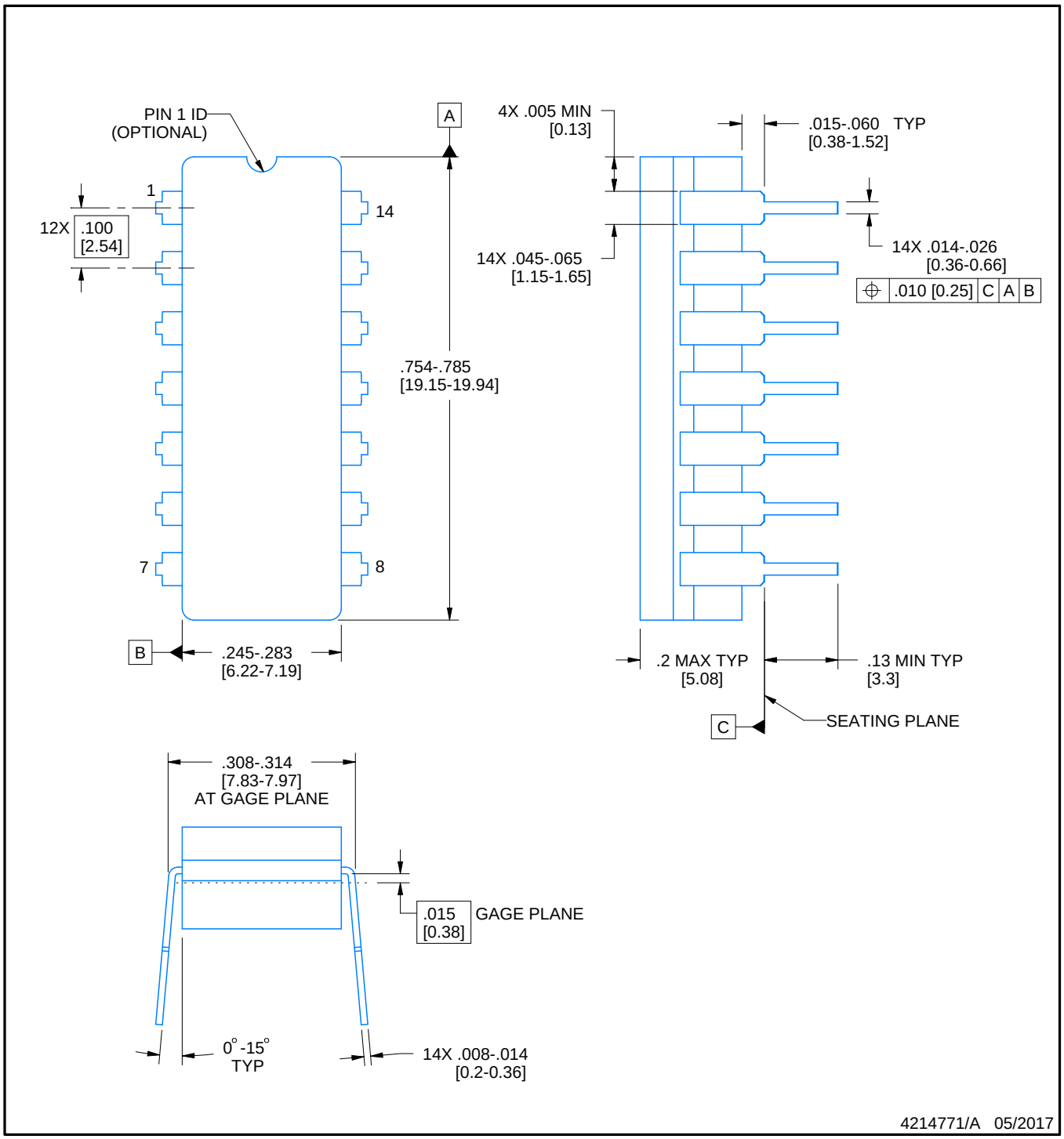
4040083-5/G

PACKAGE OUTLINE

J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



NOTES:

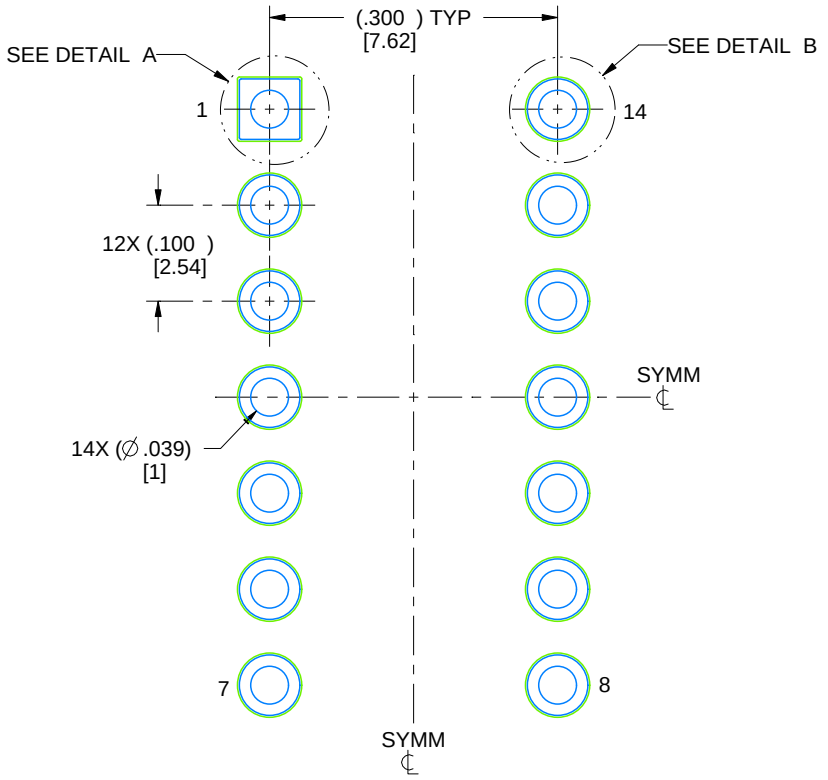
1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermitically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

EXAMPLE BOARD LAYOUT

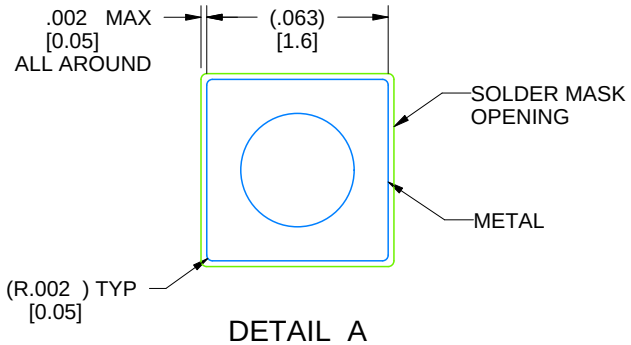
J0014A

CDIP - 5.08 mm max height

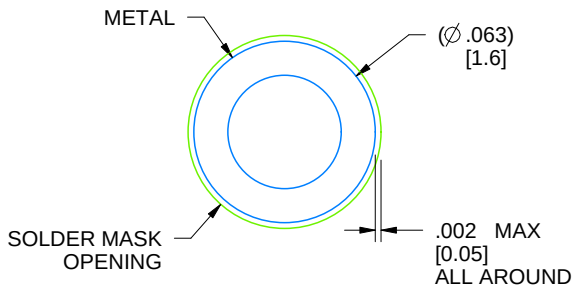
CERAMIC DUAL IN LINE PACKAGE



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X



DETAIL A
SCALE: 15X



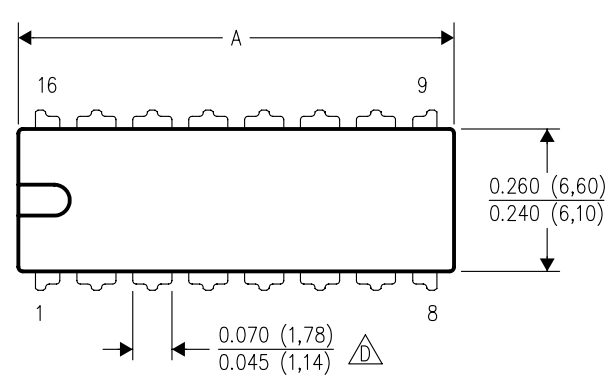
DETAIL B
13X, SCALE: 15X

4214771/A 05/2017

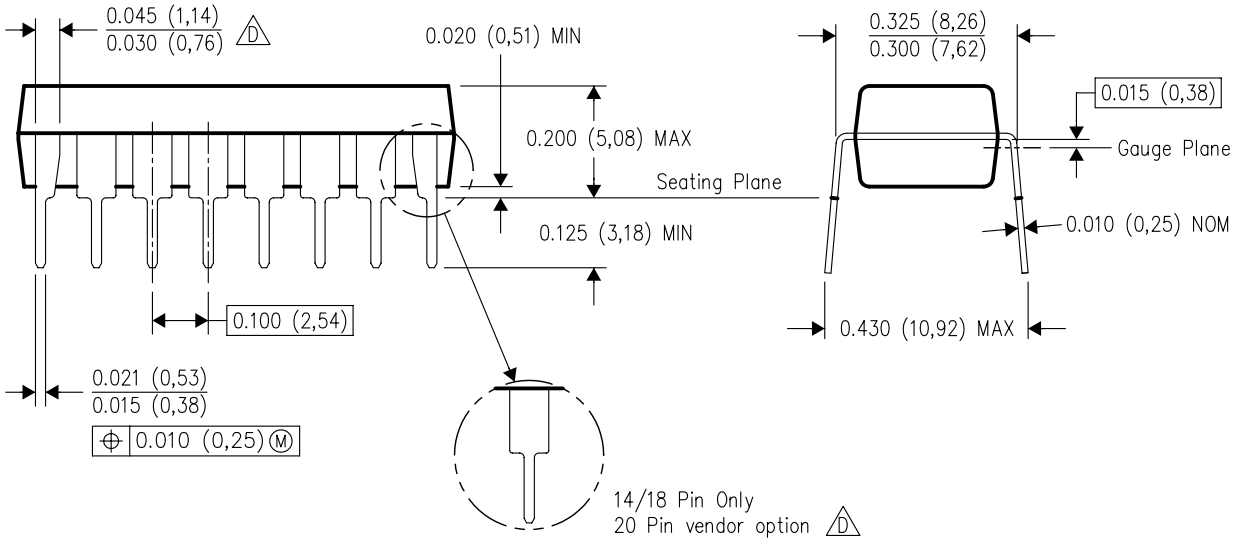
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

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