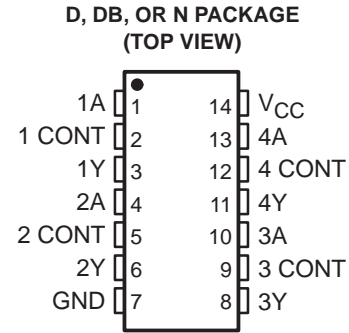


# SN75C189, SN75C189A QUADRUPLE LOW-POWER LINE RECEIVERS

SLLS041G – OCTOBER 1988 – REVISED JANUARY 2000

- Meet or Exceed the Requirements of TIA/EIA-232-F and ITU Recommendation V.28
- Low Supply Current . . . 420  $\mu$ A Typ
- Preset On-Chip Input Noise Filter
- Built-in Input Hysteresis
- Response and Threshold Control Inputs
- Push-Pull Outputs
- Functionally Interchangeable and Pin-to-Pin Compatible With Texas Instruments SN75189/SN75189A and Motorola MC1489/MC1489A
- Package Options Include Plastic Small-Outline (D) and Shrink Small-Outline (DB) Packages, and Standard Plastic (N) DIP



## description

The SN75C189 and SN75C189A are low-power, bipolar, quadruple line receivers that are used to interface data terminal equipment (DTE) with data circuit-terminating equipment (DCE). These devices have been designed to conform to TIA/EIA-232-F.

The SN75C189 has a 0.33-V typical hysteresis, compared with 0.97 V for the SN75C189A. Each receiver has provision for adjustment of the overall input threshold levels. This is achieved by choosing external series resistors and voltages to provide bias levels for the response-control pins. The output is in the high logic state if the input is open circuit or shorted to ground.

These devices have an on-chip filter that rejects input pulses of less than 1- $\mu$ s duration. An external capacitor can be connected from the control pins to ground to provide further input noise filtering for each receiver.

The SN75C189 and SN75C189A have been designed using low-power techniques in a bipolar technology. In most applications, these receivers interface to single inputs of peripheral devices such as UARTs, ACEs, or microprocessors. By using sampling, such peripheral devices usually are insensitive to the transition times of the input signals. If this is not the case, or for other uses, it is recommended that the SN75C189 and SN75C189A outputs be buffered by single Schmitt input gates or single gates of the HCMOS, ALS, or 74F logic families.

The SN75C189 and SN75C189A are characterized for operation from 0°C to 70°C.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS  
INSTRUMENTS**

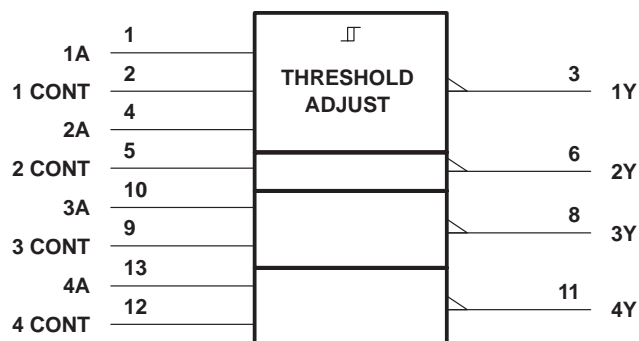
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 2000, Texas Instruments Incorporated

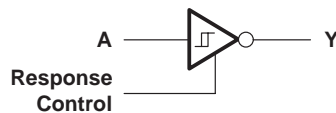
# SN75C189, SN75C189A QUADRUPLE LOW-POWER LINE RECEIVERS

SLLS041G – OCTOBER 1988 – REVISED JANUARY 2000

## logic symbol†



## logic diagram (each receiver)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## schematic of inputs and outputs



‡ All resistor values shown are nominal.

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)§

Supply voltage, $V_{CC}$ (see Note 1)	7 V
Input voltage range, $V_I$	-30 V to 30 V
Output voltage range, $V_O$	-0.3 V to $V_{CC} + 0.3$ V
Package thermal impedance, $\theta_{JA}$ (see Note 2):	
D package	86°C/W
DB package	96°C/W
N package	80°C/W
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C
Storage temperature range, $T_{stg}$	-65°C to 150°C

§ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltages are with respect to network GND.

2. The package thermal impedance is calculated in accordance with JESD 51.



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

# SN75C189, SN75C189A QUADRUPLE LOW-POWER LINE RECEIVERS

SLLS041G – OCTOBER 1988 – REVISED JANUARY 2000

## recommended operating conditions

	MIN	NOM	MAX	UNIT
V <sub>CC</sub> Supply voltage	4.5	5	6	V
V <sub>I</sub> Input voltage (see Note 3)	-25		25	V
I <sub>OH</sub> High-level output current			-3.2	mA
I <sub>OL</sub> Low-level output current			3.2	mA
Response-control current			±1	mA
T <sub>A</sub> Operating free-air temperature	0		70	°C

NOTE 3: The algebraic convention, where the more positive (less negative) limit is designated as maximum, is used in this data sheet for logic levels only, e.g., if -10 V is a maximum, the typical value is a more negative voltage.

## electrical characteristics over recommended free-air temperature range, V<sub>CC</sub> = 5 V ±10% (unless otherwise noted) (see Note 4)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V <sub>IT+</sub> Positive-going input threshold voltage	'C189	See Figure 1	1		1.5	V
	'C189A		1.6		2.25	
V <sub>IT-</sub> Negative-going input threshold voltage	'C189	See Figure 1	0.75		1.25	V
	'C189A		0.75	1	1.25	
V <sub>hys</sub> Input hysteresis voltage (V <sub>IT+</sub> - V <sub>IT-</sub> )	'C189	See Figure 1	0.15	0.33		V
	'C189A		0.65	0.97		
V <sub>OH</sub> High-level output voltage		V <sub>CC</sub> = 4.5 V to 6 V, V <sub>I</sub> = 0.75 V, I <sub>OH</sub> = -20 μA	3.5			V
		V <sub>CC</sub> = 4.5 V to 6 V, V <sub>I</sub> = 0.75 V, I <sub>OH</sub> = -3.2 mA	2.5			
V <sub>OL</sub> Low-level output voltage		V <sub>CC</sub> = 4.5 V to 6 V, V <sub>I</sub> = 3 V, I <sub>OL</sub> = 3.2 mA			0.4	V
I <sub>IH</sub> High-level input current		See Figure 2	V <sub>I</sub> = 25 V	3.6	8.3	mA
			V <sub>I</sub> = 3 V	0.43	1	
I <sub>IL</sub> Low-level input current		See Figure 2	V <sub>I</sub> = -25 V	-3.6	-8.3	mA
			V <sub>I</sub> = -3 V	-0.43	-1	
I <sub>OS</sub> Short-circuit output current		See Figure 3			-35	mA
I <sub>CC</sub> Supply current		V <sub>I</sub> = 5 V, No load, See Figure 2		420	700	μA

† All typical values are at T<sub>A</sub> = 25°C.

NOTE 4: All characteristics are measured with response-control terminal open.

## switching characteristics, V<sub>CC</sub> = 5 V ±10%, T<sub>A</sub> = 25°C

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t <sub>PLH</sub> Propagation delay time, low- to high-level output	R <sub>L</sub> = 5 kΩ, C <sub>L</sub> = 50 pF, See Figure 4			6	μs
t <sub>PHL</sub> Propagation delay time, high- to low-level output				6	μs
t <sub>TLH</sub> Transition time, low- to high-level output‡				500	ns
t <sub>THL</sub> Transition time, high- to low-level output‡				300	ns
t <sub>w(N)</sub> Duration of longest pulse rejected as noise§			1		6

‡ Measured between 10% and 90% points of output waveform

§ The receiver ignores any positive- or negative-going pulse that is less than the minimum value of t<sub>w(N)</sub> and accepts any positive- or negative-going pulse greater than the maximum of t<sub>w(N)</sub>.



# SN75C189, SN75C189A QUADRUPLE LOW-POWER LINE RECEIVERS

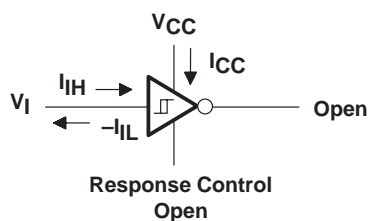
SLLS041G – OCTOBER 1988 – REVISED JANUARY 2000

## PARAMETER MEASUREMENT INFORMATION



NOTE A: Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

Figure 1.  $V_{T+}$ ,  $V_{IT-}$ ,  $V_{OH}$ ,  $V_{OL}$



NOTE A: Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

Figure 2.  $I_{iH}$ ,  $I_{iL}$ ,  $I_{CC}$



NOTE A: Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

Figure 3.  $I_{OS}$

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

- NOTES: A.  $C_L$  includes probe and jig capacitances.  
 B. The pulse generator has the following characteristics:  $Z_O = 50\ \Omega$ ,  $t_w = 25\ \mu\text{s}$ .

Figure 4. Test Circuit and Voltage Waveforms

# SN75C189, SN75C189A QUADRUPLE LOW-POWER LINE RECEIVERS

SLLS041G – OCTOBER 1988 – REVISED JANUARY 2000

## TYPICAL CHARACTERISTICS

**SN75C189**  
INPUT THRESHOLD VOLTAGE (POSITIVE GOING)  
vs  
FREE-AIR TEMPERATURE



Figure 5

**SN75C189A**  
INPUT THRESHOLD VOLTAGE (POSITIVE GOING)  
vs  
FREE-AIR TEMPERATURE



Figure 6

**SN75C189**  
INPUT THRESHOLD VOLTAGE (NEGATIVE GOING)  
vs  
FREE-AIR TEMPERATURE

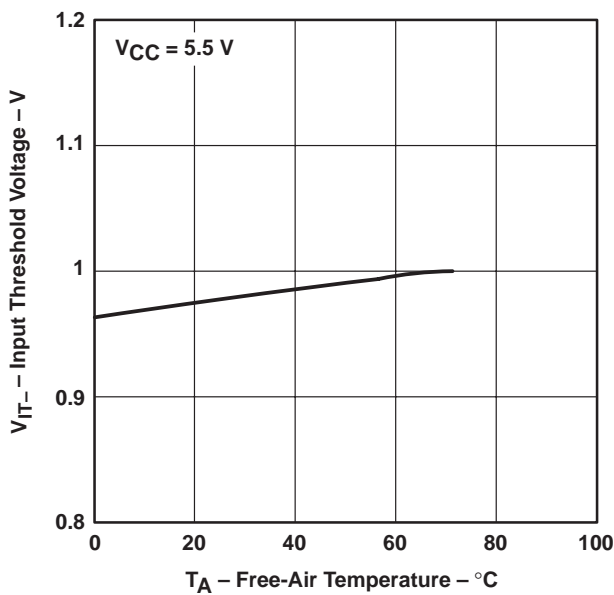


Figure 7

**SN75C189A**  
INPUT THRESHOLD VOLTAGE (NEGATIVE GOING)  
vs  
FREE-AIR TEMPERATURE

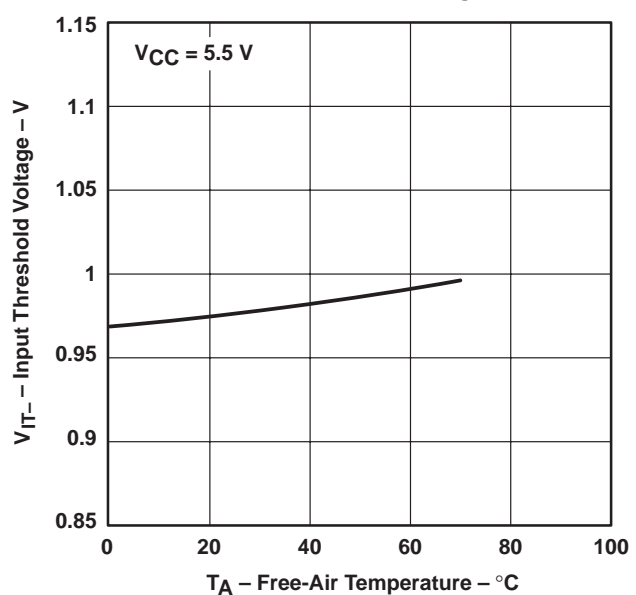


Figure 8



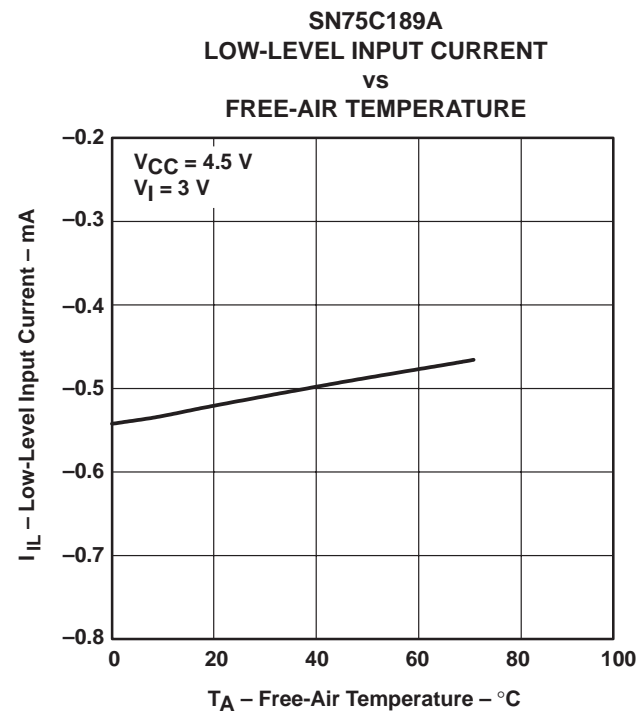
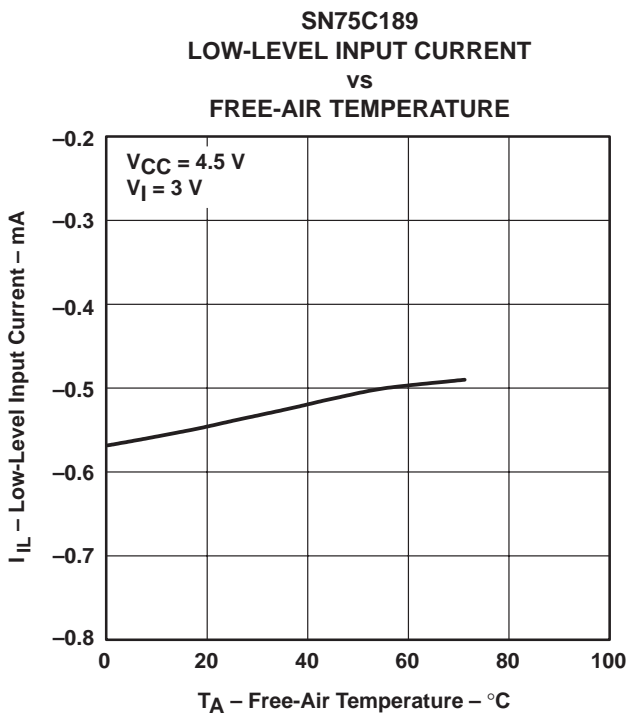
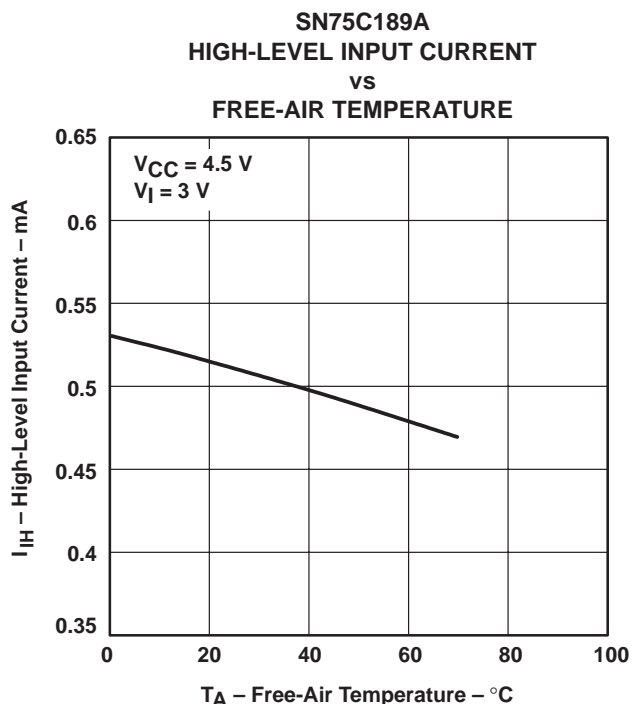
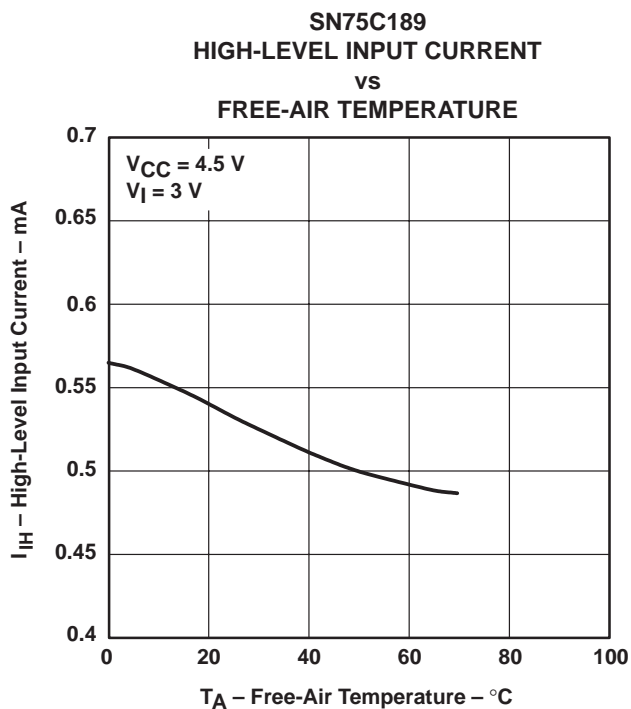
TYPICAL CHARACTERISTICS



# SN75C189, SN75C189A QUADRUPLE LOW-POWER LINE RECEIVERS

SLLS041G – OCTOBER 1988 – REVISED JANUARY 2000

## TYPICAL CHARACTERISTICS





TYPICAL CHARACTERISTICS



Figure 17



Figure 18

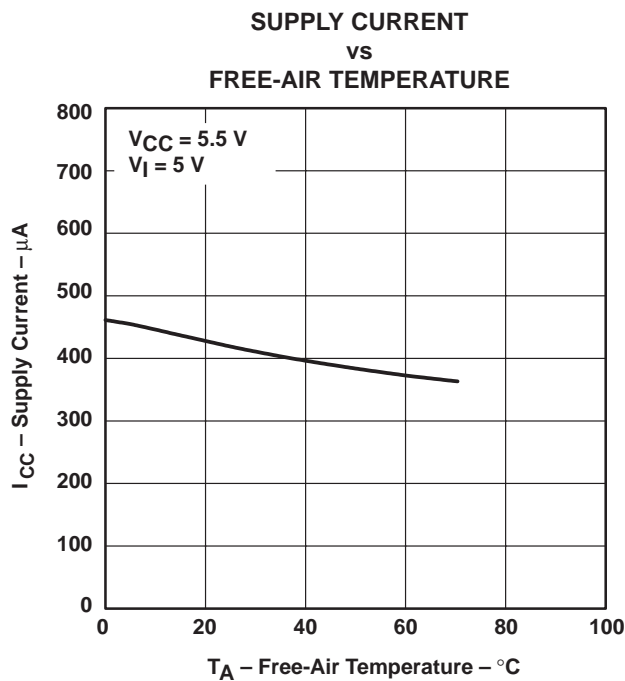


Figure 19



Figure 20

# SN75C189, SN75C189A QUADRUPLE LOW-POWER LINE RECEIVERS

SLLS041G – OCTOBER 1988 – REVISED JANUARY 2000

## TYPICAL CHARACTERISTICS



Figure 21

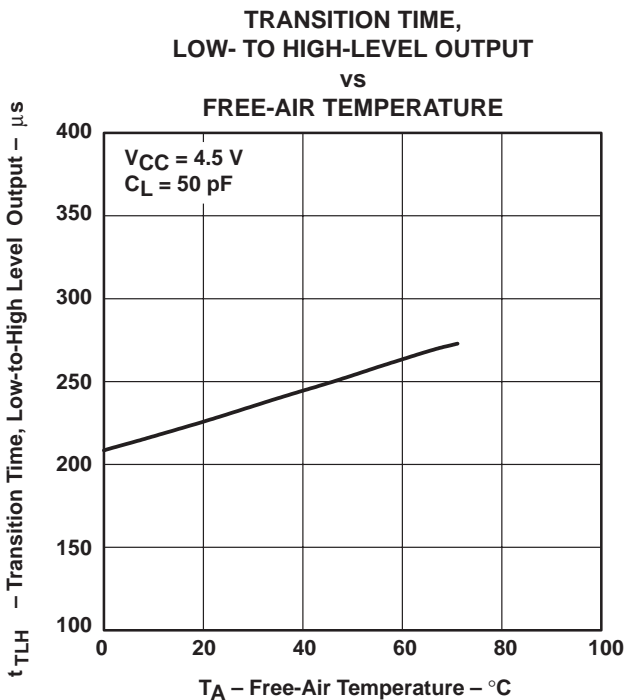


Figure 22

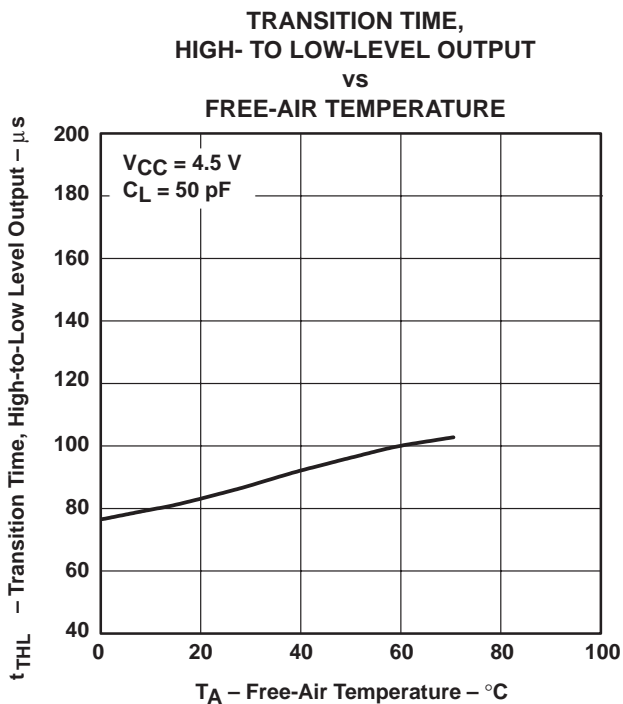


Figure 23



**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN75C189AD	OBSOLETE	SOIC	D	14		TBD	Call TI	Call TI	0 to 70	75C189A	
SN75C189ADBR	ACTIVE	SSOP	DB	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	CA189A	Samples
SN75C189ADBRE4	ACTIVE	SSOP	DB	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	CA189A	Samples
SN75C189ADR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	75C189A	Samples
SN75C189AN	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	SN75C189AN	Samples
SN75C189ANE4	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	SN75C189AN	Samples
SN75C189ANSR	ACTIVE	SOP	NS	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	75C189A	Samples
SN75C189D	OBSOLETE	SOIC	D	14		TBD	Call TI	Call TI	0 to 70	SN75C189	
SN75C189DR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75C189	Samples
SN75C189DRE4	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75C189	Samples
SN75C189N	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	SN75C189N	Samples
SN75C189NSR	ACTIVE	SOP	NS	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	75C189	Samples

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN75C189ADBR	SSOP	DB	14	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
SN75C189ADR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN75C189ADR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN75C189ANSR	SOP	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN75C189DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN75C189NSR	SOP	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN75C189ADBR	SSOP	DB	14	2000	356.0	356.0	35.0
SN75C189ADR	SOIC	D	14	2500	353.0	353.0	32.0
SN75C189ADR	SOIC	D	14	2500	356.0	356.0	35.0
SN75C189ANSR	SOP	NS	14	2000	356.0	356.0	35.0
SN75C189DR	SOIC	D	14	2500	356.0	356.0	35.0
SN75C189NSR	SOP	NS	14	2000	356.0	356.0	35.0

**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN75C189AN	N	PDIP	14	25	506	13.97	11230	4.32
SN75C189ANE4	N	PDIP	14	25	506	13.97	11230	4.32
SN75C189N	N	PDIP	14	25	506	13.97	11230	4.32

D0014A



# PACKAGE OUTLINE

## SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.



# EXAMPLE BOARD LAYOUT

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



# MECHANICAL DATA

NS (R-PDSO-G\*\*)

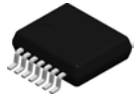
PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

# DB0014A



# PACKAGE OUTLINE

## SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



### NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-150.

# EXAMPLE BOARD LAYOUT

DB0014A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



4220762/A 05/2024

NOTES: (continued)

- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DB0014A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220762/A 05/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.



## IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](https://www.ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2024, Texas Instruments Incorporated