AM26C31-EP
QUADRUPLE DIFFERENTIAL LINE DRIVER

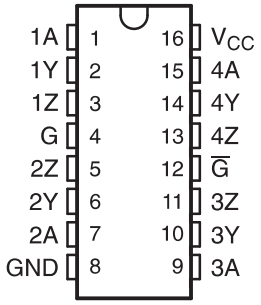
SLLS871–NOVEMBER 2007

FEATURES

- **Controlled Baseline**
  - **One Assembly**
  - **One Test Site**
  - **One Fabrication Site**
- **Extended Temperature Performance of –55°C to 125°C**
- **Enhanced Diminishing Manufacturing Sources (DMS) Support**
- **Enhanced Product-Change Notification**
- **Qualification Pedigree** (1)
- **Meets or Exceeds the Requirements of TIA/EIA-422-B and ITU Recommendation V.11**
- **Low Power, I_{CC} = 100 μA Typ**
- **Operates From a Single 5 V Supply**
- **High Speed, $t_{PLH} = t_{PHL}$ = 7 ns Typ**
- **Low Pulse Distortion, $t_{sk(p)}$ = 0.5 ns Typ**
- **High Output Impedance in Power-Off Conditions**
- **Improved Replacement for AM26LS31**

(1) Component qualification in accordance with JEDEC and industry standards to ensure reliable operation over an extended temperature range. This includes, but is not limited to, Highly Accelerated Stress Test (HAST) or biased 85/85, temperature cycle, autoclave or unbiased HAST, electromigration, bond intermetallic life, and mold compound life. Such qualification testing should not be viewed as justifying use of this component beyond specified performance and environmental limits.

AM26C31... D PACKAGE



DESCRIPTION/ORDERING INFORMATION

The AM26C31 is a differential line driver with complementary outputs, designed to meet the requirements of TIA/EIA -422-B and ITU (formerly CCITT). The 3-state outputs have high-current capability for driving balanced lines, such as twisted-pair or parallel-wire transmission lines, and they provide the high-impedance state in the power-off condition. The enable functions are common to all four drivers and offer the choice of an active-high (G) or active-low ($\overline{G}$) enable input. BiCMOS circuitry reduces power consumption without sacrificing speed.

The AM26C31 is characterized for operation over extended temperature range of –55°C to 125°C.

ORDERING INFORMATION(1)

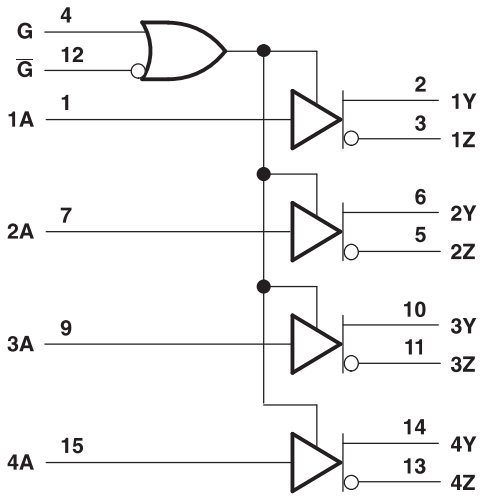
T_A	PACKAGE(2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–55°C to 125°C	SOIC – D	Reel of 2500	AM26C31MDREP	26C31EP

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

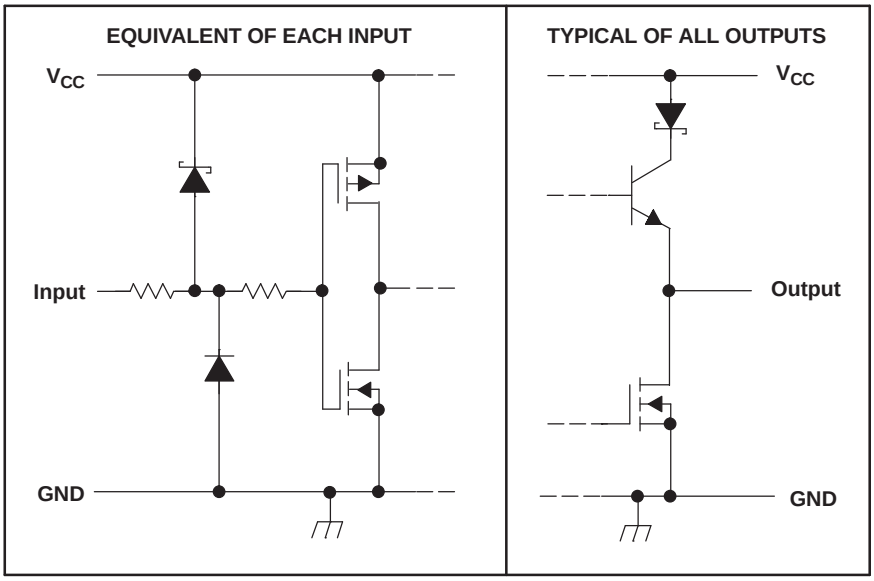
FUNCTION TABLE
(each driver)

INPUT A	ENABLES		OUTPUT	
	G	$\overline{G}$	Y	Z
H	H	X	H	L
L	H	X	L	H
H	X	L	H	L
L	X	L	L	H
X	L	H	Z	Z

LOGIC DIAGRAM (POSITIVE LOGIC)



SCHEMATICS OF INPUTS AND OUTPUTS



ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{CC}	Supply voltage range(2)	–0.5	7	V
V_I	Input voltage range	–0.5	V_{CC} + 0.5	V
V_{ID}	Differential input voltage range	–14	14	V
V_O	Output voltage range	–0.5	7	V
I_{IK} or I_{OK}	Input or output clamp current		±20	mA
I_O	Output current		±150	mA
	V_{CC} current		200	mA
	GND current		–200	mA
θ_{JA}	Package thermal impedance(3)(4)		73	°C/W
T_J	Operating virtual junction temperature		150	°C
T_{stg}	Storage temperature range	–65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential output voltage (V_{OD}), are with respect to the network ground terminal.
(3) Maximum power dissipation is a function of $T_J(max)$, θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) – T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
(4) The package thermal impedance is calculated in accordance with JESD 51-7.

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{ID}	Differential input voltage		±7		V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{OH}	High-level output current			–20	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature	–55		125	°C

ELECTRICAL CHARACTERISTICS

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
V_{OH}	High-level output voltage	I_O = –20 mA		2.2	3.4		V
V_{OL}	Low-level output voltage	I_O = 20 mA			0.2	0.4	V
$\|V_{OD}\|$	Differential output voltage magnitude	R_L = 100 Ω, See Figure 1		2	3.1		V
$\Delta\|V_{OD}\|$	Change in magnitude of differential output voltage(2)	R_L = 100 Ω, See Figure 1				±0.4	V
V_{OC}	Common-mode output voltage	R_L = 100 Ω, See Figure 1				3	V
$\Delta\|V_{OC}\|$	Change in magnitude of common-mode output voltage(2)	R_L = 100 Ω, See Figure 1				±0.4	V
I_I	Input current	V_I = V_{CC} or GND				±1	µA
$I_{O(off)}$	Driver output current with power off	V_{CC} = 0	V_O = 6 V			100	µA
			V_O = –0.25 V			–100	
I_{OS}	Driver output short-circuit current	V_O = 0				–170	mA
I_{OZ}	High-impedance off-state output current	V_O = 2.5 V				20	µA
		V_O = 0.5 V				–20	
I_{CC}	Quiescent supply current	I_O = 0	V_I = 0 V or 5 V			100	µA
		I_O = 0	V_I = 2.4 V or 0.5 V(3)			3.2	mA
C_I	Input capacitance				6		pF

(1) All typical values are at V_{CC} = 5 V and T_A = 25°C.
(2) $\Delta|V_{OD}|$ and $\Delta|V_{OC}|$ are the changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low level.
(3) This parameter is measured per input. All other inputs are at 0 V or 5 V.

SWITCHING CHARACTERISTICS

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	S1 is open,	See Figure 2		7	12	ns
t_{PHL}	Propagation delay time, high- to low-level output	S1 is open,	See Figure 2		6.5	12	ns
$t_{sk(p)}$	Pulse skew time ($\|t_{PLH} - t_{PHL}\|$)	S1 is open,	See Figure 2		0.5	4	ns
$t_{r(OD)}$, $t_{f(OD)}$	Differential output rise and fall times	S1 is open,	See Figure 3		5	12	ns
t_{PZH}	Output enable time to high level	S1 is closed,	See Figure 4		10	19	ns
t_{PZL}	Output enable time to low level	S1 is closed,	See Figure 4		10	19	ns
t_{PHZ}	Output disable time from high level	S1 is closed,	See Figure 4		7	16	ns
t_{PLZ}	Output disable time from low level	S1 is closed,	See Figure 4		7	16	ns
C_{pd}	Power dissipation capacitance (each driver)(2)	S1 is open,	See Figure 2		100		pF

(1) All typical values are at V_{CC} = 5 V, T_A = 25°C.
(2) C_{pd} is used to estimate the switching losses according to $P_D = C_{pd} \times V_{CC}^2 \times f$, where f is the switching frequency.

PARAMETER MEASUREMENT INFORMATION

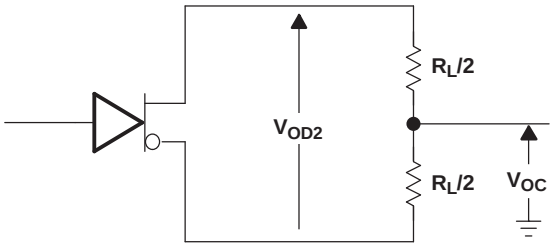
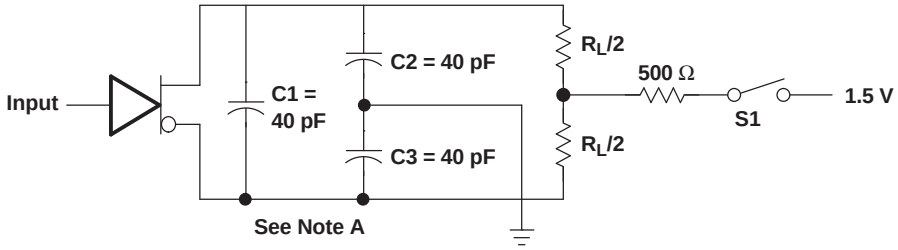
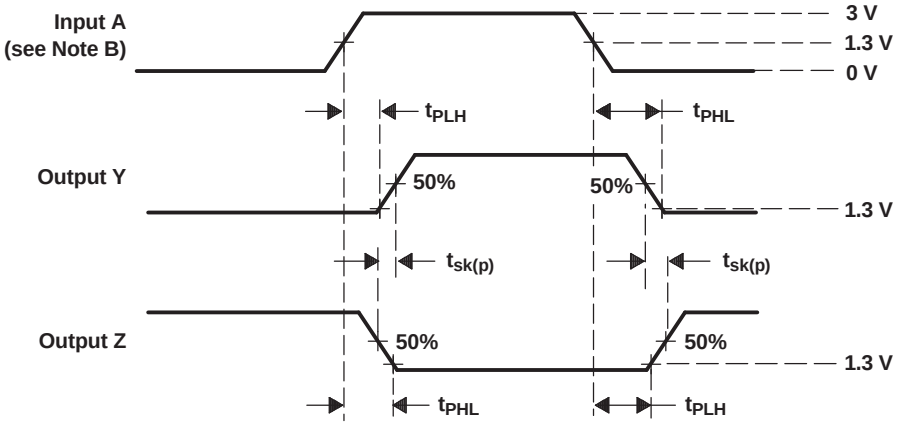


Figure 1. Differential and Common-Mode Output Voltages



TEST CIRCUIT

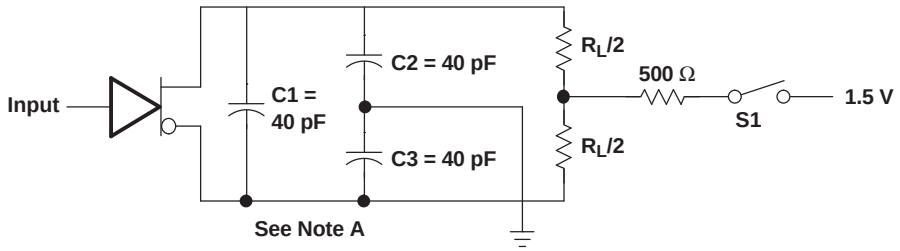


A. C1, C2, and C3 include probe and jig capacitance.

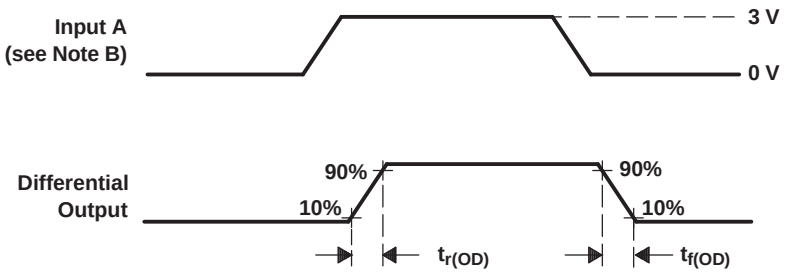
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, duty cycle ≤ 50%, and t_r, t_f ≤ 6 ns.

Figure 2. Propagation Delay Time and Skew Waveforms and Test Circuit

PARAMETER MEASUREMENT INFORMATION (continued)



TEST CIRCUIT



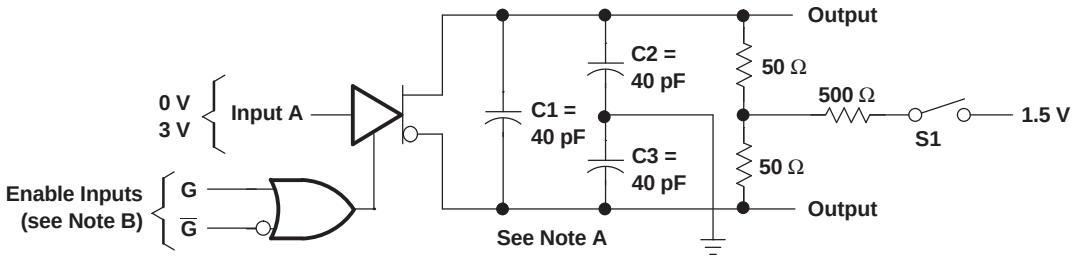
VOLTAGE WAVEFORMS

A. C1, C2, and C3 include probe and jig capacitance.

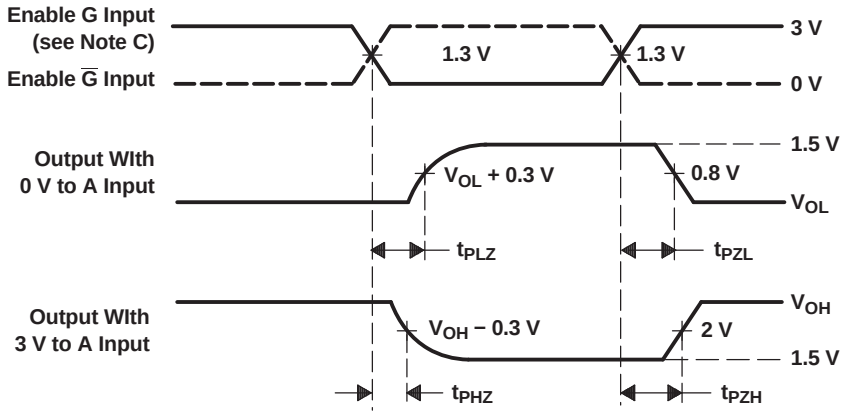
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, duty cycle ≤ 50%, and t_r, t_f ≤ 6 ns.

Figure 3. Differential Output Rise and Fall Time Waveforms and Test Circuit

PARAMETER MEASUREMENT INFORMATION (continued)



TEST CIRCUIT



VOLTAGE WAVEFORMS

A. C1, C2, and C3 include probe and jig capacitance.

B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, duty cycle ≤ 50%, t_r < 6 ns, and t_f < 6 ns.

C. Each enable is tested separately.

Figure 4. Output Enable and Disable Time Waveforms and Test Circuit

TYPICAL CHARACTERISTICS

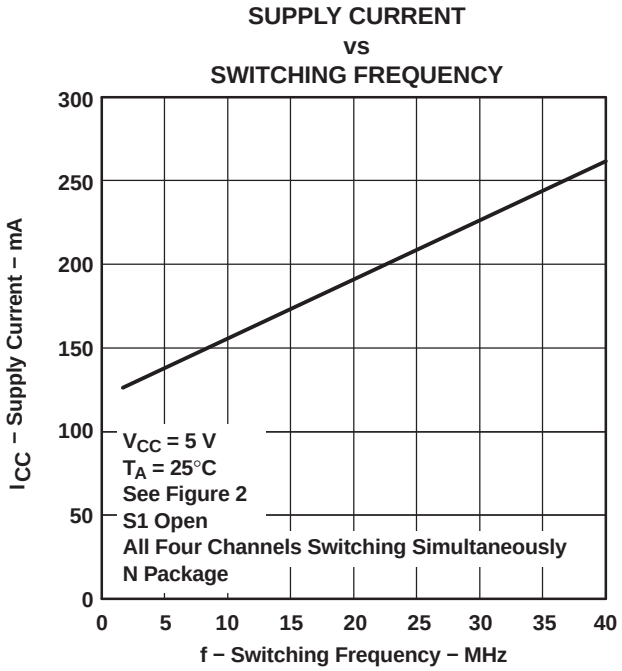


Figure 5.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
AM26C31MDREP	ACTIVE	SOIC	D	16	2500	RoHS & Green	Call TI | NIPDAU	Level-1-260C-UNLIM	-55 to 125	26C31EP	Samples
V62/07647-01XE	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	26C31EP	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF AM26C31-EP :

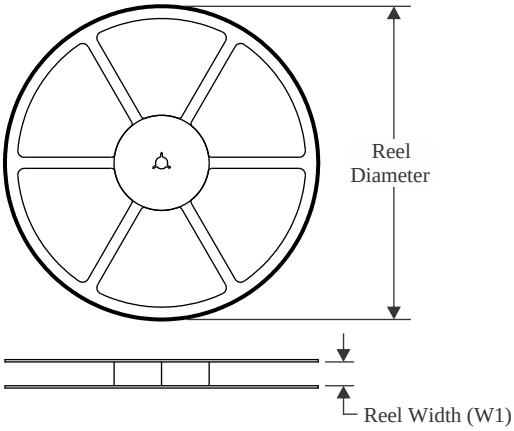
- Catalog: AM26C31
- Military: AM26C31M

NOTE: Qualified Version Definitions:

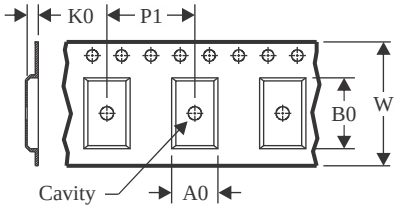
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

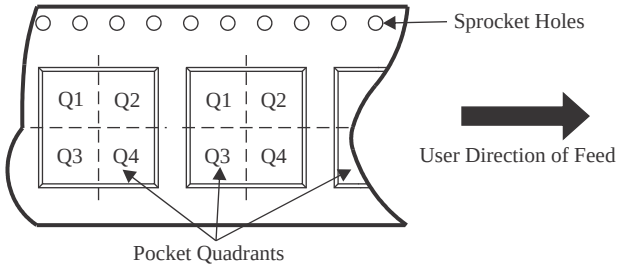


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

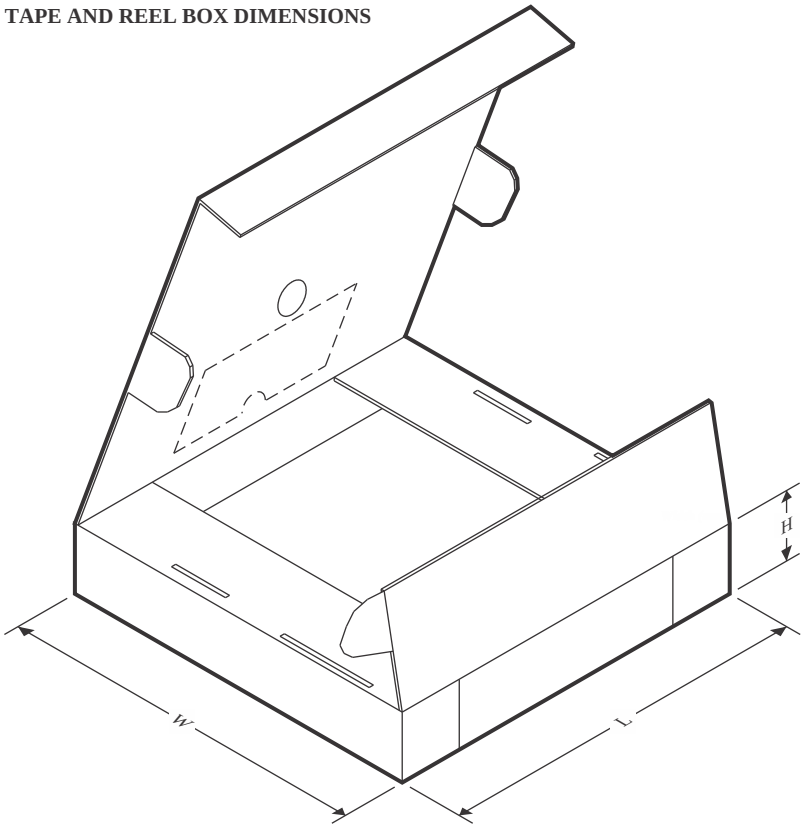
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
AM26C31MDREP	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1

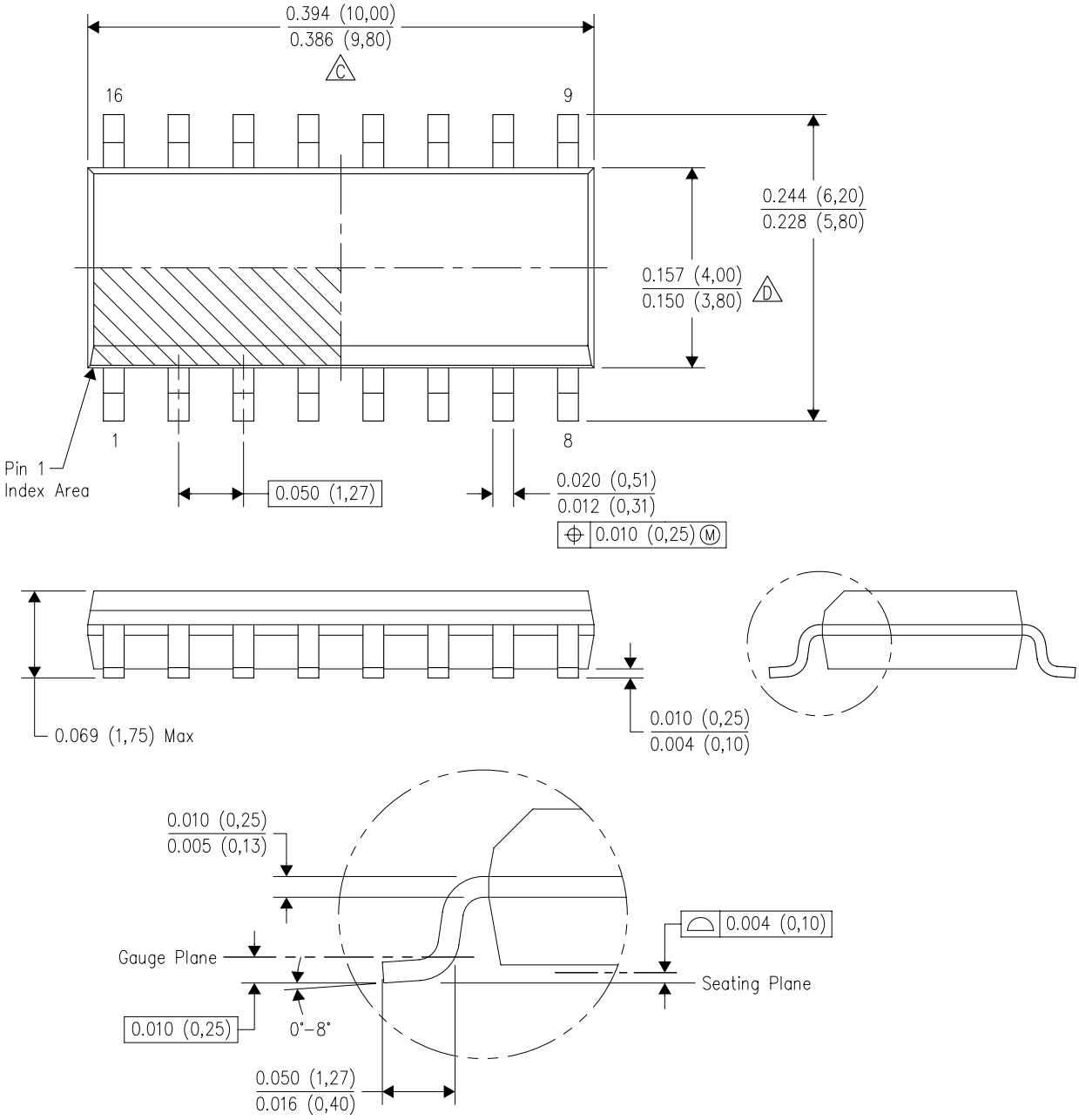
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
AM26C31MDREP	SOIC	D	16	2500	340.5	336.1	32.0

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265