



# 16-Ch/Dual 8-Ch High-Performance CMOS Analog Multiplexers

## DESCRIPTION

The DG406B is a 16-channel single-ended analog multiplexer designed to connect one of sixteen inputs to a common output as determined by a 4-bit binary address. The DG407B selects one of eight differential inputs to a common differential output. Break-before-make switching action protects against momentary shorting of inputs.

An on channel conducts current equally well in both directions. In the off state each channel blocks voltages up to the power supply rails. An enable (EN) function allows the user to reset the multiplexer/demultiplexer to all switches off for stacking several devices. All control inputs, address (A<sub>x</sub>) and enable (EN) are TTL compatible over the full specified operating temperature range.

Applications for the DG406B, DG407B include high speed data acquisition, audio signal switching and routing, ATE systems, and avionics. High performance and low power dissipation make them ideal for battery operated and remote instrumentation applications.

Designed in the 44 V silicon-gate CMOS process, the absolute maximum voltage rating is extended to 44 V, allowing operation with ± 20 V supplies. Additionally single (12 V) supply operation is allowed. An epitaxial layer prevents latchup.

## FEATURES

- Low on-resistance - R<sub>DS(on)</sub>: 45 Ω
- Low charge injection - Q: 11 pC
- Fast transition time - t<sub>TRANS</sub>: 115 ns
- Low power: 0.2 mW
- Single supply capability
- Material categorization: for definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)



## Note

\* This datasheet provides information about parts that are RoHS-compliant and / or parts that are non RoHS-compliant. For example, parts with lead (Pb) terminations are not RoHS-compliant. Please see the information / tables in this datasheet for details

## BENEFITS

- Higher accuracy
- Reduced glitching
- Improved data throughput
- Reduced power consumption
- Increased ruggedness
- Wide supply ranges: ± 5 V to ± 20 V

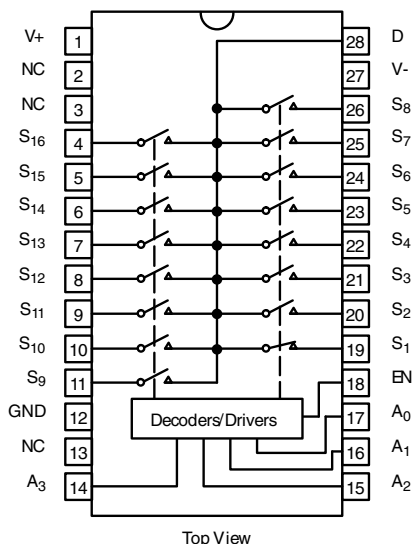
## APPLICATIONS

- Data acquisition systems
- Audio signal routing
- Medical instrumentation
- ATE systems
- Battery powered systems
- High-rel systems
- Single supply systems

## FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION

DG406B

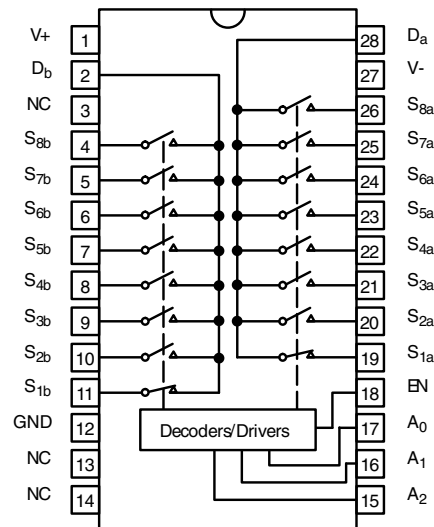
SOIC Wide-Body



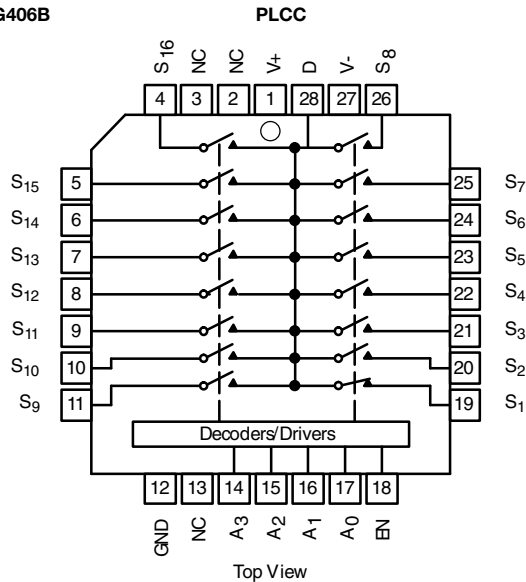
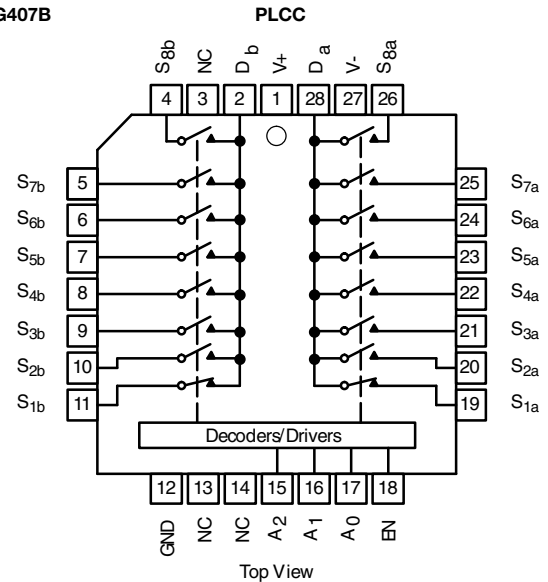
Top View

DG407B

SOIC Wide-Body



Top View

**FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION**
**DG406B**

**DG407B**


TRUTH TABLE (DG406B)					
A <sub>3</sub>	A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>	EN	ON SWITCH
X	X	X	X	0	None
0	0	0	0	1	1
0	0	0	1	1	2
0	0	1	0	1	3
0	0	1	1	1	4
0	1	0	0	1	5
0	1	0	1	1	6
0	1	1	0	1	7
0	1	1	1	1	8
1	0	0	0	1	9
1	0	0	1	1	10
1	0	1	0	1	11
1	0	1	1	1	12
1	1	0	0	1	13
1	1	0	1	1	14

ORDERING INFORMATION (DG406B)		
TEMP. RANGE	PACKAGE	PART NUMBER
-40 °C to +85 °C	28-pin PLCC	DG406BDN-T1-E3
	28-pin widebody SOIC	DG406BDW-E3, DG406BDW-T1-E3

**Note**

- T1 indicates tape and reel, -E3 indicates lead (Pb)-free and RoHS-compliant, NO -E3 indicates standard tin/lead finish

TRUTH TABLE (DG406B)					
1	1	1	0	1	15
1	1	1	1	1	16

TRUTH TABLE (DG407B)				
A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>	EN	ON SWITCH
X	X	X	0	None
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

**Notes**

- Logic "0" = V<sub>AL</sub> ≤ 0.8 V
- Logic "1" = V<sub>AH</sub> ≥ 2.4 V
- X = do not care

ORDERING INFORMATION (DG407B)		
TEMP. RANGE	PACKAGE	PART NUMBER
-40 °C to +85 °C	28-pin PLCC	DG407BDN-T1-E3
	28-pin widebody SOIC	DG407BDW-E3, DG407BDW-T1-E3



ABSOLUTE MAXIMUM RATINGS			
PARAMETER		LIMIT	UNIT
Voltages referenced to V-	V+ to V- <sup>e</sup>	44	V
	GND to V-	-25	
Digital inputs <sup>a</sup> , V <sub>S</sub> , V <sub>D</sub>		(V-) - 2 to (V+) + 2 or 20 mA, whichever occurs first	
Current (any terminal)		30	mA
Peak current, S or D (pulsed at 1 ms, 10 % duty cycle max.)		100	
Storage temperature		-65 to +150	°C
Power dissipation (package) <sup>b</sup>	28-pin plastic PLCC <sup>c</sup>	450	mW
	28-pin widebody SOIC <sup>d</sup>	450	mW

**Notes**

- a. Signals on S<sub>X</sub>, D<sub>X</sub> or I<sub>NX</sub> exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings
- b. All leads soldered or welded to PC board
- c. Derate 8.3 mW/°C above 75 °C
- d. Derate 6 mW/°C above 75 °C
- e. Also applies when V- = GND

SPECIFICATIONS							
PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE SPECIFIED	TEMP. <sup>b</sup>	TYP. <sup>c</sup>	D SUFFIX -40 °C to +85 °C		UNIT
					MIN. <sup>d</sup>	MAX. <sup>d</sup>	
<b>Analog Switch</b>							
Analog signal range <sup>e</sup>	V <sub>ANALOG</sub>		Full	-	-15	15	V
Drain-source on-resistance	R <sub>DS(on)</sub>	V <sub>D</sub> = ± 10 V, I <sub>S</sub> = -10 mA sequence each switch on	Room	45	-	60	Ω
			Full	45	-	74	
R <sub>DS(on)</sub> matching between channels <sup>g</sup>	ΔR <sub>DS(on)</sub>	V <sub>D</sub> = ± 10 V	Room	5	-	-	%
Source off leakage current	I <sub>S(off)</sub>	V <sub>S</sub> = ± 10 V, V <sub>D</sub> = ± 10 V, V <sub>EN</sub> = 0 V	Room	-	-0.5	0.5	nA
			Full	-	-5	5	
Drain off leakage current	DG406B	V <sub>D</sub> = ± 10 V, V <sub>S</sub> = ± 10 V, V <sub>EN</sub> = 0 V	Room	-	-1	1	
			Full	-	-40	40	
	DG407B		Room	-	-1	1	
			Full	-	-20	20	
Drain on leakage current	DG406B	V <sub>S</sub> = V <sub>D</sub> = ± 10 V sequence each switch on	Room	-	-1	1	
			Full	-	-40	40	
	DG407B		Room	-	-1	1	
			Full	-	-20	20	
<b>Digital Control</b>							
Logic high input voltage	V <sub>INH</sub>		Full	-	2.4	-	V
Logic low input voltage	V <sub>INL</sub>		Full	-	-	0.8	
Logic high input current	I <sub>AH</sub>	V <sub>A</sub> = 2.4 V, 15 V	Full	-	-1	1	μA
Logic low input current	I <sub>AL</sub>	V <sub>EN</sub> = 0 V, 2.4 V, V <sub>A</sub> = 0 V	Full	-	-1	1	
Logic input capacitance	C <sub>in</sub>	f = 1 MHz	Room	6	-	-	pF



SPECIFICATIONS								
PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE SPECIFIED		TEMP. <sup>b</sup>	TYP. <sup>c</sup>	D SUFFIX -40 °C to +85 °C		UNIT
		V <sub>+</sub> = 15 V, V <sub>-</sub> = -15 V				MIN. <sup>d</sup>	MAX. <sup>d</sup>	
		V <sub>AL</sub> = 0.8 V, V <sub>AH</sub> = 2.4 V <sup>f</sup>						
<b>Dynamic Characteristics</b>								
Transition time	t <sub>TRANS</sub>	see figure 2	Room	115	-	148	ns	
			Full	-	-	161		
Break-before-make interval	t <sub>OPEN</sub>	see figure 4	Room	39	10	-		
			Full	-	21	-		
Enable turn-on time	t <sub>ON(EN)</sub>	see figure 3	Room	75	-	107		
			Full	-	-	123		
Enable turn-off time	t <sub>OFF(EN)</sub>		Room	50	-	88		
			Full	-	-	94		
Charge injection	Q	C <sub>L</sub> = 1 nF, V <sub>S</sub> = 0 V, R <sub>S</sub> = 0 Ω	Room	11	-	-	pC	
Off isolation <sup>h</sup>	OIRR	V <sub>EN</sub> = 0 V, R <sub>L</sub> = 50 Ω, f = 1 MHz	Room	-86	-	-	dB	
Source off capacitance	C <sub>S(off)</sub>	V <sub>EN</sub> = 0 V, V <sub>S</sub> = 0 V, f = 1 MHz	Room	6	-	-	pF	
Drain off capacitance	DG406B	V <sub>EN</sub> = 0 V, V <sub>D</sub> = 0 V, f = 1 MHz	Room	108	-	-		
	DG407B		Room	54	-	-		
Drain on capacitance	DG406B		Room	114	-	-		
	DG407B		Room	57	-	-		
<b>Power Supplies</b>								
Positive supply current	I <sub>+</sub>	V <sub>EN</sub> = V <sub>A</sub> = 0 V or 5 V	Room	23	-	30	μA	
			Full	-	-	75		
Negative supply current	I <sub>-</sub>		Room	-0.02	-1	-		
			Full	-	-10	-		
Positive supply current	I <sub>+</sub>	V <sub>EN</sub> = 2.4 V, V <sub>A</sub> = 0 V	Room	28	-	500		
			Full	-	-	700		
Negative supply current	I <sub>-</sub>		Room	-0.01	-20	-		
			Full	-	-20	-		

**Notes**

- a. Guaranteed by ± 15 V leakage test, not production tested
- b. Room = 25 °C, full = as determined by the operating temperature suffix
- c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing
- d. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this datasheet
- e. Guaranteed by design, not subject to production test
- f. V<sub>IN</sub> = input voltage to perform proper function
- g. ΔR<sub>DS(on)</sub> = R<sub>DS(on)</sub> max. - R<sub>DS(on)</sub> min.
- h. Worst case isolation occurs on channel 4 due to proximity to the drain pin



SPECIFICATIONS (single supply)									
PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE SPECIFIED		TEMP. <sup>b</sup>	TYP. <sup>c</sup>	D SUFFIX -40 °C to +85 °C		UNIT	
		V <sub>+</sub> = 15 V, V <sub>-</sub> = -15 V				MIN. <sup>d</sup>	MAX. <sup>d</sup>		
		V <sub>AL</sub> = 0.8 V, V <sub>AH</sub> = 2.4 V <sup>f</sup>							
<b>Analog Switch</b>									
Analog signal range <sup>e</sup>	V <sub>ANALOG</sub>			Full	-	0	12	V	
Drain-source on-resistance	R <sub>DS(on)</sub>	V <sub>D</sub> = 3 V, I <sub>S</sub> = -1 mA sequence each switch on		Room	78	-	100	Ω	
R <sub>DS(on)</sub> matching between channels <sup>g</sup>	ΔR <sub>DS(on)</sub>			Room	5	-	-	%	
Source off leakage current <sup>a</sup>	I <sub>S(off)</sub>	V <sub>D</sub> = 10 V or 0.5 V, V <sub>S</sub> = 0.5 V or 10 V, V <sub>EN</sub> = 0 V		Room	-	-0.5	0.5	nA	
Drain off leakage current	DG406B			I <sub>D(off)</sub>	Room	-	-1		1
	DG407B			I <sub>D(off)</sub>	Room	-	-1		1
Drain on leakage current	DG406B			I <sub>D(on)</sub>	V <sub>S</sub> = V <sub>D</sub> = ± 10 V sequence each switch on		Room		-
	DG407B	Room	-				-1	1	
<b>Dynamic Characteristics</b>									
Transition time	t <sub>TRANS</sub>	V <sub>S1</sub> = 8 V, V <sub>S8</sub> = 0 V, V <sub>IN</sub> = 2.4 V		Room	130	-	163	ns	
Enable turn-on time	t <sub>ON(EN)</sub>	V <sub>INH</sub> = 2.4 V, V <sub>INL</sub> = 0 V, V <sub>IN</sub> = 5 V		Room	93	-	125		
Enable turn-off time	t <sub>OFF(EN)</sub>			Room	63	-	94		
Charge injection	Q	C <sub>L</sub> = 1 nF, V <sub>S</sub> = 6 V, R <sub>S</sub> = 0 Ω		Room	9	-	-	pC	
<b>Power Supplies</b>									
Positive supply current	I <sub>+</sub>	V <sub>EN</sub> = 0 V or 5 V, V <sub>A</sub> = 0 V or 5 V		Room	13	-	30	μA	
				Full	-	-	75		
Positive supply current	I <sub>+</sub>			Room	-0.01	-20	-		
				Full	-	-20	-		

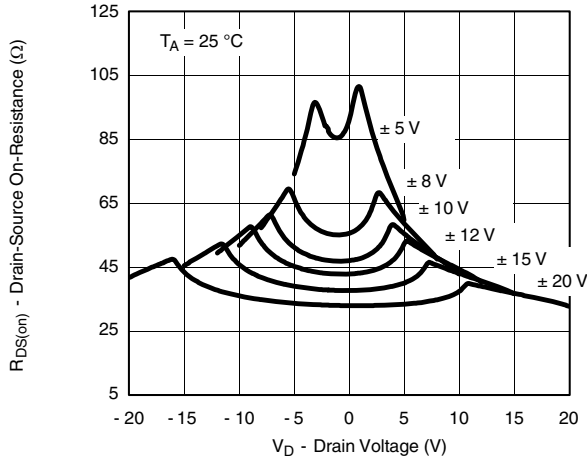
**Notes**

- Guaranteed by ± 15 V leakage test, not production tested
- Room = 25 °C, full = as determined by the operating temperature suffix
- Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing
- The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this datasheet
- Guaranteed by design, not subject to production test
- V<sub>IN</sub> = input voltage to perform proper function
- ΔR<sub>DS(on)</sub> = R<sub>DS(on)</sub> max. - R<sub>DS(on)</sub> min.
- Worst case isolation occurs on channel 4 due to proximity to the drain pin

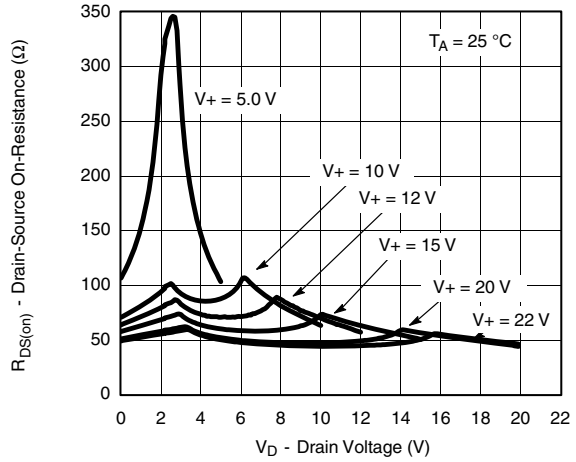
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



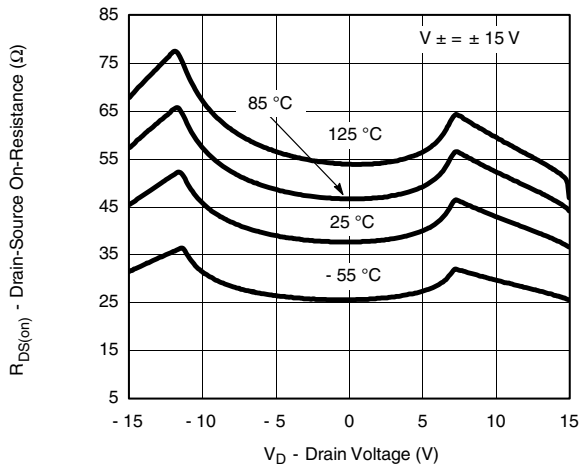
**TYPICAL CHARACTERISTICS** ( $T_A = 25\text{ }^\circ\text{C}$ , unless otherwise noted)



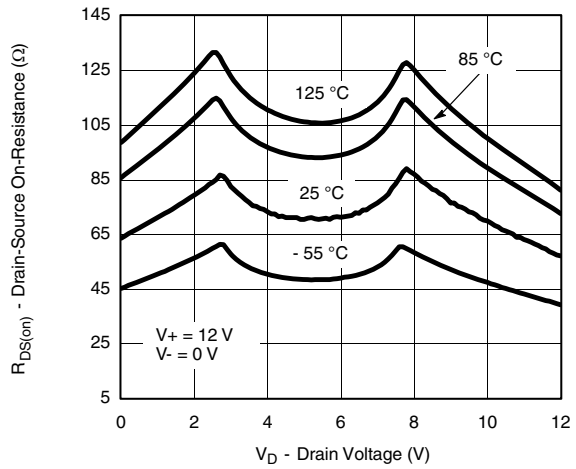
**On-Resistance vs.  $V_D$  and Dual Supply Voltage**



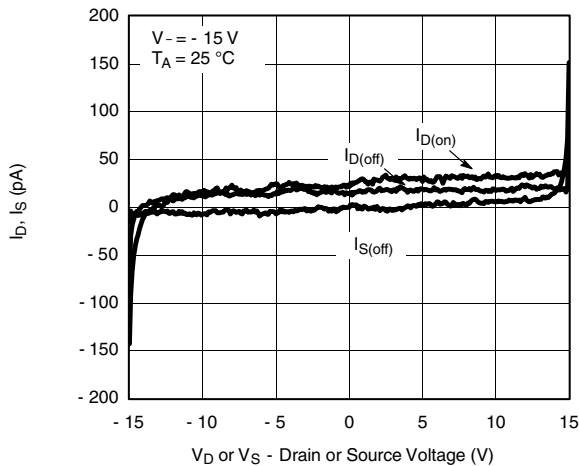
**On-Resistance vs.  $V_D$  and Unipolar Supply Voltage**



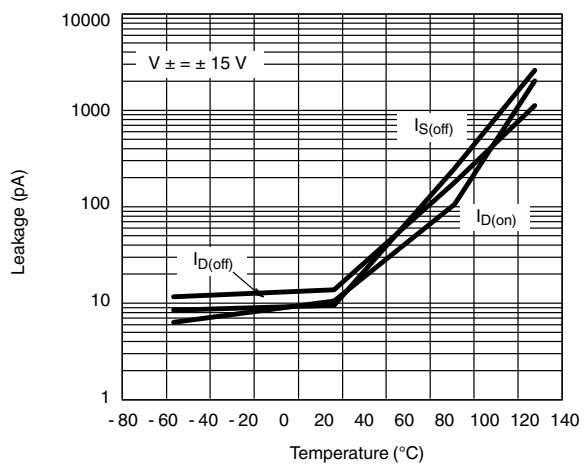
**On-Resistance vs.  $V_D$  and Temperature**



**On-Resistance vs.  $V_D$  and Temperature**



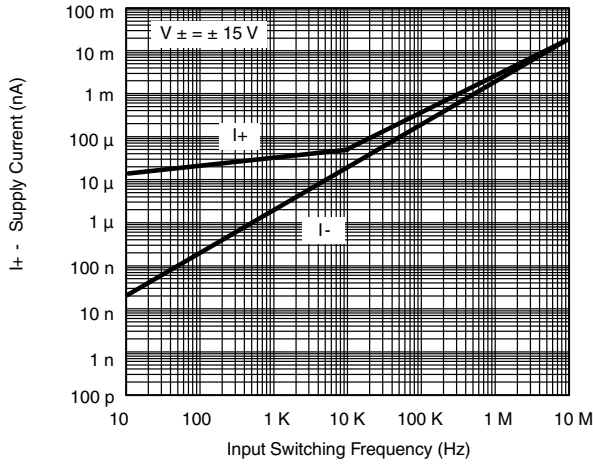
**Leakage vs. Analog Voltage**



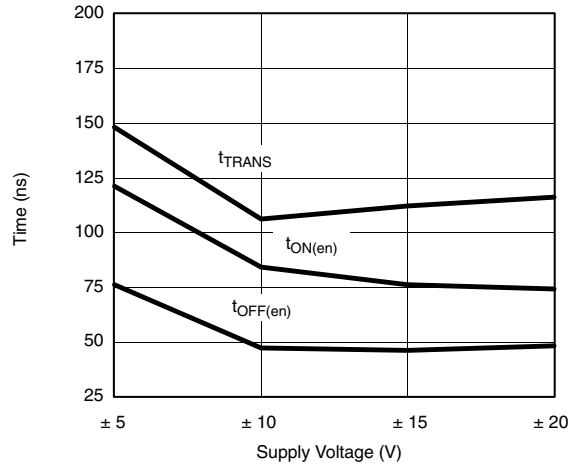
**Leakage vs. Current**



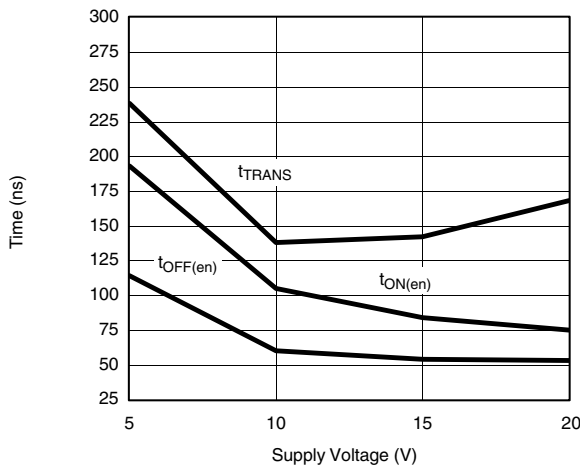
**TYPICAL CHARACTERISTICS** ( $T_A = 25\text{ }^\circ\text{C}$ , unless otherwise noted)



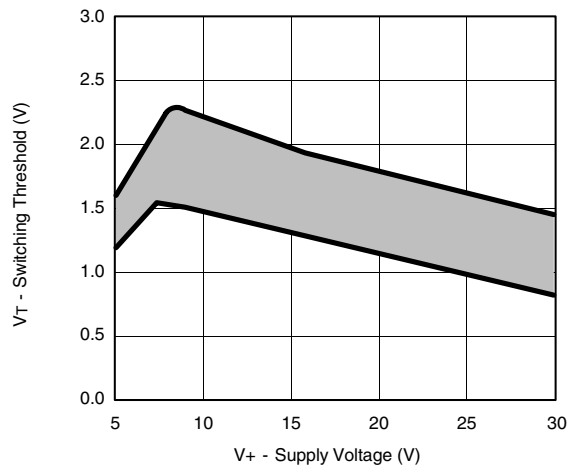
**Supply Current vs. Input Switching Frequency**



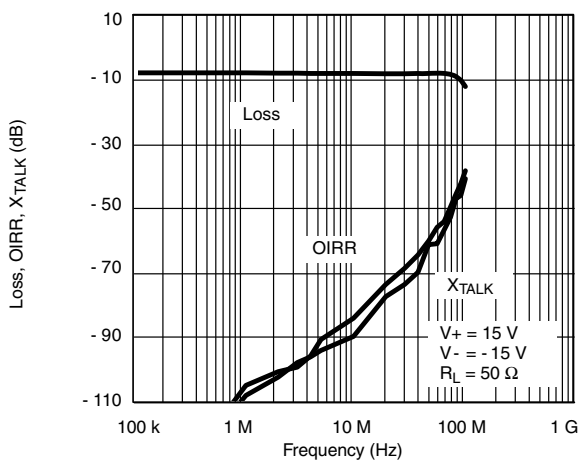
**Switching Time vs. Bipolar Supplies**



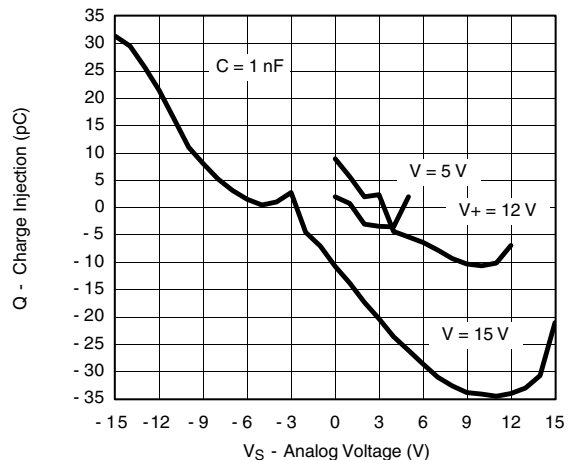
**Switching Time vs. Single Supplies**



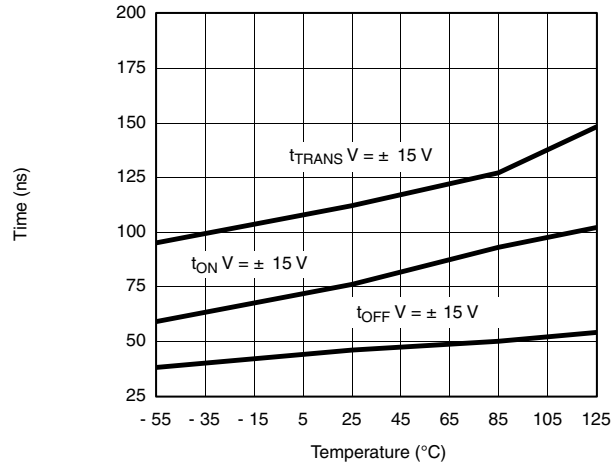
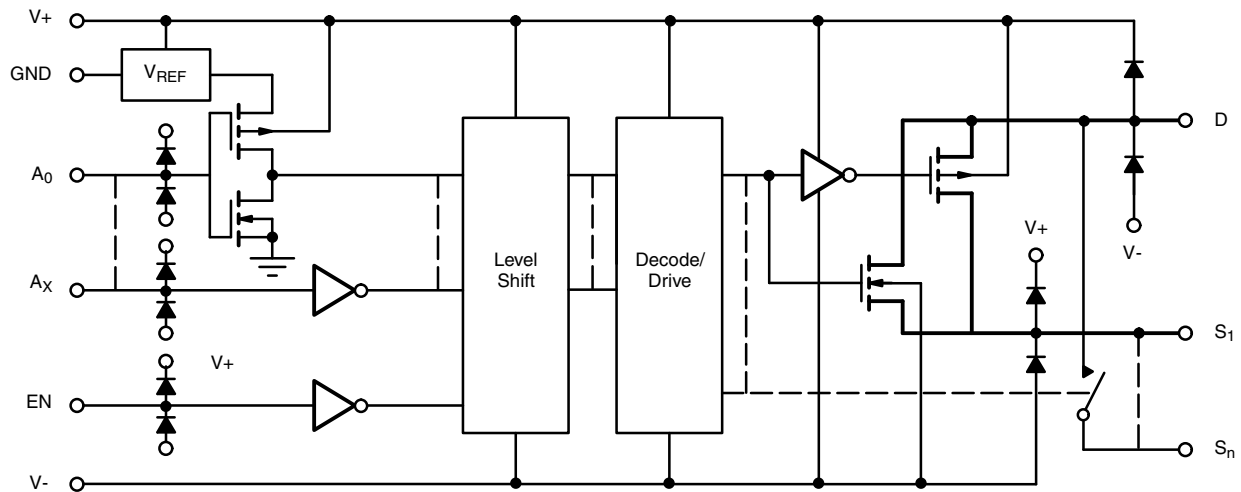
**Switching Threshold vs. Supply Voltage**



**Insertion Loss, Off-Isolation Crosstalk vs. Frequency**

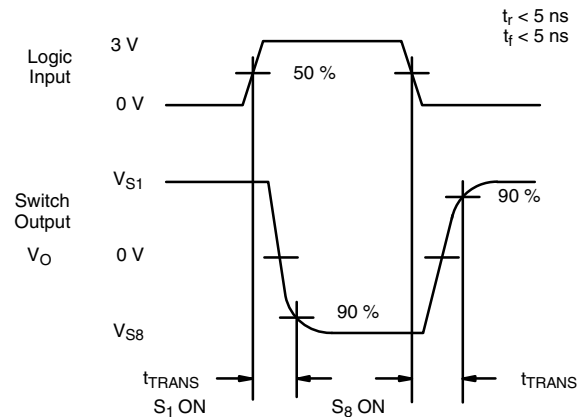
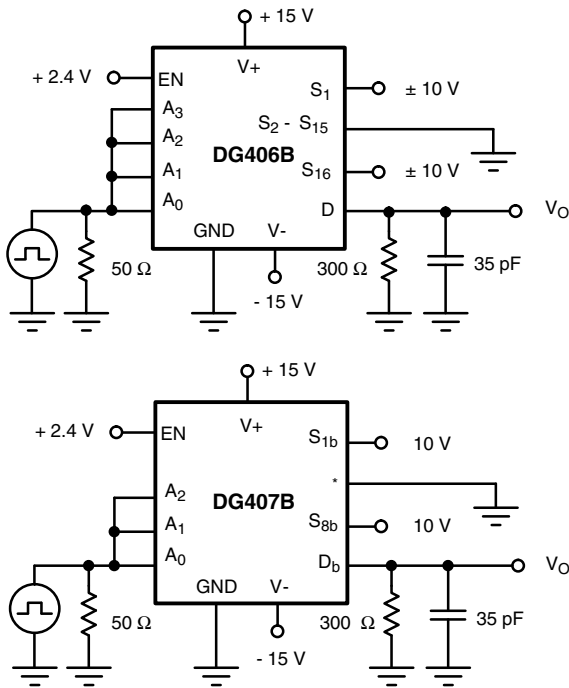


**Charge Injection vs. Analog Voltage**

**TYPICAL CHARACTERISTICS** ( $T_A = 25\text{ }^\circ\text{C}$ , unless otherwise noted)

**Switching Time vs. Temperature**
**SCHEMATIC DIAGRAM** (typical channel)

**Fig. 1**



TEST CIRCUITS



\* = S<sub>1a</sub> - S<sub>8a</sub>, S<sub>2b</sub> - S<sub>7b</sub>, D<sub>a</sub>

Fig. 2 - Transition Time

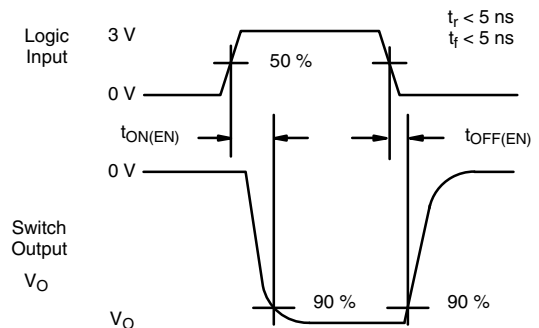
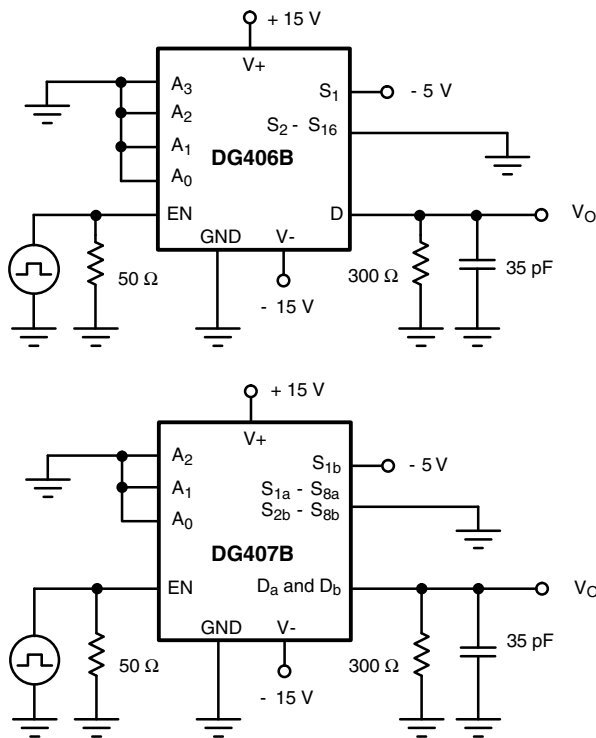
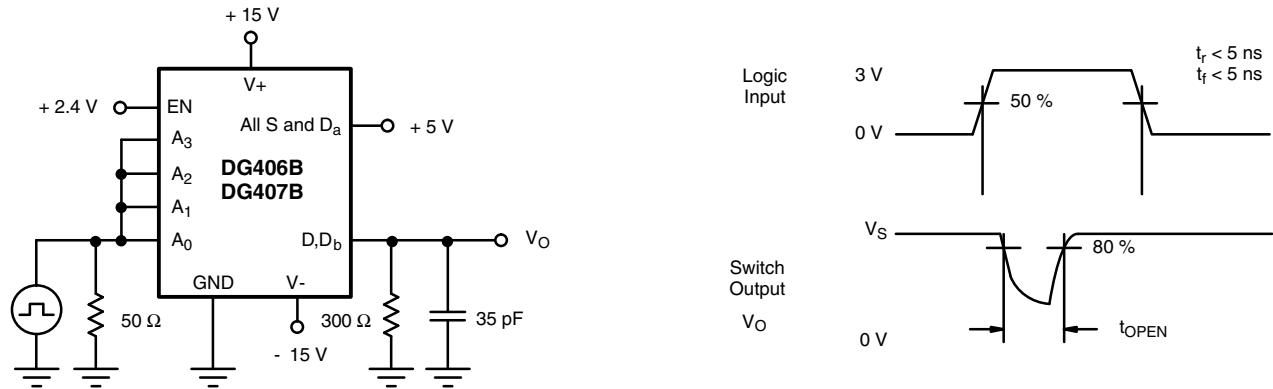


Fig. 3 - Enable Switching Time

**TEST CIRCUITS**

**Fig. 4 - Break-Before-Make Interval**

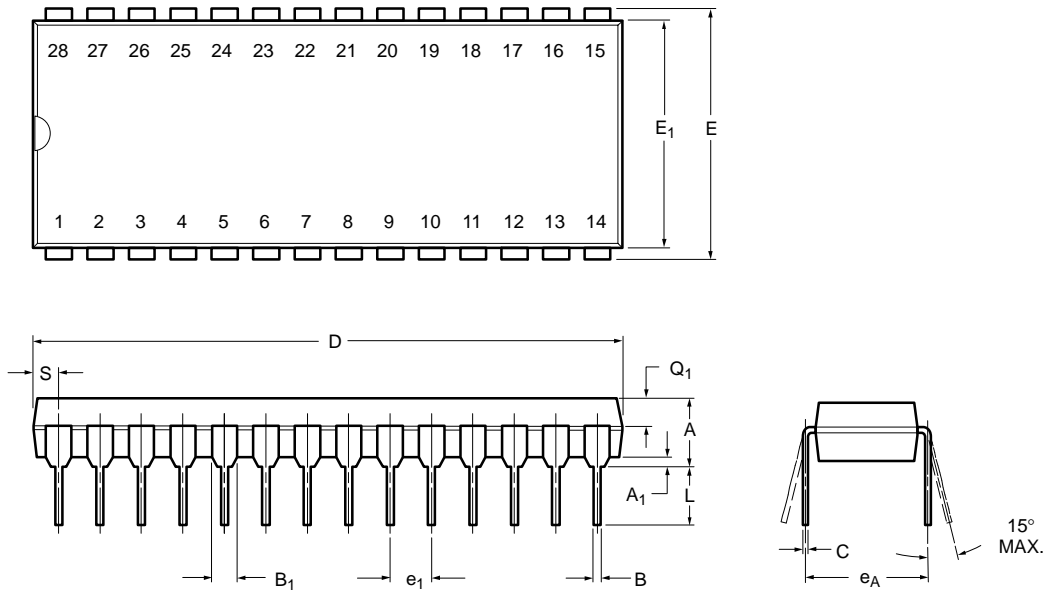


PRODUCT SUMMARY				
Part number	DG406B	DG406B	DG407B	DG407B
Status code	2	2	2	2
Configuration	16:1 x 1	16:1 x 1	8:1 x 2	8:1 x 2
Single supply min. (V)	5	5	5	5
Single supply max. (V)	40	40	40	40
Dual supply min. (V)	5	5	5	5
Dual supply max. (V)	20	20	20	20
On-resistance ( $\Omega$ )	45	45	45	45
Charge injection (pC)	11	11	11	11
Source on capacitance (pF)	114	114	57	57
Source off capacitance (pF)	6	6	6	6
Leakage switch on typ. (nA)	-	-	-	-
Leakage switch off max. (nA)	0.5	0.5	0.5	0.5
-3 dB bandwidth (MHz)	-	-	-	-
Package	PLCC-28	SO-28 (wide)	PLCC-28	SO-28 (wide)
Functional circuit / applications	Multi purpose, instrumentation, medical and healthcare	Multi purpose, instrumentation, medical and healthcare	Multi purpose, instrumentation, medical and healthcare	Multi purpose, instrumentation, medical and healthcare
Interface	Parallel	Parallel	Parallel	Parallel
Single supply operation	Yes	Yes	Yes	Yes
Dual supply operation	Yes	Yes	Yes	Yes
Turn on time max. (ns)	148	148	148	148
Crosstalk and off isolation	-86	-86	-86	-86

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see [www.vishay.com/ppg?72552](http://www.vishay.com/ppg?72552).



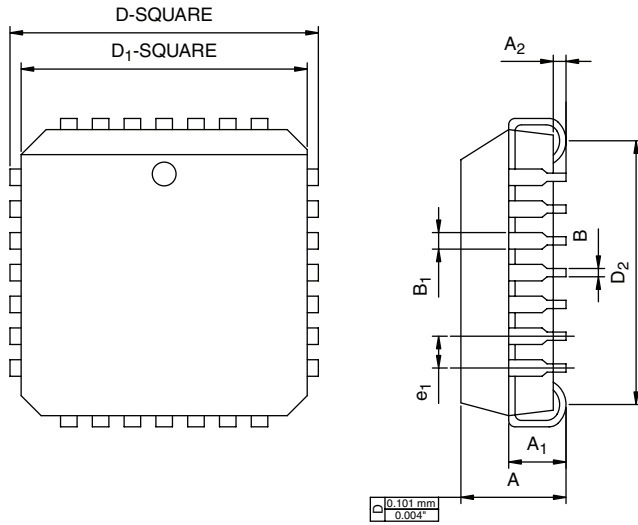
**PDIP: 28-LEAD**



Dim	MILLIMETERS		INCHES	
	Min	Max	Min	Max
<b>A</b>	2.29	5.08	0.090	0.200
<b>A<sub>1</sub></b>	0.39	1.77	0.015	0.070
<b>B</b>	0.38	0.56	0.015	0.022
<b>B<sub>1</sub></b>	0.89	1.65	0.035	0.065
<b>C</b>	0.204	0.30	0.008	0.012
<b>D</b>	35.10	39.70	1.380	1.565
<b>E</b>	15.24	15.88	0.600	0.625
<b>E<sub>1</sub></b>	13.21	14.73	0.520	0.580
<b>e<sub>1</sub></b>	2.29	2.79	0.090	0.110
<b>e<sub>A</sub></b>	14.99	15.49	0.590	0.610
<b>L</b>	2.60	5.08	0.100	0.200
<b>Q<sub>1</sub></b>	0.95	2.345	0.0375	0.0925
<b>S</b>	0.995	2.665	0.0375	0.105

ECN: S-03946—Rev. F, 09-Jul-01  
DWG: 5488

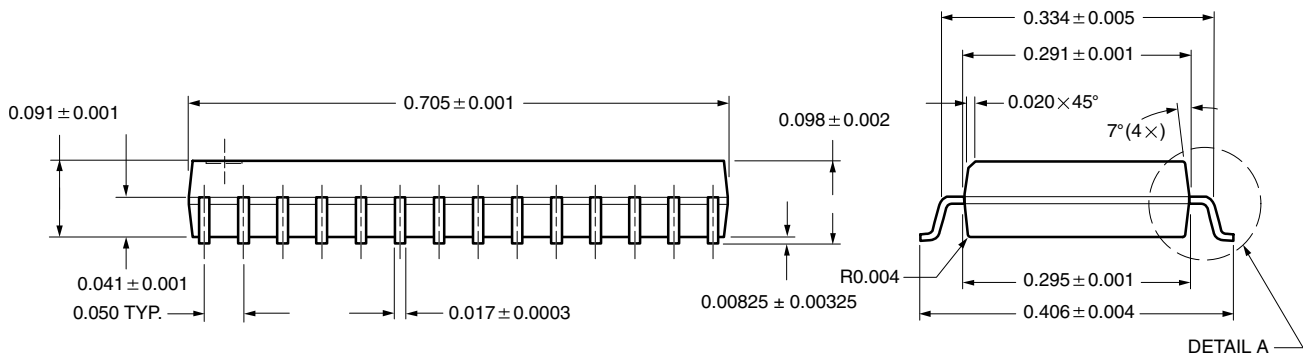
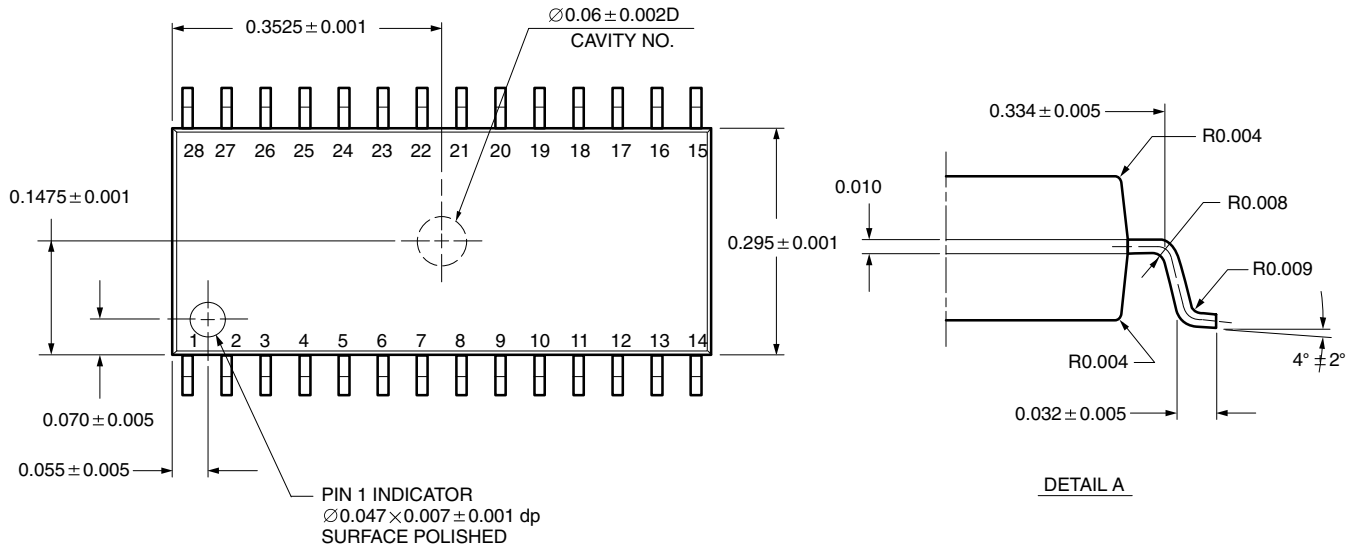
## PLCC: 28-LEAD



DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	4.20	4.57	0.165	0.180
A <sub>1</sub>	2.29	3.04	0.090	0.120
A <sub>2</sub>	0.51	-	0.020	-
B	0.331	0.553	0.013	0.021
B <sub>1</sub>	0.661	0.812	0.026	0.032
D	12.32	12.57	0.485	0.495
D <sub>1</sub>	11.430	11.582	0.450	0.456
D <sub>2</sub>	9.91	10.92	0.390	0.430
e <sub>1</sub>	1.27 BSC		0.050 BSC	
ECN: T09-0766-Rev. D, 28-Sep-09 DWG: 5491				



### SOIC (WIDE-BODY): 28-LEADS



All Dimensions In Inches

ECN: E11-2209-Rev. D, 01-Aug-11  
DWG: 5850



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