

# SN74HC4852 Dual 4-to-1 Channel Analog Multiplexer/Demultiplexer With Injection-Current Effect Control

## 1 Features

- Injection current cross-coupling <math><1\text{mV/mA}</math> (see [Figure 8-1](#))
- Low crosstalk between switches
- Pin compatible with SN74HC4052, SN74LV4052A, and CD4052B
- 2V to 5.5V  $V_{CC}$  operation
- Latch-up performance exceeds 100mA per JESD 78, Class II

## 2 Applications

- Analog signal switching or multiplexing:
  - Signal gating, modulator, squelch control, demodulator, chopper, commutating switch
- Digital signal switching and multiplexing
  - Audio and video signal routing
- Transmission-gate logic implementation
- Analog-to-digital and digital-to-analog conversion
- Digital control of frequency, impedance, phase, and analog-signal gain
- Motor speed control
- Battery chargers
- DC-DC converter

## 3 Description

This dual 4-to-1 CMOS analog multiplexer/demultiplexer is pin compatible with the 4052 function and also features injection-current effect control. This feature has excellent value in automotive applications where voltages in excess of normal supply voltages are common.

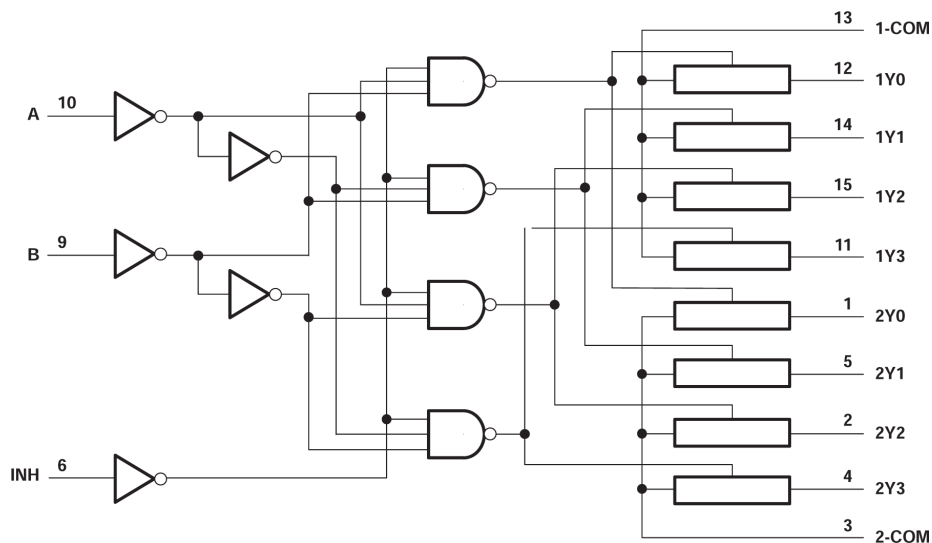
The injection-current effect control allows signals at disabled analog input channels to exceed the supply voltage without affecting the signal of the enabled analog channel. This eliminates the need for external diode/resistor networks typically used to keep the analog channel signals within the supply voltage range.

### Package Information

PART NUMBER	PACKAGE <sup>(1)</sup>	PACKAGE SIZE <sup>(2)</sup>
SN74HC4852	PW (TSSOP, 16)	5mm × 6.4mm

(1) For more information, see [Section 11](#).

(2) The package size (length × width) is a nominal value and includes pins, where applicable.



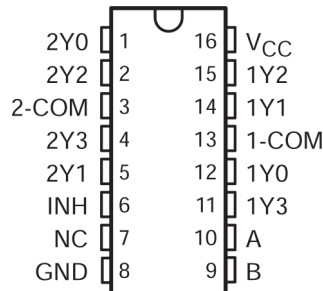
Functional Diagram



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## 4 Pin Configuration and Functions



NC – No internal connection

Figure 4-1. PW Package, 16-Pin TSSOP (Top View)

Table 4-1. Function Table

INPUTS			ON CHANNEL
INH	B	A	
L	L	L	1Y0, 2Y0
L	L	H	1Y1, 2Y1
L	H	L	1Y2, 2Y2
L	H	H	1Y3, 2Y3
H	X	X	None

## 5 Specifications

### 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1) (2)</sup>

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage	-0.5	6	V
V <sub>SEL</sub> or V <sub>EN</sub>	Logic control input pin voltage (EN, A0, A1, A2)	-0.5	V <sub>CC</sub> +0.5V	V
V <sub>S</sub> or V <sub>D</sub>	Source or drain voltage (Sx, D)	-0.5	V <sub>CC</sub> +0.5V	V
I <sub>IK</sub>	Input clamp current (V <sub>I</sub> < 0 or V <sub>I</sub> > V <sub>CC</sub> )	-20	20	mA
I <sub>IOK</sub>	I/O diode current (V <sub>IO</sub> < 0 or V <sub>IO</sub> > V <sub>CC</sub> )	-20	20	mA
I <sub>T</sub>	Switch through current (V <sub>IO</sub> = 0 to V <sub>CC</sub> )	-25	25	mA
I <sub>GND</sub>	Continuous current through V <sub>CC</sub> or GND	-50	50	mA
T <sub>stg</sub>	Storage temperature	-65	150	°C
T <sub>J</sub>	Junction temperature		150	

- (1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If briefly operating outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime.
- (2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

### 5.2 ESD Ratings

			VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human body model (HBM), per AEC Q100-002 <sup>(1)</sup>	±2000	V
		Charged device model (CDM), per AEC Q100-011	±750	

- (1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

### 5.3 Thermal Information: SN74HC485x

THERMAL METRIC <sup>(1)</sup>		SN74HC485x	UNIT
		PW (TSSOP)	
		PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	139.6	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 5.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V <sub>CC</sub>	Supply voltage		2		5.5	V
V <sub>IH</sub>	Input logic high	2V	1.5			V
		2.5V	2.1			
		3.3V	2.3			
		4.5V	3.15			
		5.5V	4.2			
V <sub>IL</sub>	Input logic low	2V	0		0.5	V
		2.5V	0		0.7	
		3.3V	0		0.8	
		4.5V	0		0.95	
		5.5V	0		1.05	
V <sub>SEL</sub> or V <sub>EN</sub>	Logic control input pin voltage ( $\overline{\text{EN}}$ , A0, A1, A2)		0		V <sub>CC</sub>	V
V <sub>S</sub> or V <sub>D</sub>	Signal path input/output voltage (source or drain pin) (Sx, D)		0		V <sub>CC</sub>	V
$\Delta t/\Delta v$	Input transition rise or fall time	V <sub>CC</sub> = 2V			1000	ns
		V <sub>CC</sub> = 3V			800	
		V <sub>CC</sub> = 3.3V			700	
		V <sub>CC</sub> = 4.5V			500	
		V <sub>CC</sub> = 5.5V			400	
T <sub>A</sub>	Ambient temperature		-40		125	°C

## 5.5 Electrical Characteristics

At specified  $V_{CC} \pm 10\%$

Typical values measured at nominal  $V_{CC}$ .

PARAMETER		TEST CONDITIONS	$V_{CC}$	Operating free-air temperature ( $T_A$ )									UNIT
				25°C			–40°C to 85°C			–40°C to 125°C			
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
$R_{ON}$	On-state switch resistance	$V_S = 0V$ to $V_{CC}$ $I_{SD} = 0.5mA$	2V	500	650		670		700			$\Omega$	
			3V	215	280		320		360				
			3.3V	210	270		305		345				
			4.5V	160	210		240		270				
$\Delta_{RON}$	On-state switch resistance matching between inputs	$V_S = V_{CC} / 2$ $I_{SD} = 0.5mA$	2V	4	18		22		24		$\Omega$		
			3V	2	12		14		16				
			3.3V	2	12		14		16				
			4.5V	2	8		12		16				
$I_I$	Control input current	$V_I = V_{CC}$ or GND	5V		$\pm 0.1$		$\pm 0.1$		$\pm 1$	$\mu A$			
$I_{S(OFF)}$	Off-state switch leakage current (any one channel)	Switch Off $V_{INH} = V_{IH}$ $V_D = V_{CC} / GND$ $V_S = GND / V_{CC}$	5V		$\pm 0.1$		$\pm 0.5$		$\pm 1$	$\mu A$			
	Off-state switch leakage current (common channel)				$\pm 0.2$		$\pm 2$		$\pm 4$	$\mu A$			
$I_{S(ON)}$	Channel on-state leakage current	Switch Off $V_{INH} = V_{IL}$ $V_D = V_{CC} / GND$ $V_S = GND / V_{CC}$	5V		$\pm 0.1$		$\pm 0.5$		$\pm 1$	$\mu A$			
$I_{DD}$	$V_{CC}$ supply current	Logic inputs = 0V or $V_{CC}$	5V		2		5		10	$\mu A$			
$C_{IC}$	Control input capacitance	A, B, C, INH		3.5	10		10		10	pF			
$C_{IS}$	Common terminal capacitance	Switch off		22	40		40		40	pF			
$C_{OS}$	Switch terminal capacitance	Switch off		6.7	15		15		15	pF			
$C_{PD}$	Power Dissipation Capacitance	No Load $t_r = t_f = 1ns$ $f = 1MHz$	3.3V	32						pF			
			5V	37									

## 5.6 Timing Characteristics

At specified  $V_{CC} \pm 10\%$

Typical values measured at nominal  $V_{CC}$ .

PARAMETER	TEST CONDITIONS	$V_{CC}$	Operating free-air temperature ( $T_A$ )									UNIT
			25°C			-40°C to 85°C			-40°C to 125°C			
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
SWITCHING CHARACTERISTICS <sup>(1)</sup>												
$t_{PD}$	Propagation delay	$C_L = 50\text{pF}$ Sx to D, D to Sx	2V	7	19.5	33	6	34	6	35	ns	
			3V	3.6	12	16.5	2.5	18	2.5	19.5		
			3.3V	3.9	11	15	2.5	16.5	2.5	18.5		
			5V	2.3	8.6	11.6	2.1	12.5	2	13.5		
$t_{TRAN}$	Transition-time between inputs	$R_L = 10\text{k}\Omega$ , $C_L = 50\text{pF}$ Ax to D, Ax to Sx	2V	19.6	44	94	15.4	103	13.8	103	ns	
			3V	12.4	30	63	9.3	67	8.2	67		
			3.3V	11.4	23	51	8.5	54	7.5	54		
			5V	9.3	18	43	6.5	46	5.6	46		
$t_{ON(EN)}$	Turnon-time from enable	$R_L = 10\text{k}\Omega$ , $C_L = 50\text{pF}$ EN to D, EN to Sx	2V	15	39	64	13.8	75	12.5	75	ns	
			3V	7.9	30	45	6.2	50	5.5	55		
			3.3V	7	26.5	42.5	6.4	47.5	5.4	52.5		
			5V	4	24	40	4.3	45	3.4	50		
$t_{OFF(EN)}$	Turnoff time from enable	$R_L = 10\text{k}\Omega$ , $C_L = 50\text{pF}$ EN to D, EN to Sx	2V	26	48.4	100	25	105	25	115	ns	
			3V	15	21	90	14	100	14	110		
			3.3V	12	15	85	11	95	11	105		
			5V	24.5	41.4	80	24.2	90	24	100		

(1)  $t_{PLH}/t_{PHL} = t_{PD}$  propagation delay time,  $t_{PZH}/t_{PLZ} = t_{ON(EN)}$  enable delay time,  $t_{PHZ}/t_{PLZ} = t_{OFF(EN)}$  disable delay time,  $t_{PLH}/t_{PHL}$  Channel select =  $t_{TRAN}$

## 5.7 Injection Current Coupling

At specified  $V_{CC} \pm 10\%$

Typical values measured at nominal  $V_{CC}$  and  $T_A = 25^\circ\text{C}$ .

PARAMETER	$V_{CC}$	TEST CONDITIONS	-40°C to 125°C			UNIT	
			MIN	TYP	MAX		
INJECTION CURRENT COUPLING							
$\Delta V_{OUT}$	Maximum shift of output voltage of enabled analog input <sup>(1)</sup>	3.3V	$R_S \leq 3.9\text{k}\Omega$	$I_{INJ} \leq 1\text{mA}$	0.05	1	mV
		5V			0.1	1	
		3.3V		$I_{INJ} \leq 10\text{mA}$	0.345	5	
		5V			0.067	5	
		3.3V	$R_S \leq 20\text{k}\Omega$	$I_{INJ} \leq 1\text{mA}$	0.05	2	
		5V			0.11	2	
		3.3V		$I_{INJ} \leq 10\text{mA}$	0.05	20	
		5V			0.024	20	

(1)  $I_{INJ}$  = total current injected into all disabled channels

## 6 Parameter Measurement Information

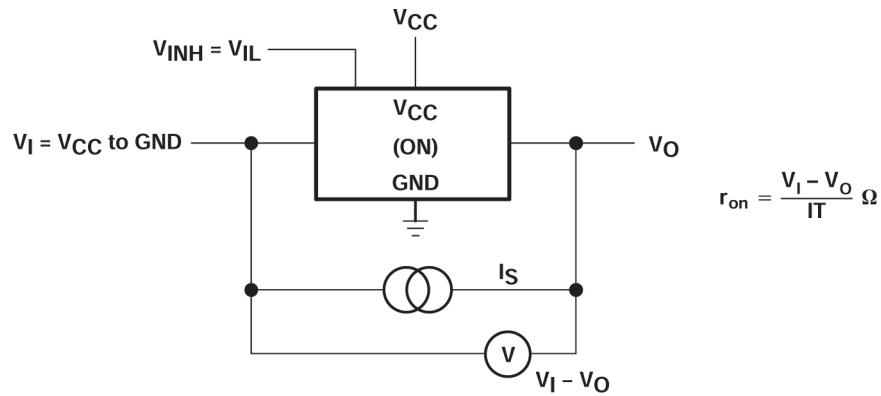


Figure 6-1. On-State Resistance Test Circuit

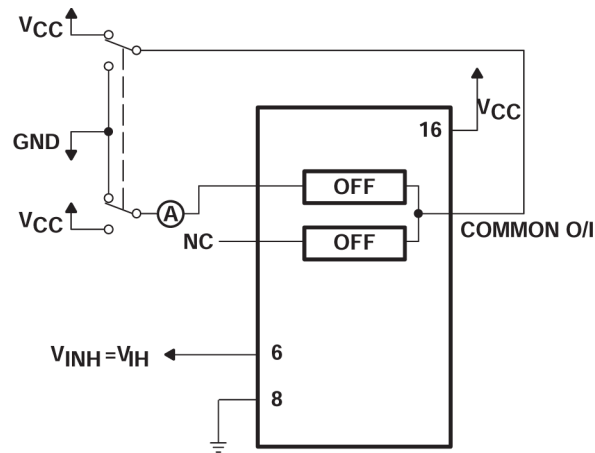


Figure 6-2. Maximum Off-Channel Leakage Current, Any One Channel, Test Setup

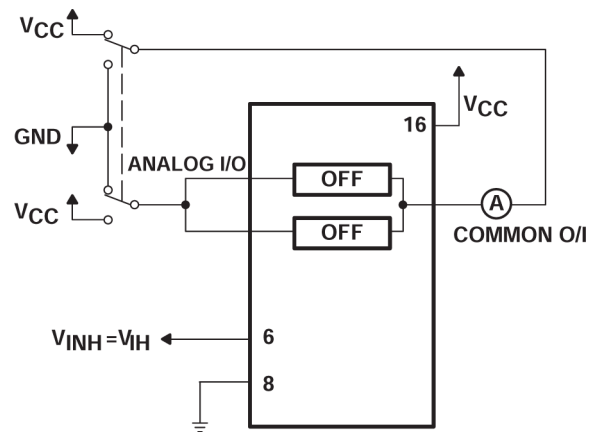


Figure 6-3. Maximum Off-Channel Leakage Current, Common Channel, Test Setup

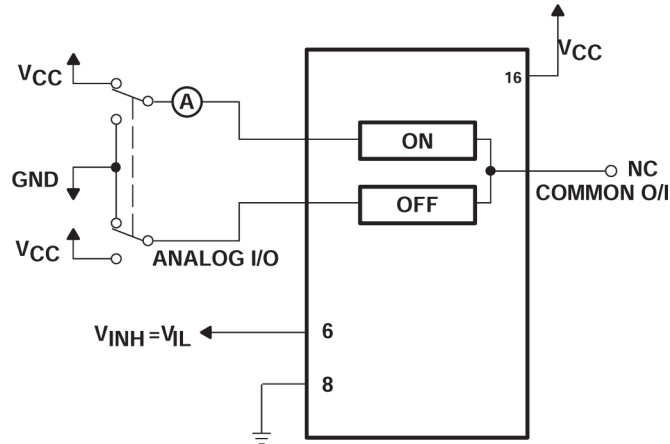


Figure 6-4. Maximum On-Channel Leakage Current, Channel to Channel, Test Setup

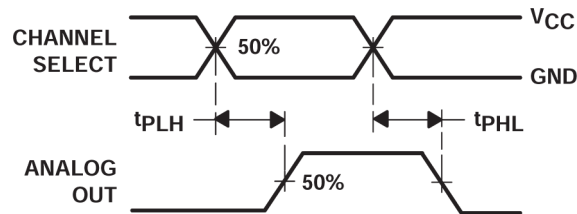


Figure 6-5. Propagation Delays, Channel Select to Analog Out

†

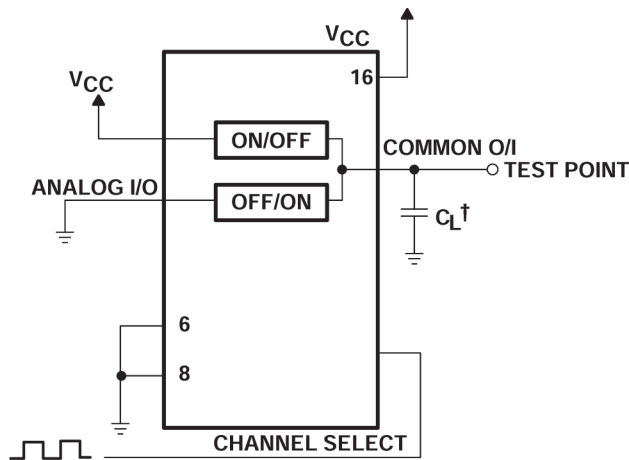


Figure 6-6. Propagation Delay, Channel Select to Analog Out, Test Setup

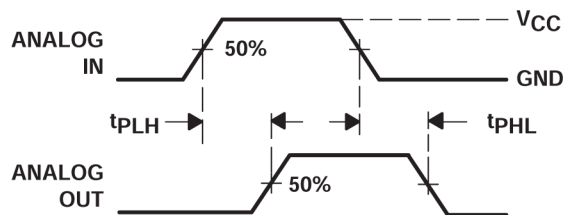


Figure 6-7. Propagation Delays, Analog in to Analog Out

† Includes all probe and jig capacitance



†

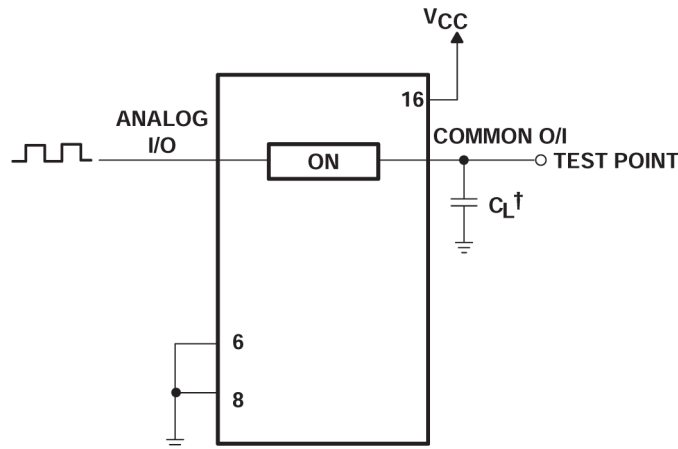


Figure 6-8. Propagation Delay, Analog in to Analog Out, Test Setup

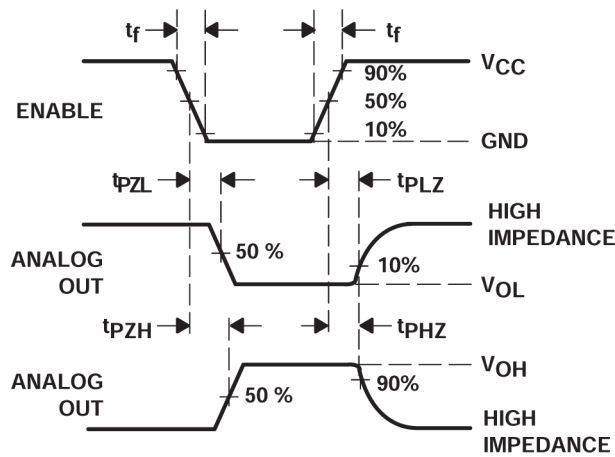


Figure 6-9. Propagation Delays, Enable to Analog Out

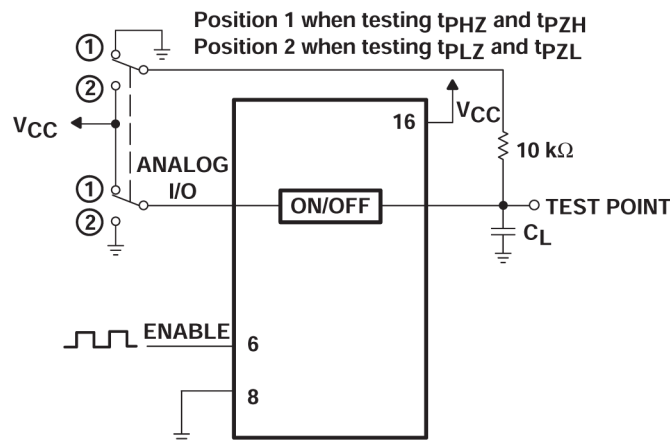


Figure 6-10. Propagation Delay, Enable to Analog Out, Test Setup

† Includes all probe and jig capacitance

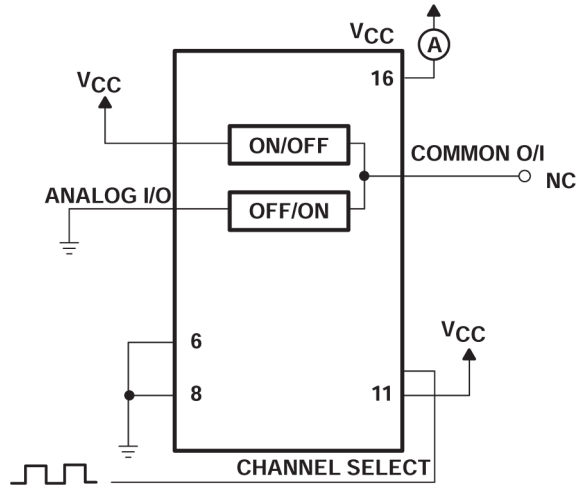
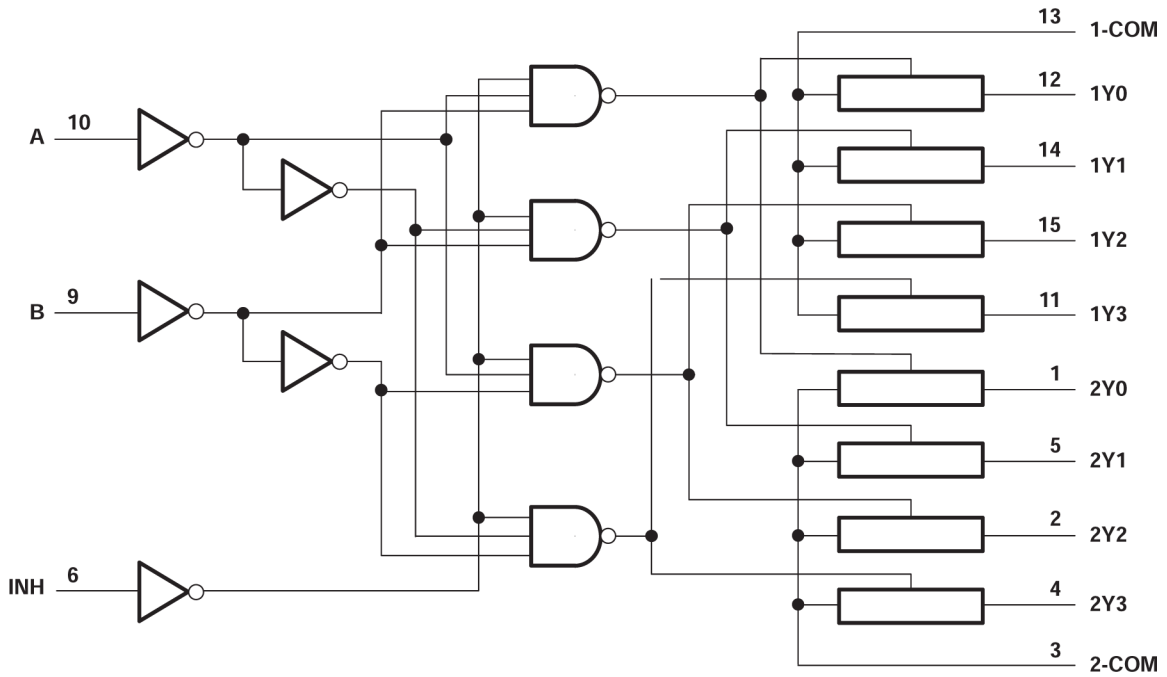


Figure 6-11. Power-Dissipation Capacitance, Test Setup

## 7 Detailed Description

### 7.1 Functional Block Diagram



## 8 Application and Implementation

### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

### 8.1 Application Information

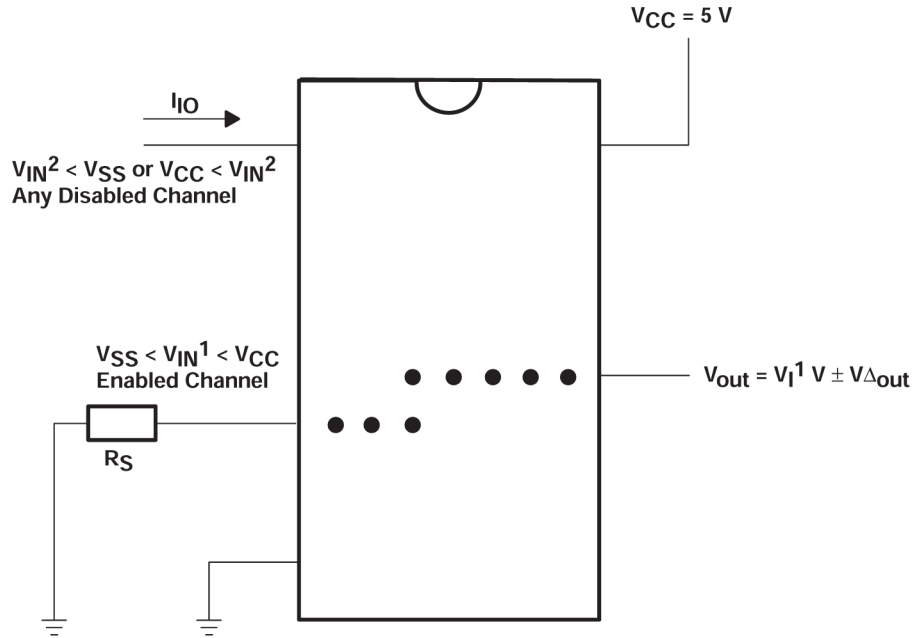


Figure 8-1. Injection-Current Coupling Specification

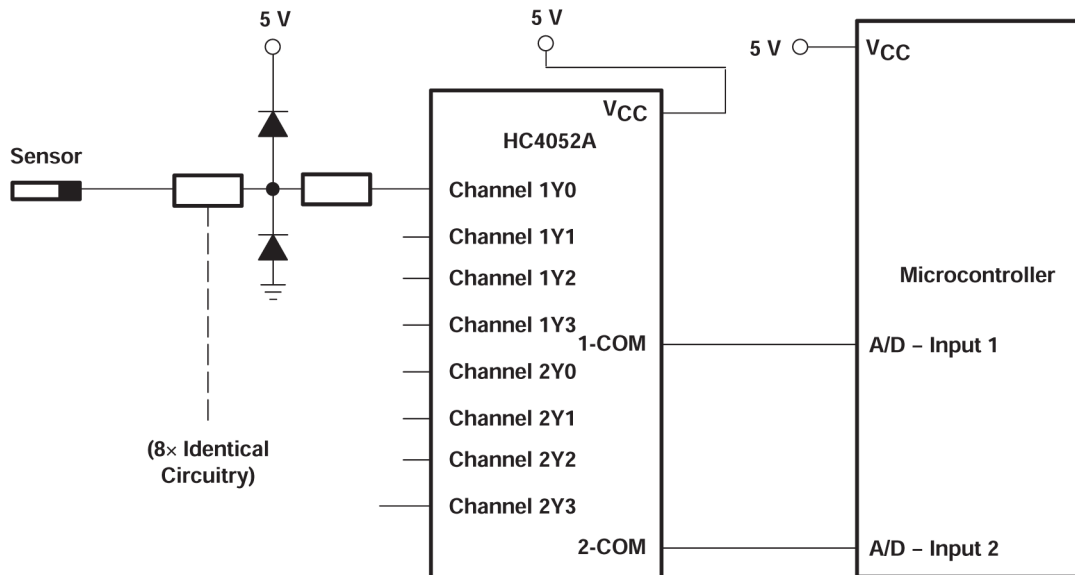


Figure 8-2. Actual Technology Requires 32 Passive Components and One Extra 6-v Regulator to Suppress Injection Current into a Standard HC4052 Multiplexer

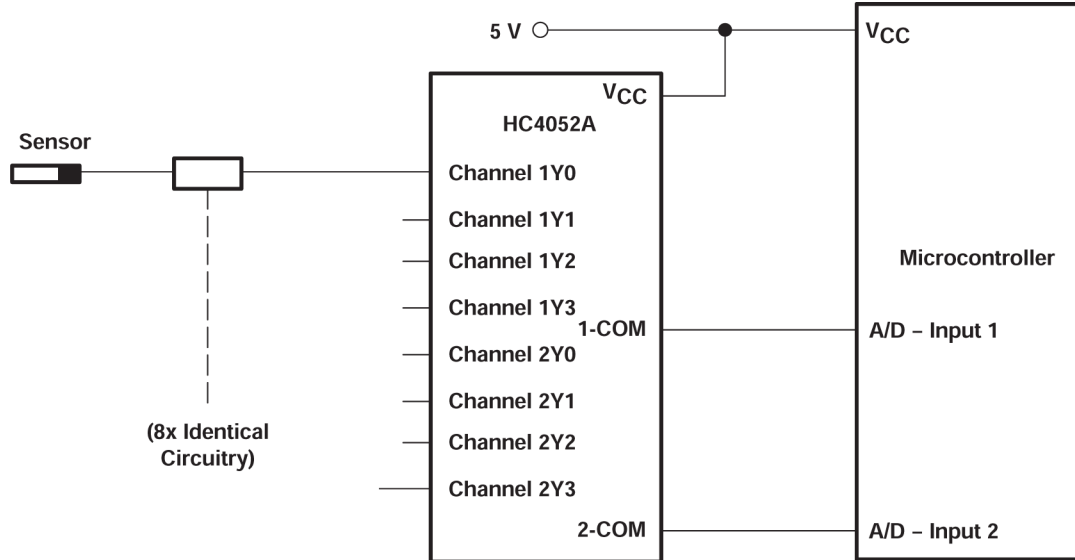


Figure 8-3. Solution by Applying the HC4852 Multiplexer

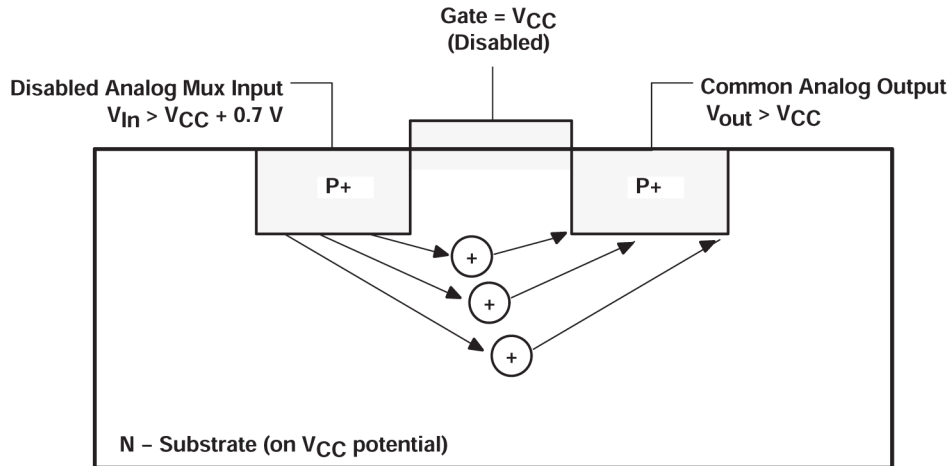


Figure 8-4. Diagram of Bipolar Coupling Mechanism (Appears If  $V_{In}$  Exceeds  $V_{CC}$ , Driving Injection Current into the Substrate)

## 9 Device and Documentation Support

### 9.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](http://ti.com). Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 9.2 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

### 9.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

### 9.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 9.5 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (March 2004) to Revision A (June 2024)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document.....	1
• Changed VCC ABS Max from 7V to 6V.....	3
• Changed RθJA.....	3
• Recommended supply changed from 6V to 5.5V and all test conditions using 6V were removed.....	4
• Changed tpd, ttran, tON, tOFF parameters.....	6

## 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74HC4852D	NRND	SOIC	D	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HC4852	
SN74HC4852DGVR	NRND	TVSOP	DGV	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HC4852	
SN74HC4852DR	NRND	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HC4852	
SN74HC4852DRG4	NRND	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC4852	
SN74HC4852N	NRND	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 125	SN74HC4852N	
SN74HC4852PW	NRND	TSSOP	PW	16	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HC4852	
SN74HC4852PWR	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HC4852	Samples
SN74HC4852PWRE4	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC4852	Samples

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

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**OTHER QUALIFIED VERSIONS OF SN74HC4852 :**

- Automotive : [SN74HC4852-Q1](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects



**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74HC4852DGVR	TVSOP	DGV	16	2000	330.0	12.4	6.8	4.0	1.6	8.0	12.0	Q1
SN74HC4852DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74HC4852PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74HC4852PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74HC4852DGVR	TVSOP	DGV	16	2000	356.0	356.0	35.0
SN74HC4852DR	SOIC	D	16	2500	353.0	353.0	32.0
SN74HC4852PWR	TSSOP	PW	16	2000	356.0	356.0	35.0
SN74HC4852PWR	TSSOP	PW	16	2000	210.0	185.0	35.0

**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN74HC4852D	D	SOIC	16	40	507	8	3940	4.32
SN74HC4852N	N	PDIP	16	25	506	13.97	11230	4.32
SN74HC4852PW	PW	TSSOP	16	90	530	10.2	3600	3.5

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



4040047-6/M 06/11

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  -  C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  -  D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AC.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



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**NOTES:**

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



SOLDER MASK DETAILS

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NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



DGV (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE

24 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.  
 D. Falls within JEDEC: 24/48 Pins – MO-153  
 14/16/20/56 Pins – MO-194

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - D The 20 pin end lead shoulder width is a vendor option, either half or full width.

4040049/E 12/2002

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