

High-Speed CMOS Logic Quad Bilateral Switch

February 1998 - Revised August 2004

Features

- **Wide Analog-Input-Voltage Range** 0V to 10V
- **Low "ON" Resistance**
 - 45Ω (Typ) $V_{CC} = 4.5V$
 - 35Ω (Typ) $V_{CC} = 6V$
 - 30Ω (Typ) $1fC V_{CC} = 9V$
- **Fast Switching and Propagation Delay Times**
- **Low "OFF" Leakage Current**
- **Built-In "Break-Before-Make" Switching**
- **Suitable for Sample and Hold Applications**
- **Wide Operating Temperature Range** . . . -55°C to 125°C
- **HC Types**
 - 2V to 10V Operation
 - High Noise Immunity: $N_{IL} = 30\%$, $N_{IH} = 30\%$ of V_{CC} at $V_{CC} = 5V$

Description

The CD74HC4016 contains four independent digitally controlled analog switches that use silicon-gate CMOS technology to achieve operating speeds similar to LSTTL with the low power consumption of standard CMOS integrated circuits.

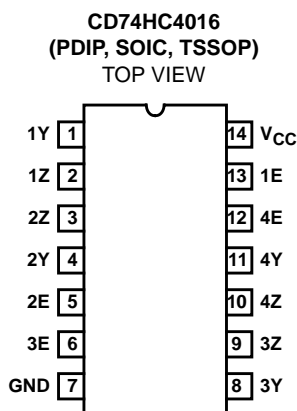
Each switch has two input/output terminals (nY, nZ) and an active high enable input (nE). Current through the switch will not cause additional V_{CC} current provided the analog voltage is maintained between V_{CC} and GND.

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE
CD74HC4016E	-55 to 125	14 Ld PDIP
CD74HC4016M	-55 to 125	14 Ld SOIC
CD74HC4016MT	-55 to 125	14 Ld SOIC
CD74HC4016M96	-55 to 125	14 Ld SOIC
CD74HC4016PW	-55 to 125	14 Ld TSSOP
CD74HC4016PWR	-55 to 125	14 Ld TSSOP

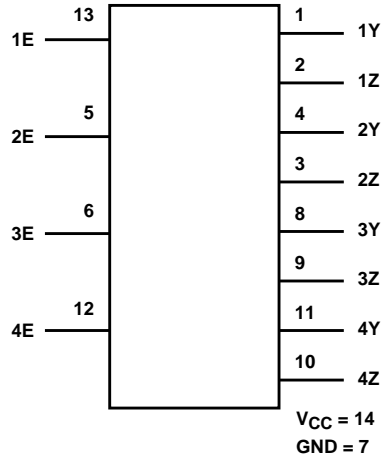
NOTE: When ordering, use the entire part number. The suffix 96 denotes tape and reel. The suffix T denotes a small-quantity reel of 250.

Pinout



CD74HC4016

Functional Diagram

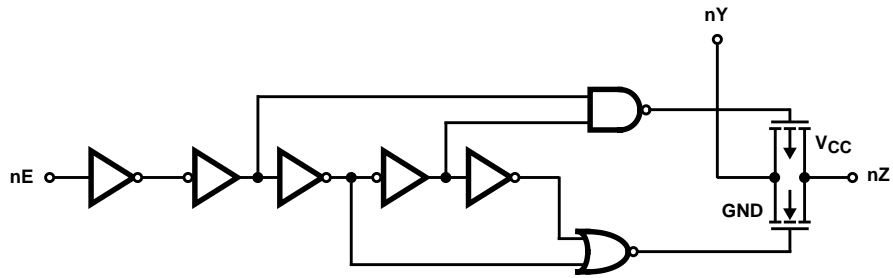


TRUTH TABLE

INPUT nE	SWITCH
L	OFF
H	ON

H = High Level Voltage
L = Low Level Voltage

Logic Diagram



CD74HC4016

Absolute Maximum Ratings

DC Supply Voltage, V_{CC}	-0.5V to 7V
DC Input Diode Current, I_{IK}	
For $V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$	$\pm 20mA$
DC Drain Current, per Output, I_O	
For $-0.5V < V_O < V_{CC} + 0.5V$	$\pm 25mA$
DC Output Diode Current, I_{OK}	
For $V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$	$\pm 20mA$
DC Output Source or Sink Current per Output Pin, I_O	
For $V_O > -0.5V$ or $V_O < V_{CC} + 0.5V$	$\pm 25mA$
DC V_{CC} or Ground Current, I_{CC}	$\pm 50mA$

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} ($^{\circ}C/W$)
E (PDIP) Package	80
M (SOIC) Package	86
PW (TSSOP) Package	96
Maximum Junction Temperature (Plastic Package)	150 $^{\circ}C$
Maximum Storage Temperature Range	-65 $^{\circ}C$ to 150 $^{\circ}C$
Maximum Lead Temperature (Soldering 10s)	300 $^{\circ}C$

Operating Conditions

Temperature Range, T_A	-55 $^{\circ}C$ to 125 $^{\circ}C$
Supply Voltage Range, V_{CC}	
HC Types2V to 10V
DC Input or Output Voltage, V_I, V_O	0V to V_{CC}
Input Rise and Fall Time	
2V	1000ns (Max)
4.5V	500ns (Max)
6V	400ns (Max)
9V	250ns (Max)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

- The package thermal impedance is calculated in accordance with JESD 51-7.

DC Electrical Specifications

PARAMETER	SYMBOL	TEST CONDITIONS			25 $^{\circ}C$			-40 $^{\circ}C$ TO 85 $^{\circ}C$		-55 $^{\circ}C$ TO 125 $^{\circ}C$		UNITS
		V_I (V)	V_{IS} (V)	V_{CC} (V)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HC TYPES												
High Level Input Voltage	V_{IH}	-	-	2	1.5	-	-	1.5	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	3.15	-	V
				6	4.2	-	-	4.2	-	4.2	-	V
Low Level Input Voltage	V_{IL}	-	-	2	-	-	0.5	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	-	1.35	V
				6	-	-	1.8	-	1.8	-	1.8	V
"ON" Resistance $I_O = 1mA$	R_{ON}	V_{IH} or V_{IL}	V_{CC} or GND	4.5	-	45	180	-	225	-	270	Ω
				6	-	35	160	-	200	-	240	Ω
				9	-	30	135	-	170	-	205	Ω
				4.5	-	85	320	-	400	-	480	Ω
				6	-	55	240	-	300	-	360	Ω
				9	-	35	170	-	215	-	255	Ω
Maximum "ON" Resistance Between Any Two Switches	ΔR_{ON}	V_{IL} or V_{IH}	V_{CC} or GND	4.5	-	10	-	-	-	-	-	Ω
				6	-	8.5	-	-	-	-	-	Ω
Switch Off Leakage Current	I_{IZ}	En = GND	V_{CC} or GND	6	-	-	± 0.1	-	± 1	-	± 1	μA
				10	-	-	± 0.1	-	± 1	-	± 1	μA
Logic Input Leakage Current	I_I	V_{CC} or GND	-	6	-	-	± 0.1	-	± 1	-	± 1	μA

CD74HC4016

DC Electrical Specifications (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS			25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
		V _I (V)	V _{IS} (V)	V _{CC} (V)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	
Quiescent Device Current I _O = 0mA	I _{CC}	V _{CC} or GND	V _{CC} or GND	6	-	-	2	-	20	-	40	μA
				10	-	-	16	-	160	-	320	μA

Switching Specifications Input t_r, t_f = 6ns

PARAMETER	SYMBOL	TEST CONDITIONS	V _{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HC TYPES											
Propagation Delay, Switch In to Switch Out	t _{PLH} , t _{PHL}	C _L = 50pF	2	-	-	60	-	75	-	90	ns
			4.5	-	-	12	-	15	-	18	ns
		C _L = 15pF	5	-	4	-	-	-	-	-	ns
			C _L = 50pF	6	-	-	10	-	13	-	15
		9		-	-	8	-	10	-	12	ns
Propagation Delay, Switch Turn-On En to Out	t _{PZH} , t _{PZL}	C _L = 50pF	2	-	-	190	-	240	-	285	ns
			4.5	-	-	38	-	48	-	57	ns
		C _L = 15pF	5	-	16	-	-	-	-	-	ns
			C _L = 50pF	6	-	-	32	-	41	-	48
		9		-	-	28	-	35	-	42	ns
Propagation Delay, Switch Turn-Off En to Out	t _{PHZ} , t _{PLZ}	C _L = 50pF	2	-	-	145	-	180	-	220	ns
			4.5	-	-	29	-	36	-	44	ns
		C _L = 15pF	5	-	12	-	-	-	-	-	ns
			C _L = 50pF	6	-	-	25	-	31	-	38
		9		-	-	22	-	28	-	33	ns
Input Capacitance	C _I	-	-	-	-	10	-	10	-	10	pF
Power Dissipation Capacitance (Notes 2, 3)	C _{PD}	-	5	-	12	-	-	-	-	-	pF

NOTES:

- C_{PD} is used to determine the dynamic power consumption, per package.
- $P_D = C_{PD} V_{CC}^2 f_i + \sum (C_L + C_S) V_{CC}^2 f_o$ where f_i = input frequency, f_o = output frequency, C_L = output load capacitance, C_S = switch capacitance, V_{CC} = supply voltage.

Analog Channel Specifications T_A = 25°C

PARAMETER	TEST CONDITIONS	V _{CC} (V)	CD74HC4016	UNITS
Switch Frequency Response Bandwidth at -3dB Figure 3	Figure 6, Notes 4, 5	4.5	>200	MHz
Crosstalk Between Any Two Switches, Figure 4	Figure 5, Notes 5, 6	4.5	TBE	dB
Total Harmonic Distortion	1kHz, V _{IS} = 4V _{P-P} Figure 7	4, 5	0.078	%
	1kHz, V _{IS} = 8V _{P-P} Figure 7	9	0.018	%

CD74HC4016

Analog Channel Specifications $T_A = 25^\circ\text{C}$ (Continued)

PARAMETER	TEST CONDITIONS	V_{CC} (V)	CD74HC4016	UNITS
Control to Switch Feedthrough Noise	Figure 8	4.5	TBE	mV
		9	TBE	mV
Switch "OFF" Signal Feedthrough, Figure 4	Figure 9, Notes 5, 6	4.5	-62	dB
Switch Input Capacitance, C_S		-	5	pF

NOTES:

4. Adjust input level for 0dBm at output, $f = 1\text{MHz}$.
5. V_{IS} is centered at $V_{CC}/2$.
6. Adjust input for 0dBm at V_{IS} .

Typical Performance Curves

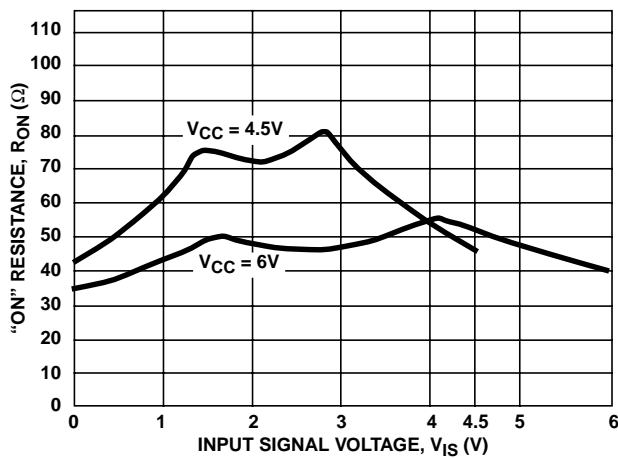


FIGURE 1. TYPICAL "ON" RESISTANCE vs INPUT SIGNAL VOLTAGE

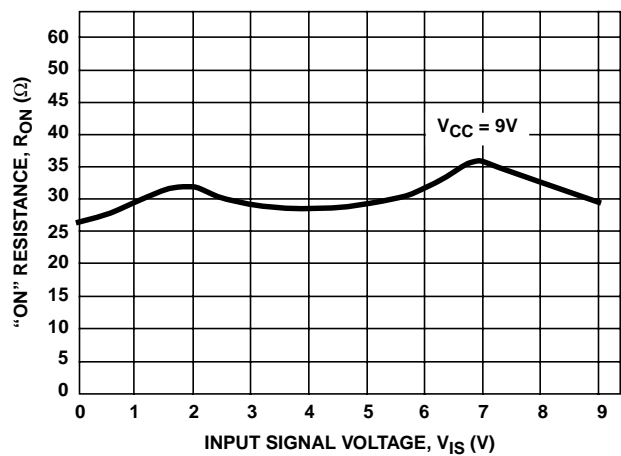


FIGURE 2. TYPICAL "ON" RESISTANCE vs INPUT SIGNAL VOLTAGE

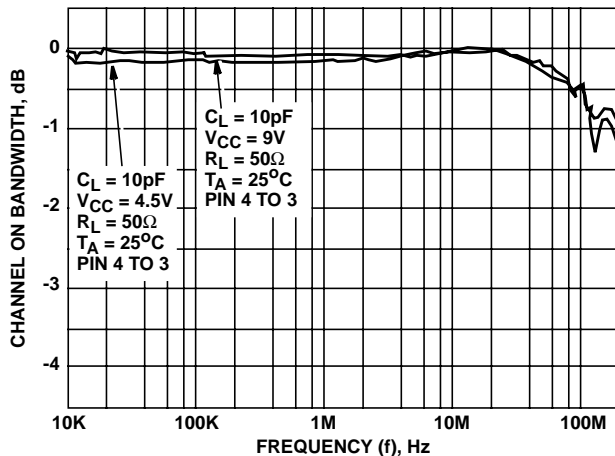


FIGURE 3. SWITCH FREQUENCY RESPONSE

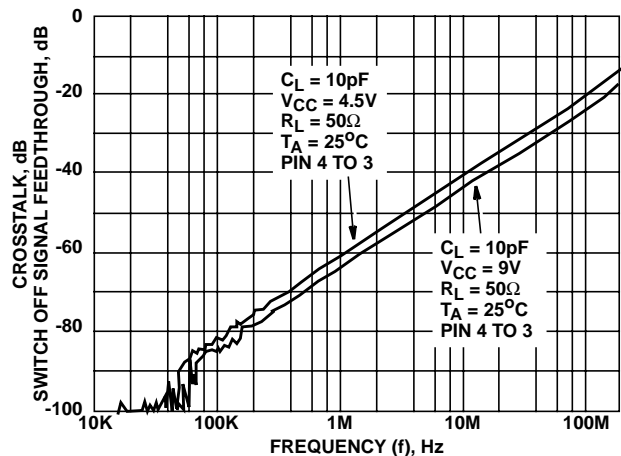


FIGURE 4. SWITCH-OFF SIGNAL FEEDTHROUGH AND CROSSTALK vs FREQUENCY

Analog Test Circuits

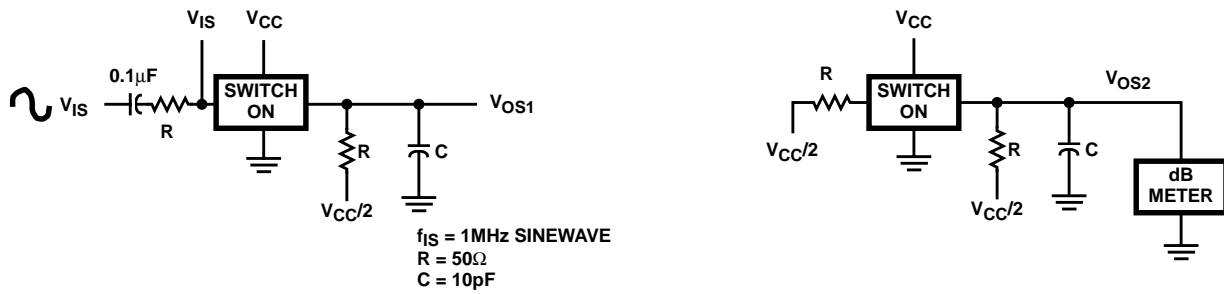


FIGURE 5. CROSSTALK BETWEEN TWO SWITCHES TEST CIRCUIT

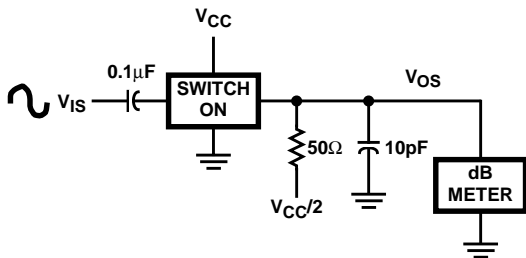


FIGURE 6. FREQUENCY RESPONSE TEST CIRCUIT

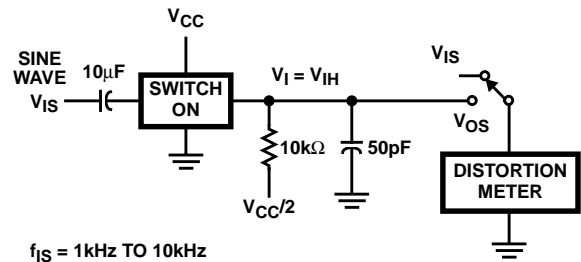


FIGURE 7. TOTAL HARMONIC DISTORTION TEST CIRCUIT

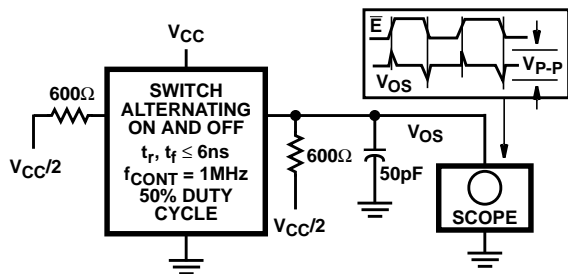


FIGURE 8. CONTROL-TO-SWITCH FEEDTHROUGH NOISE TEST CIRCUIT

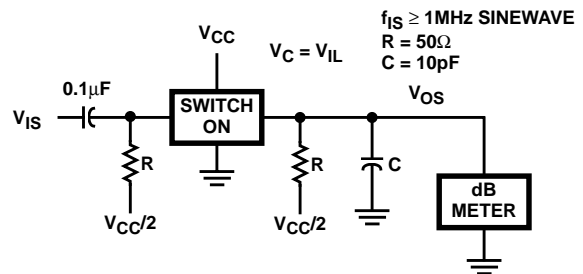


FIGURE 9. SWITCH OFF SIGNAL FEEDTHROUGH

Test Circuits and Waveforms

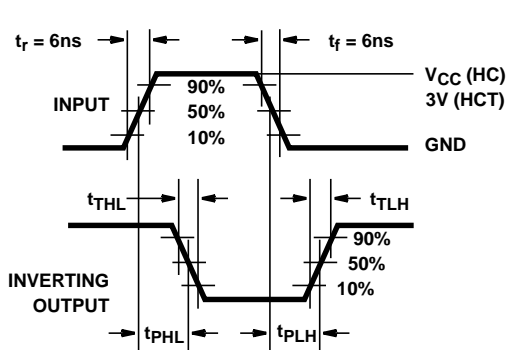


FIGURE 10. HC/HCT TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC

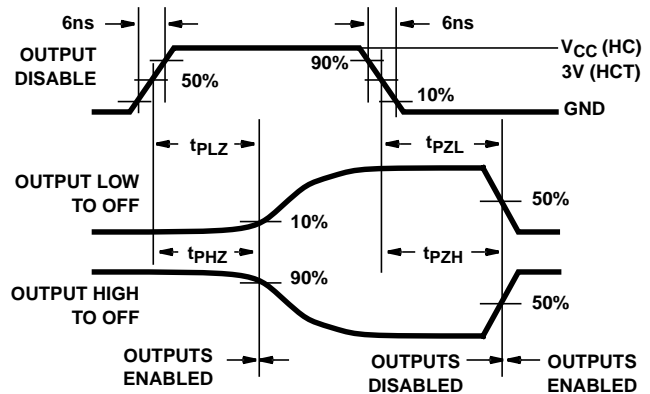


FIGURE 11. SWITCH TURN-ON AND TURN-OFF PROPAGATION DELAY TIMES

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CD74HC4016E	NRND	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-55 to 125	CD74HC4016E	
CD74HC4016M96	NRND	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC4016M	
CD74HC4016MT	NRND	SOIC	D	14	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC4016M	
CD74HC4016PW	NRND	TSSOP	PW	14	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HP14	

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74HC4016M96	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
CD74HC4016MT	SOIC	D	14	250	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74HC4016M96	SOIC	D	14	2500	356.0	356.0	35.0
CD74HC4016MT	SOIC	D	14	250	210.0	185.0	35.0

TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
CD74HC4016E	N	PDIP	14	25	506	13.97	11230	4.32
CD74HC4016E	N	PDIP	14	25	506	13.97	11230	4.32
CD74HC4016PW	PW	TSSOP	14	90	530	10.2	3600	3.5

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



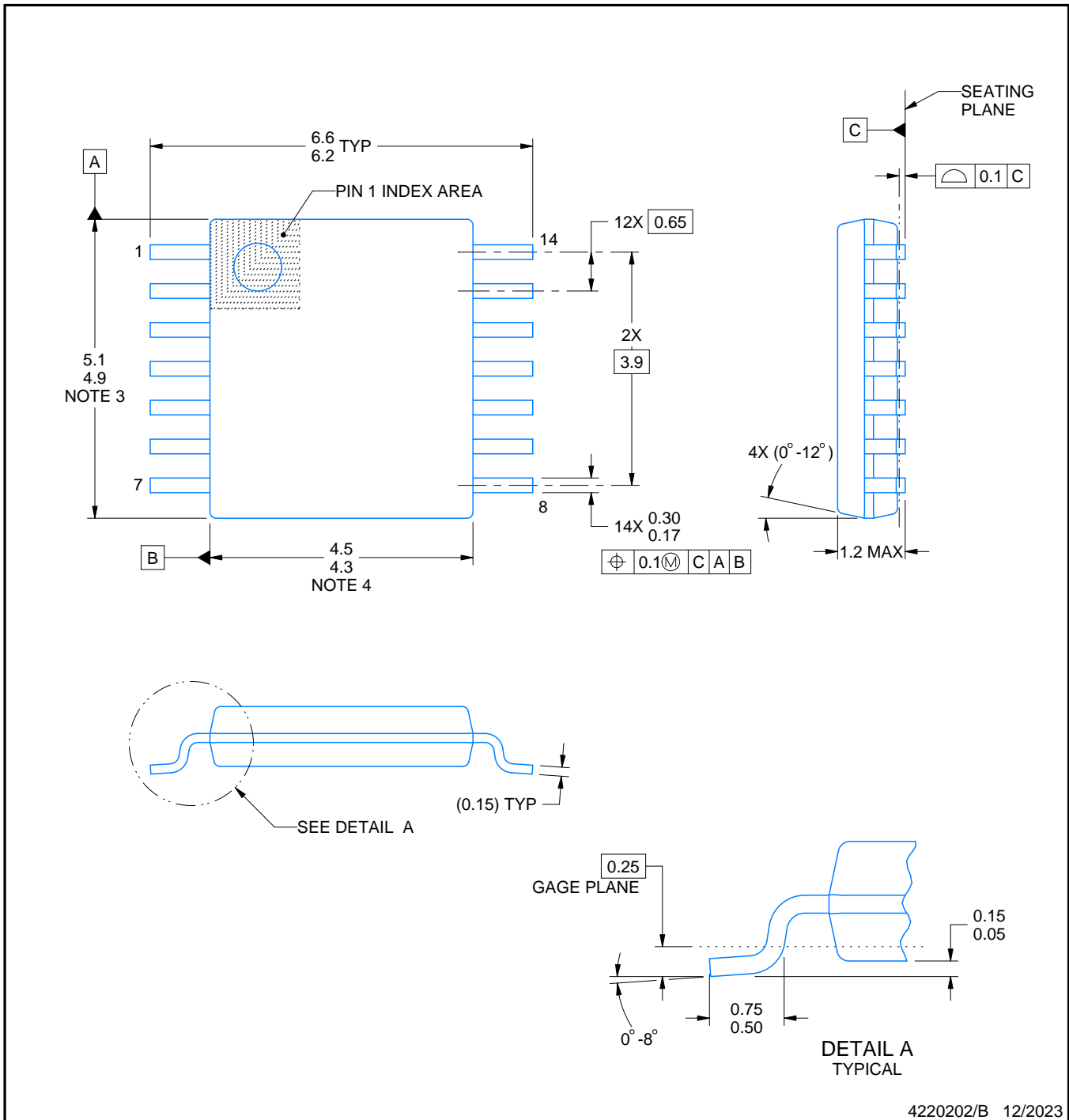
- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

PW0014A



PACKAGE OUTLINE
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4220202/B 12/2023

NOTES:

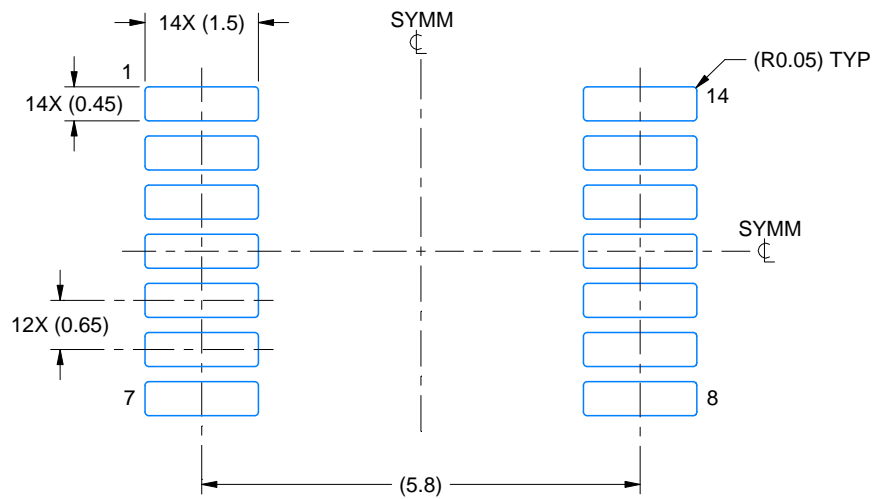
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

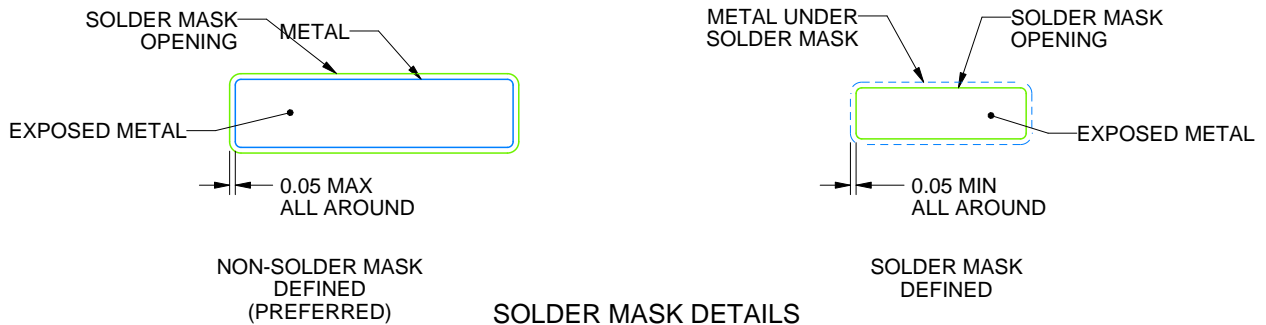
PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4220202/B 12/2023

NOTES: (continued)

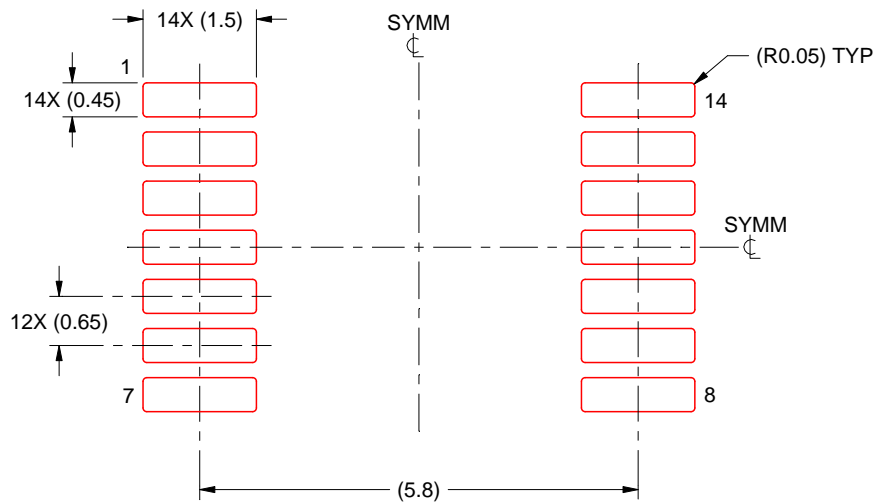
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



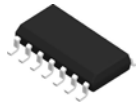
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

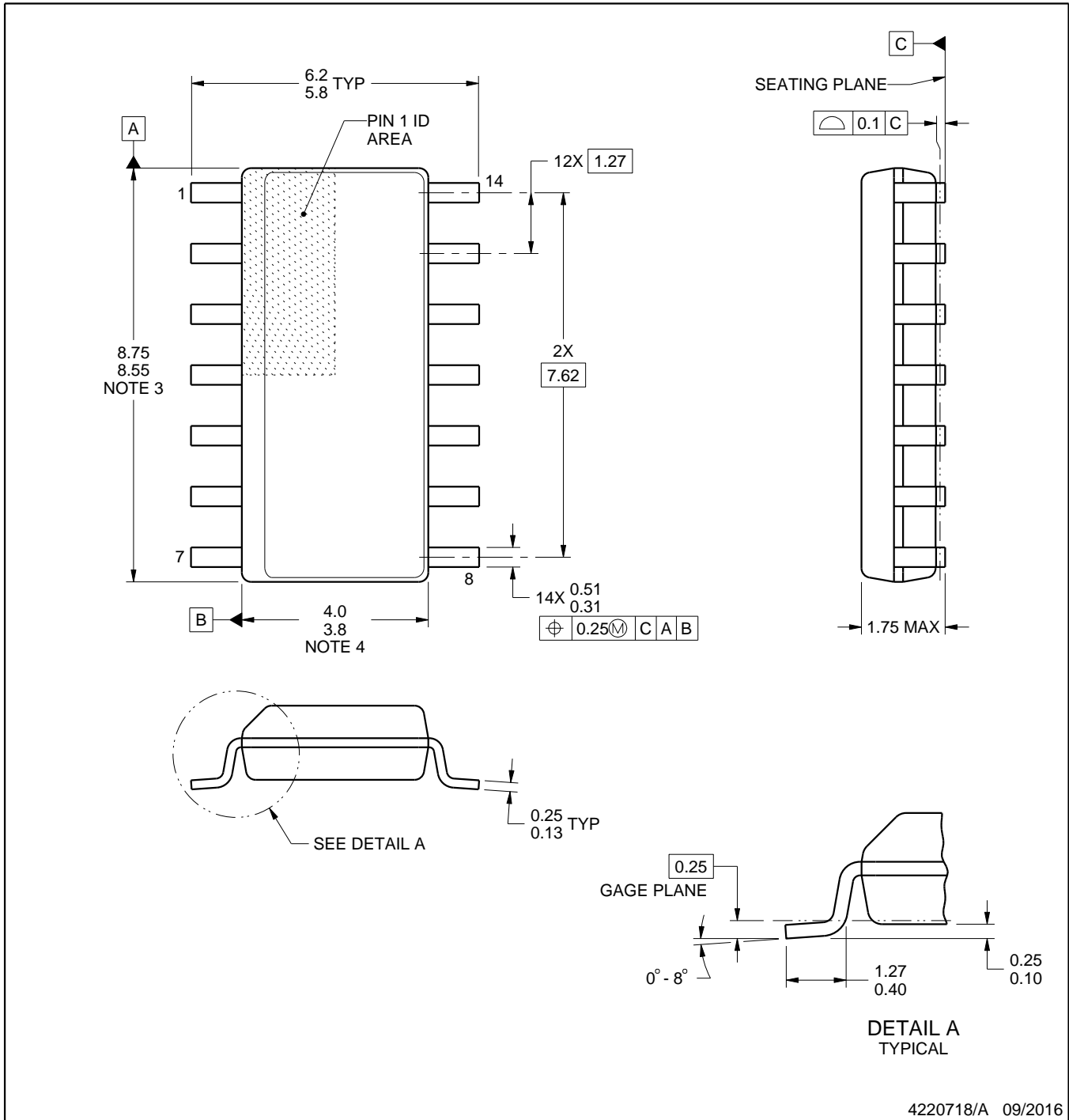
D0014A



PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4220718/A 09/2016

EXAMPLE BOARD LAYOUT

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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