

CD74HCT4066-Q1 Automotive High-speed CMOS Logic Quad Bilateral Switch

1 Features

- Qualified for automotive applications
- Low ON resistance:
 - 25Ω typical ($V_{CC} = 4.5V$)
- Fast switching and propagation speeds
- Low OFF leakage current
- Wide operating temperature range: $-40^{\circ}C$ to $125^{\circ}C$
- Direct LSTTL input logic compatibility: $V_{IL} = 0.8V$ maximum, $V_{IH} = 2V$ minimum
- CMOS input compatibility: $I_I \leq 1\mu A$ at V_{OL} , V_{OH}

2 Applications

- Analog signal switching and multiplexing: signal gating, modulators, squelch controls, demodulators, choppers, commutating switches
- Digital signal switching and multiplexing
- Analog-to-digital and digital-to-analog conversions
- Digital control of frequency, impedance, phase, and analog-signal gain
- Building automation

3 Description

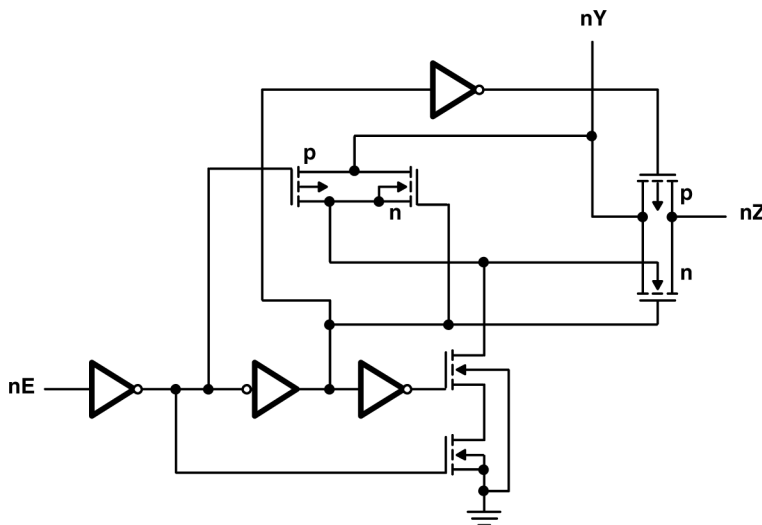
The CD74HCT4066-Q1 contains four independent digitally controlled analog switches that use silicon-gate CMOS technology to achieve operation speeds similar to LSTTL, with the low power consumption of standard CMOS integrated circuits.

These switches feature the characteristic linear ON resistance of the metal-gate CD4066B. Each switch is turned on by a high-level voltage on its control input.

Package Information

PART NUMBER	PACKAGE ⁽¹⁾	PACKAGE SIZE ⁽²⁾
CD74HCT4066-Q1	PW (TSSOP, 14)	5mm × 6.4mm

- (1) For more information, see [Section 10](#)
- (2) The package size (length × width) is a nominal value and includes pins, where applicable.



Logic Diagram (Positive Logic)



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4 Pin Configuration and Functions

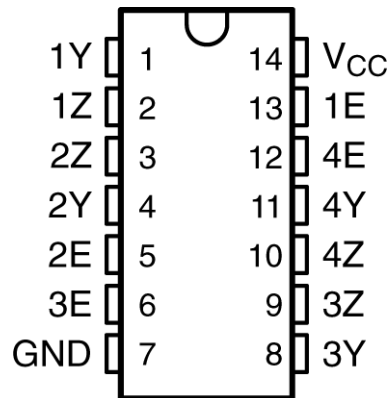


Figure 4-1. DW or PW Package, 14-Pin SOIC or TSSOP (Top View)

Table 4-1. Pin Functions

PIN		TYPE ⁽¹⁾	DESCRIPTION
NAME	NO.		
1Y	1	I/O	Input/Output for Switch 1
1Z	2	I/O	Input/Output for Switch 1
2Z	3	I/O	Input/Output for Switch 2
2Y	4	I/O	Input/Output for Switch 2
2E	5	I	Control pin for Switch 2
3E	6	I	Control pin for Switch 3
GND	7	-	Ground Pin
3Y	8	I/O	Input/Output for Switch 3
3Z	9	I/O	Input/Output for Switch 3
4Z	10	I/O	Input/Output for Switch 4
4Y	11	I/O	Input/Output for Switch 4
4E	12	I	Control pin for Switch 4
1E	13	I	Control pin for Switch 1
V _{CC}	14	-	Power Pin

(1) Signal Types: I = Input, O = Output, I/O = Input or Output.

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
V_{CC} (see (2))	Supply voltage range	-0.5	+7	V
I_{IK} ($V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$)	Input clamp current		±20	mA
I_{OK} ($V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$)	Output clamp current		±20	mA
I_O (see (3)) ($V_O > -0.5V$ or $V_O < V_{CC} + 0.5V$)	Switch current		±25	mA
I_O ($V_O > -0.5V$ or $V_O < V_{CC} + 0.5V$)	Output source or sink current per output pin		±25	mA
	Continuous current through V_{CC} or GND		±50	mA
T_{stg}	Storage temperature range	-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages referenced to GND unless otherwise specified.
- (3) In certain applications, the external load-resistor current may include both V_{CC} and signal-line components. To avoid drawing V_{CC} current when switch current flows into the transmission gate inputs (terminals 1, 4, 8, and 11), the voltage drop across the bidirectional switch must not exceed 0.6V (calculated from r_{on} values shown in the electrical characteristics table). No V_{CC} current flows through R_L if the switch current flows into terminals 2, 3, 9, and 10.

5.2 Thermal Information

THERMAL METRIC ⁽¹⁾		CD74HCT4066-Q1		UNIT
		PW (TSSOP)		
		14 PINS		
R _{θJA}	Junction-to-ambient thermal resistance	133.9		°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

5.3 Recommended Operating Conditions

(see ⁽¹⁾)

		MIN	MAX	UNIT
V _{CC}	Supply voltage	4.5	5.5	V
V _{IH}	High-level input voltage	2		V
V _{IL}	Low-level input voltage		0.8	V
V _I	Input voltage	0	V _{CC}	V
V _O	Output voltage	0	V _{CC}	V
t _t	Input transition (rise and fall) time		V _{CC} = 4.5V	ns
T _A	Operating free-air temperature	-40	125	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

5.4 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _I	V _{CC}	T _A = 25°C		T _A = -40 TO 125°C		UNIT
				MIN	TYP	MAX	MIN	
I _{IL}	Any control	V _{CC} or GND	5.5V			±0.1	±1	µA
I _{IZ}	V _{IS} = V _{CC} or GND	V _{IL}	5.5V			±0.1	±1	µA
r _{on}	I _O = 1mA, See Figure 5-1	V _{IS} = V _{CC} or GND	V _{CC}	4.5V	25	80	128	Ω
		V _{IS} = V _{CC} to GND	V _{CC}	4.5V	35	95	142	
Δr _{on}	Between any two switches	V _{CC}	4.5V		1			Ω
I _{CC}		V _{CC} or GND	5.5V			2	40	µA
ΔI _{CC}	Per input pin: 1 unit load, See ⁽¹⁾	V _{CC} - 2.1V	4.5V to 5.5V		100	360	490	µA
C _I	Control inputs					10	10	pF

(1) For dual-supply systems, theoretical worst case (V_I = 2.4V, V_{CC} = 5.5V) specification is 1.8mA.

5.5 HCT Input Loading

INPUT	UNIT LOADS ⁽¹⁾
All	1

(1) Unit load is ΔI_{CC} limit specified in the electrical characteristics table, for example, 360 µA max at 25°C.

5.6 Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 6-6](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	V _{CC}	T _A = 25°C			T _A = -40°C TO 125°C		UNIT
					MIN	TYP	MAX	MIN	MAX	
t _{pd}	Y or Z	Z or Y	C _L = 15pF	5V	1.3					ns
			C _L = 50pF	4.5V				12	18	
t _{en}	E	Y or Z	C _L = 15pF	5V	5					ns
			C _L = 50pF	4.5V				24	36	
t _{dis}	E	Y or Z	C _L = 15pF	5V	5.5					ns
			C _L = 50pF	4.5V				35	53	

5.7 Operating Characteristics

V_{CC} = 5V, T_A = 25°C, input t_r, t_f = 6ns

PARAMETER		TYP	UNIT
C _{pd}	Power dissipation capacitance (see ⁽¹⁾)	38	pF

(1) C_{pd} is used to determine the dynamic power consumption (P_D), per package.

- $P_D = (C_{pd} \times V_{CC}^2 \times f_i) + \sum (C_L + C_S) \times V_{CC}^2 \times f_O$
- f_O = output frequency
- f_I = input frequency
- C_L = output load capacitance
- C_S = switch capacitance
- V_{CC} = supply voltage

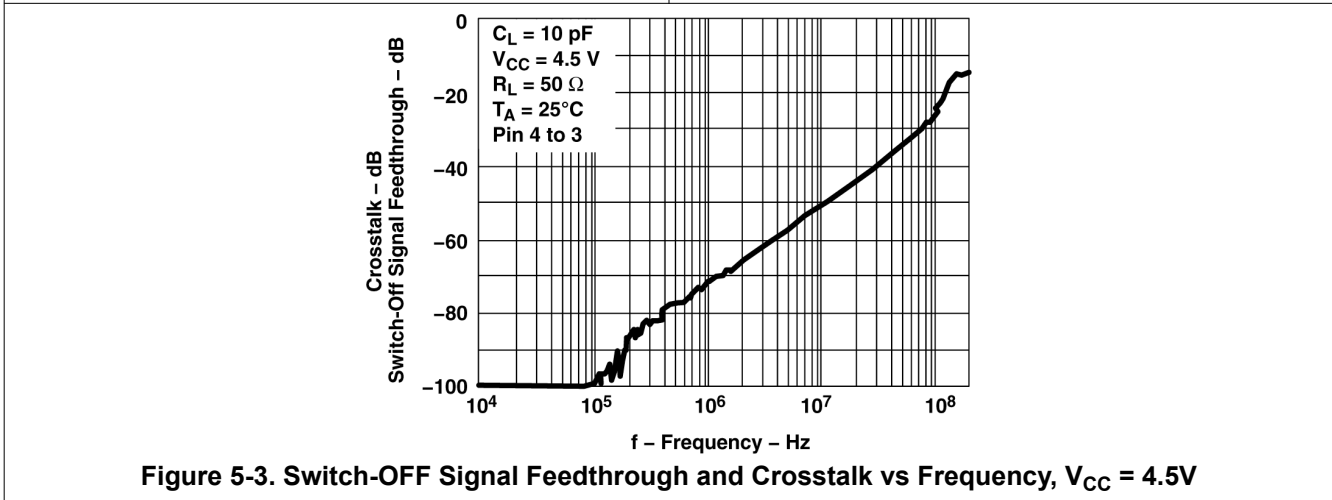
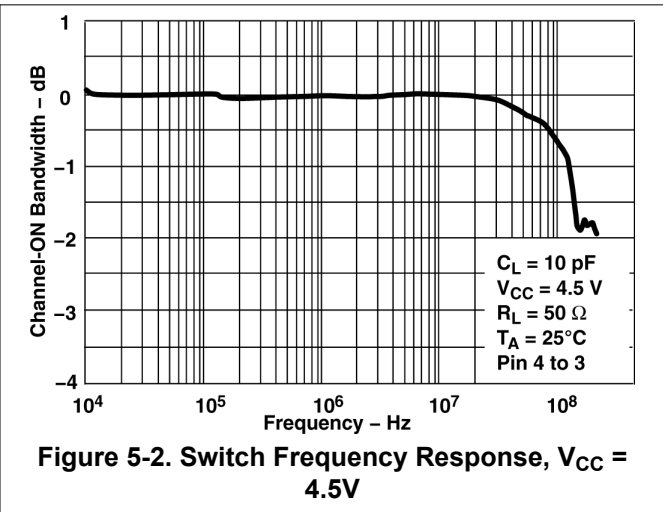
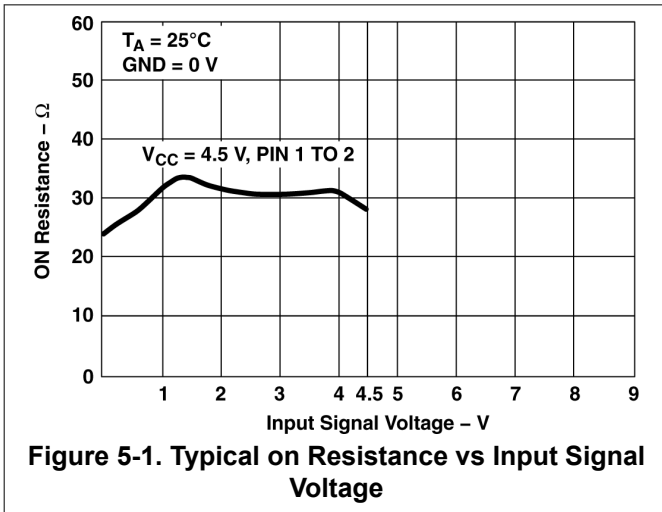
5.8 Analog Channel Characteristics

T_A = 25°C

PARAMETER		TEST CONDITIONS	V _{CC}	TYP	UNIT
f _{max}	Switch frequency response bandwidth at -3dB	See Figure 6-2 and Figure 5-2 and Notes 7 and 8	4.5V	200	MHz
	Crosstalk between any two switches	See Figure 6-1 and Figure 5-3 and Notes 8 and 9	4.5V	-72	dB
	Total harmonic distortion	See Figure 6-3 , 1kHz, V _{IS} = 4V _{P-P}	4.5V	0.023	%
	Control to switch feedthrough noise	See Figure 6-4	4.5V	130	mV
	Switch OFF signal feedthrough	See Figure 6-5 and Figure 5-3 and Notes 8 and 9	4.5V	-72	dB
C _S	Switch input capacitance			5	pF

- (1) Adjust input voltage to obtain 0dBm at output, f = 1MHz.
- (2) V_{IS} is centered at V_{CC}/2.
- (3) Adjust input for 0dBm at V_{IS}.

5.9 Typical Characteristics



6 Parameter Measurement Information

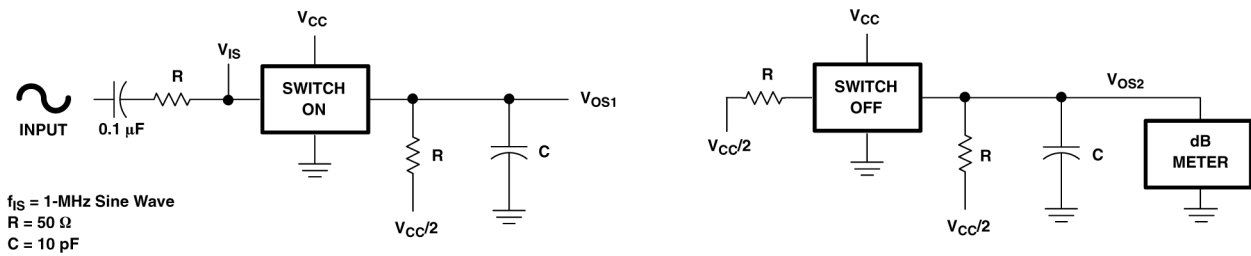


Figure 6-1. Crosstalk between Two Switches Test Circuit

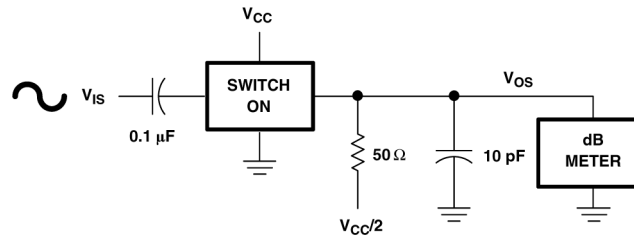


Figure 6-2. Frequency-Response Test Circuit

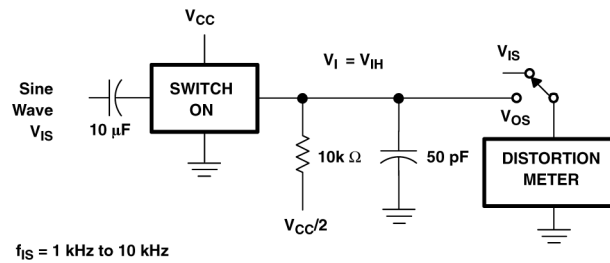


Figure 6-3. Total Harmonic Distortion Test Circuit

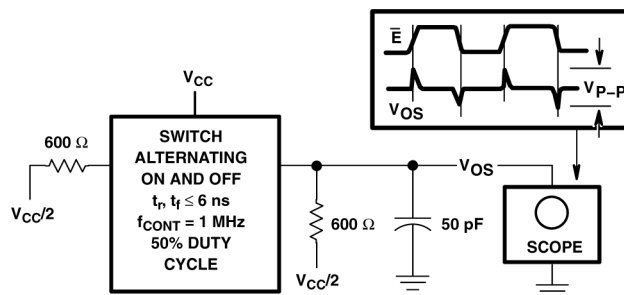


Figure 6-4. Control-to-Switch Feedthrough Noise Test Circuit

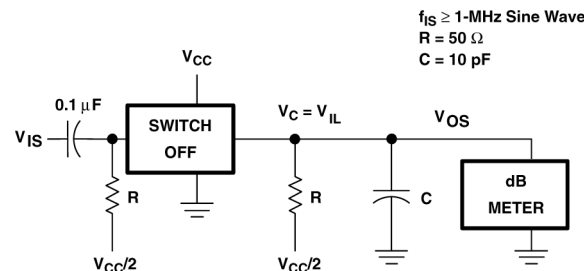
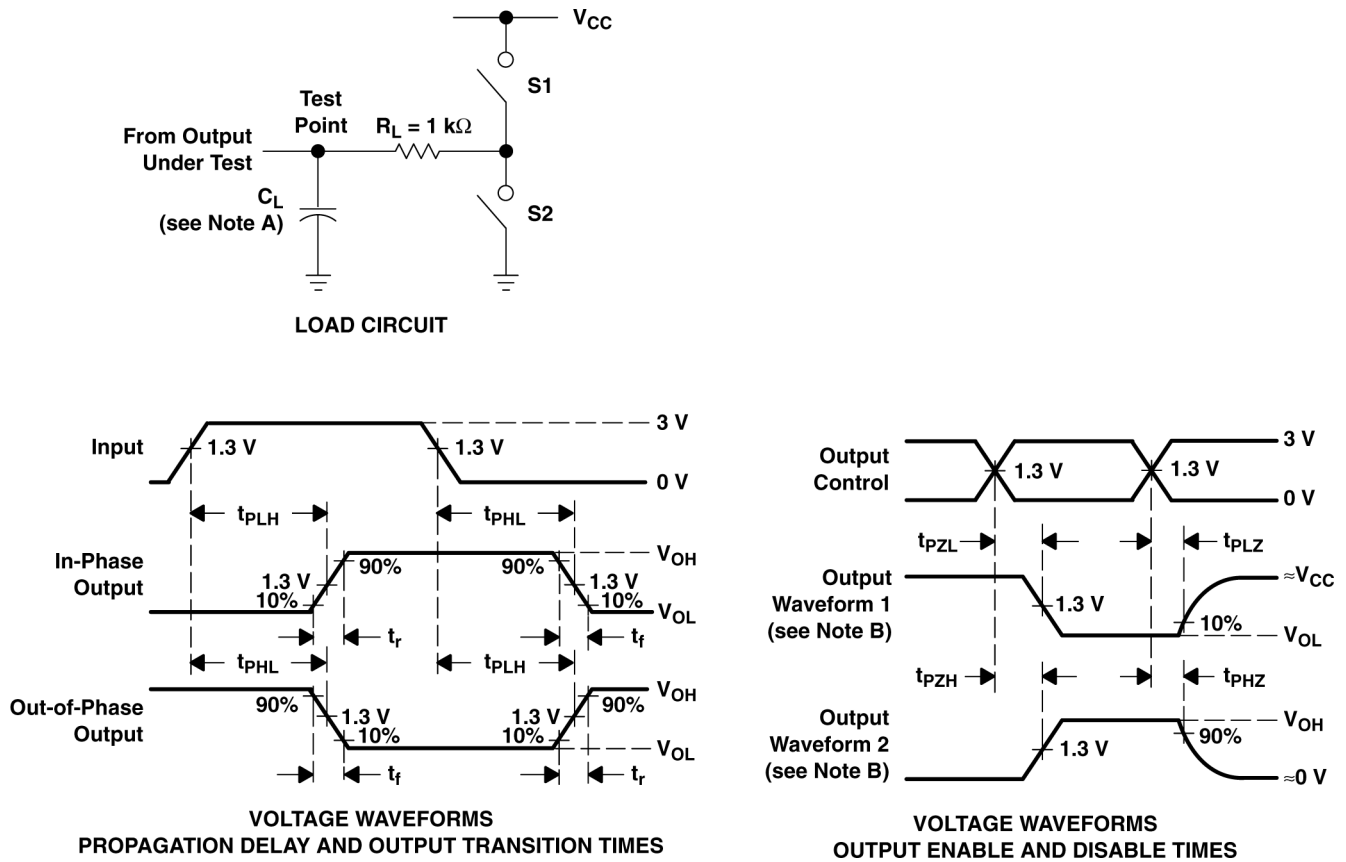


Figure 6-5. Switch off Signal Feedthrough Test Circuit



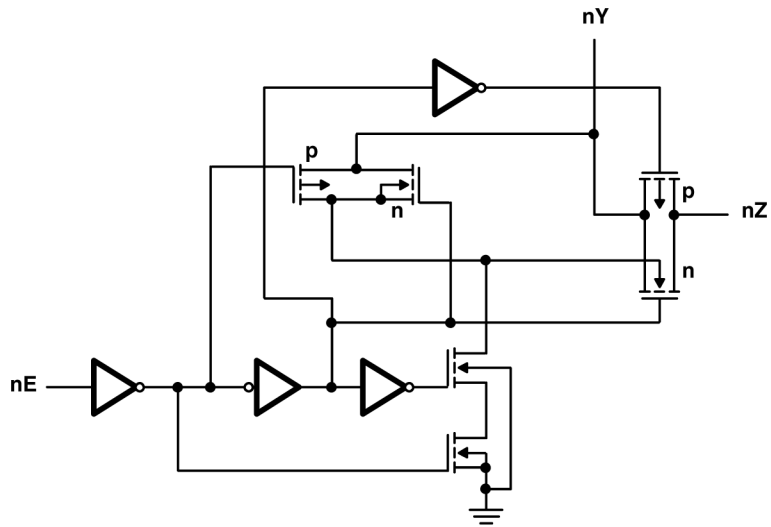
- A. C_L includes probe and test-fixture capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1\text{MHz}$, $Z_O = 50\Omega$, $t_r = 6\text{ns}$, $t_f = 6\text{ns}$.
- D. For clock inputs, f_{max} is measured with the input duty cycle at 50%.
- E. The outputs are measured one at a time, with one input transition per measurement.
- F. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- G. t_{PZL} and t_{PZH} are the same as t_{en} .
- H. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 6-6. Load Circuit and Voltage Waveforms

PARAMETER		S1	S2
t_{en}	t_{PZH}	Open	Closed
	t_{PZL}	Closed	Open
t_{dis}	t_{PHZ}	Open	Closed
	t_{PLZ}	Closed	Open
t_{pd}		Open	Open

7 Detailed Description

7.1 Functional Block Diagram



7.2 Device Functional Modes

Table 7-1. Function Table

INPUT	SWITCH
nE	
L ⁽²⁾	Off
H ⁽¹⁾	On

- (1) H = High level
 (2) L = Low level

8 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

8.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.2 Support Resources

TI E2E™ [support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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8.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
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8.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.5 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (April 2008) to Revision C (July 2024)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document.....	1
• Updated ordering information.....	1
• Updated thermal information and added CD74HCT4066-Q1.....	5
• Updated switching specifications.....	6

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CD74HCT4066QM96Q1	NRND	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HCT4066Q	
CD74HCT4066QPWRQ1	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HK4066Q	Samples
D24066QM96G4Q1	NRND	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HCT4066Q	
HCT4066QPWRG4Q1	OBSOLETE	TSSOP	PW	14		TBD	Call TI	Call TI	-40 to 125	HK4066Q	

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF CD74HCT4066-Q1 :

- Catalog : [CD74HCT4066](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74HCT4066QPWRQ1	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74HCT4066QPWRQ1	TSSOP	PW	14	2000	367.0	367.0	35.0



D0014A

PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4220718/A 09/2016

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.

EXAMPLE BOARD LAYOUT

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



4220202/B 12/2023

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4220202/B 12/2023

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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