Isolated Sigma-Delta Modulator

FEATURES

- 10 MHz clock rate
- Second-order modulator
- 16 bits, no missing codes
- ±2 LSB INL typical at 16 bits
- 1.5 μV/°C typical offset drift
- On-board digital isolator
- On-board reference
- ±250 mV analog input range
- Low power operation: 15.5 mA typical at 5.5 V
- −40°C to +125°C operating range
- 16-lead SOIC package
  - AD7401A, external clock version in 16-lead SOIC
- Safety and regulatory approvals
  - UL 1577
    - V_{ISO} = 5000 V rms for 1 minute
  - IEC / CSA 62368-1
  - IEC / CSA 61010-1
  - DIN EN IEC 60747-17 (VDE 0884-17)
    - V_{IORM} = 645 V peak

APPLICATIONS

- AC motor controls
- Shunt current monitoring
- Data acquisition systems
- Analog-to-digital and opto-isolator replacements

FUNCTIONAL BLOCK DIAGRAM

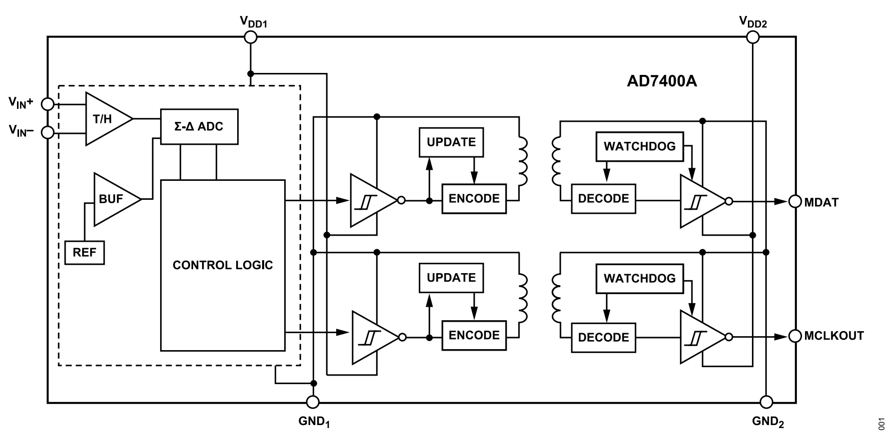


Figure 1.

GENERAL DESCRIPTION

The AD7400A[1] is a second-order, Σ-Δ modulator that converts an analog input signal into a high speed, 1-bit data stream with on-chip digital isolation based on Analog Devices, Inc., *i*Coupler® technology. The AD7400A operates from a 5 V power supply and accepts a differential input signal of ±250 mV (±320 mV full-scale). The analog input is sampled continuously by the analog modulator, eliminating the need for external sample-and-hold circuitry. The input information is contained in the output stream as a density of ones with a data rate of 10 MHz. The original information can be reconstructed with an appropriate digital filter. The serial I/O can use a 5 V or a 3 V supply (V_{DD2}).

The serial interface is digitally isolated. High speed CMOS, combined with monolithic air core transformer technology, means the on-chip isolation provides outstanding performance characteristics superior to alternatives such as optocoupler devices. The part contains an on-chip reference and has an operating temperature range of −40°C to +125°C. The AD7400A is offered in a 16-lead SOIC package.

[1] Protected by U.S. Patents 5,952,849; 6,873,065; and 7,075,329.

Rev. F

DOCUMENT FEEDBACK

TECHNICAL SUPPORT

TABLE OF CONTENTS

REVISION HISTORY

10/2024—Rev. E to Rev. F

Changed Master to Main (Throughout)...........1
Changes to Features Section...........1
Changes to Table 3...........5
Changes to Regulatory Information Section and Table 4...........5
Changed DIN V VDE V 0884-10 (VDE V 0884-10) Insulation Characteristics Section to DIN EN IEC 60747-17 (VDE 0884-17) Insulation Characteristics Section...........5
Changes to Table 5...........5
Changes to Figure 4 Caption...........6
Deleted Table 7; Renumbered Sequentially...........7
Deleted Insulation Lifetime Section and Figure 28 to Figure 30; Renumbered Sequentially...........17

SPECIFICATIONS

V_{DD1} = 4.5 V to 5.5 V, V_{DD2} = 3 V to 5.5 V, $V_{IN}+$ = −200 mV to +200 mV, except where specified, and $V_{IN}-$ = 0 V (single-ended); T_A = −40°C to +125°C, except where specified; f_{MCLK} = 10 MHz, tested with $Sinc^3$ filter, 256 decimation rate, as defined by Verilog code, unless otherwise noted.

Table 1.

	Y Version[1]				
Parameter	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions/Comments**
STATIC PERFORMANCE					
Resolution	16			Bits	Filter output truncated to 16 bits
Integral Nonlinearity[2]		±2	±12	LSB	$V_{IN}+$ = ±200 mV, T_A = −40°C to +125°C
		±4	±16	LSB	$V_{IN}+$ = ±250 mV, T_A = −40°C to +85°C
		±4	±22	LSB	$V_{IN}+$ = ±250 mV, T_A = −40°C to +125°C
Differential Nonlinearity[2]			±0.9	LSB	Guaranteed no missing codes to 16 bits
Offset Error[2]		±50	±500	µV	
Offset Drift vs. Temperature		1.5	4	µV/°C	−40°C to +125°C
Offset Drift vs. V_{DD1}		120		µV/V	
Gain Error[2]			±1.5	mV	−40°C to +85°C
			±2	mV	−40°C to +125°C
Gain Error Drift vs. Temperature		23		µV/°C	−40°C to +125°C
Gain Error Drift vs. V_{DD1}		110		µV/V	
ANALOG INPUT					
Input Voltage Range	−250		+250	mV	For specified performance, full range = ±320 mV
Dynamic Input Current		±7	±8	µA	$V_{IN}+$ = 400 mV, $V_{IN}-$ = 0 V
		±9	±10	µA	$V_{IN}+$ = 500 mV, $V_{IN}-$ = 0 V
		±0.5		µA	$V_{IN}+$ = $V_{IN}-$ = 0 V
Input Capacitance		10		pF	
DYNAMIC SPECIFICATIONS					$V_{IN}+$ = 35 Hz
Signal-to-Noise and Distortion (SINAD) Ratio[2]	70	78		dB	$V_{IN}+$ = ±200 mV
	68	78		dB	$V_{IN}+$ = ±250 mV
Signal-to-Noise Ratio (SNR)	73	80		dB	$V_{IN}+$ = ±200 mV
	72	80		dB	$V_{IN}+$ = ±250 mV
Total Harmonic Distortion (THD)[2]		−84		dB	$V_{IN}+$ = ±200 mV
		−82		dB	$V_{IN}+$ = ±250 mV
Peak Harmonic or Spurious Noise (SFDR)[2]		−86		dB	$V_{IN}+$ = ±200 mV
		−84		dB	$V_{IN}+$ = ±250 mV
Effective Number of Bits (ENOB)[2]	11.5	12.5		Bits	$V_{IN}+$ = ±200 mV
	11	12.5		Bits	$V_{IN}+$ = ±250 mV
Isolation Transient Immunity[2]	25	30		kV/µs	
LOGIC OUTPUTS					
Output High Voltage, V_{OH}	V_{DD2} − 0.1			V	I_O = −200 µA
Output Low Voltage, V_{OL}			0.4	V	I_O = +200 µA
POWER REQUIREMENTS					
V_{DD1}	4.5		5.5	V	
V_{DD2}	3		5.5	V	
I_{DD1}[3]		11	13	mA	V_{DD1} = 5.5 V
I_{DD2}[4]		4.5	6	mA	V_{DD2} = 5.5 V
		3	3.5	mA	V_{DD2} = 3.3 V

1 All voltages are relative to their respective ground.

2 See the Terminology section.

SPECIFICATIONS

3 See Figure 14.

4 See Figure 15.

TIMING SPECIFICATIONS

V_{DD1} = 4.5 V to 5.5 V, V_{DD2} = 3 V to 5.5 V, T_A = −40°C to +125°C, except where specified. Sample tested during initial release to ensure compliance.

Table 2.

Parameter	Limit at t_{MIN}, t_{MAX}	Unit	Description
$f_{MCLKOUT}$[1]	10	MHz typ	Main clock output frequency
	9/11	MHz min/MHz max	Main clock output frequency
t_1[2]	40	ns max	Data access time after MCLK rising edge
t_2[2]	10	ns min	Data hold time after MCLK rising edge
t_3	0.4 × $t_{MCLKOUT}$	ns min	Main clock low time
t_4	0.4 × $t_{MCLKOUT}$	ns min	Main clock high time

1 Mark space ratio for clock output is 40/60 to 60/40.

2 Measured with the load circuit shown in Figure 2 and defined as the time required for the output to cross 0.8 V or 2.0 V.

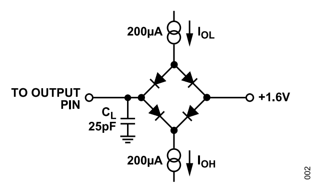


Figure 2. Load Circuit for Digital Output Timing Specifications

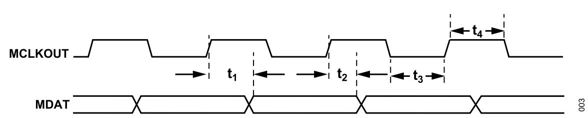


Figure 3. Data Timing

SPECIFICATIONS

INSULATION AND SAFETY-RELATED SPECIFICATIONS

Table 3.

Parameter	Symbol	Value	Unit	Conditions
Rated Dielectric Insulation Voltage	V_{ISO}	5000	V rms	1-minute duration
Minimum External Air Gap (Clearance)	L(I01)	7.8[1, 2]	mm	Measured from input terminals to output terminals, shortest distance through air
Minimum External Tracking (Creepage)	L(I02)	7.8	mm	Measured from input terminals to output terminals, shortest distance path along body
Minimum Internal Gap (Internal Clearance)		18	μm	Insulation distance through insulation
Tracking Resistance (Comparative Tracking Index)	CTI	>400	V	DIN IEC 112/VDE 0303 Part 1
Material Group		II		Material group per IEC 60664-1

1 In accordance with IEC 62368-1 guidelines for the measurement of creepage and clearance distances for a pollution degree of 2 and altitudes ≤2000 m.

2 Consideration must be given to pad layout to ensure the minimum required distance for clearance is maintained.

REGULATORY INFORMATION

The AD7400A certification approvals are listed in Table 4.

Table 4. Regulatory Information

Regulatory Agency	Standard Certification/Approval	File
UL	1577 Single Protection, 5000 V rms Isolation Voltage[1]	File E214100
CSA	IEC / CSA 62368-1 Basic Insulation, 780 V rms Reinforced Insulation, 390 V rms IEC / CSA 61010-1 Basic Insulation, 600 V rms, Overvoltage Category III Reinforced Insulation, 300 V rms	File No. 205078
Not CQC Certified		
VDE	DIN EN IEC 60747-17 (VDE 0884-17) Reinforced Insulation, 645 V peak[2]	Certificate No. 40011599

1 In accordance with UL 1577, each AD7400A is proof tested by applying an insulation test voltage ≥ 6000 V rms for 1 second (current leakage detection limit = 15 μA).

2 In accordance with DIN EN IEC 60747-17 (VDE 0884-17), each AD7400A is proof tested by applying an insulation test voltage ≥ 1671 V peak for 1 second (partial discharge detection limit = 5 pC).

DIN EN IEC 60747-17 (VDE 0884-17) INSULATION CHARACTERISTICS

This isolator is suitable for reinforced electrical isolation only within the safety limit data. Maintenance of the safety data is ensured by means of protective circuits.

Table 5.

Description	Symbol	Characteristic	Unit
OVERVOLTAGE CATEGORY PER IEC 60664-1			
For Rated Mains Voltage ≤ 300 V rms		I–IV	
For Rated Mains Voltage ≤ 450 V rms		I–II	
For Rated Mains Voltage ≤ 600 V rms		I–II	
CLIMATIC CLASSIFICATION		40/105/21	
POLLUTION DEGREE (DIN VDE 0110, Table 1)		2	
MAXIMUM REPETITIVE ISOLATION VOLTAGE	V_{IORM}	645	V peak

SPECIFICATIONS

Table 5. (Continued)

Description	Symbol	Characteristic	Unit
MAXIMUM WORKING INSULATION VOLTAGE	V_{IOWM}	456	V rms
INPUT-TO-OUTPUT TEST VOLTAGE, METHOD B1			
V_{IORM} × 1.875 = V_{PR}, 100% Production Test, t_m = 1 sec, Partial Discharge < 5 pC	V_{PR}	1209	V peak
INPUT-TO-OUTPUT TEST VOLTAGE, METHOD A	V_{PR}		
After Environmental Test Subgroup 1		1032	V peak
V_{IORM} × 1.6 = V_{PR}, t_m = 60 sec, Partial Discharge < 5 pC			
After Input and/or Safety Test Subgroup 2/3		774	V peak
V_{IORM} × 1.2 = V_{PR}, t_m = 60 sec, Partial Discharge < 5 pC			
MAXIMUM TRANSIENT ISOLATION VOLTAGE (TRANSIENT OVERVOLTAGE, t_{TR} = 10 sec)	V_{IOTM}	6000	V peak
MAXIMUM IMPULSE VOLTAGE	V_{IMP}	6000	V peak
Tested in Air, 1.2 µs/50 µs Waveform per IEC 61000-4-5			
MAXIMUM SURGE ISOLATION VOLTAGE	V_{IOSM}	N/A	V peak
Tested in Oil, 1.2 µs/50 µs Waveform per IEC 61000-4-5, V_{TEST} = V_{IOSM} × 1.3 OR ≥ 10 kV			
SAFETY-LIMITING VALUES (MAXIMUM VALUE ALLOWED IN THE EVENT OF A FAILURE, ALSO SEE Figure 4)			
Case Temperature	T_S	150	°C
Side 1 Current	I_{S1}	265	mA
Side 2 Current	I_{S2}	335	mA
INSULATION RESISTANCE AT T_S, V_{IO} = 500 V	R_S	$>10^9$	Ω

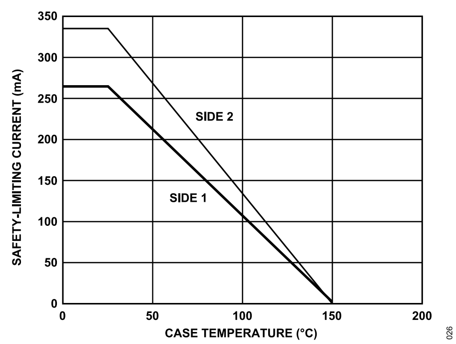


Figure 4. Thermal Derating Curve, Dependence of Safety-Limiting Values with Case Temperature per DIN EN IEC 60747-17 (VDE 0884-17)

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted. All voltages are relative to their respective ground.

Table 6.

Parameter	Rating
V_{DD1} to GND_1	−0.3 V to +6.5 V
V_{DD2} to GND_2	−0.3 V to +6.5 V
Analog Input Voltage to GND_1	−0.3 V to V_{DD1} + 0.3 V
Output Voltage to GND_2	−0.3 V to V_{DD2} + 0.3 V
Input Current to Any Pin Except Supplies[1]	±10 mA
Operating Temperature Range	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
SOIC Package	
θ_{JA} Thermal Impedance[2]	89.2°C/W
θ_{JC} Thermal Impedance[2]	55.6°C/W
Resistance (Input-to-Output), R_{I-O}	10^{12} Ω
Capacitance (Input-to-Output), C_{I-O}[3]	1.7 pF typ
RoHS-Compliant Temperature, Soldering	
Reflow	260 (+0)°C
ESD	2.5 kV

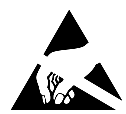
1 Transient currents of up to 100 mA do not cause SCR to latch-up.

2 JEDEC 2S2P standard board.

3 f = 1 MHz.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

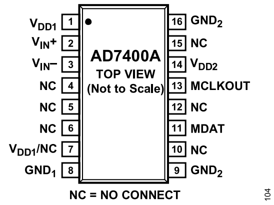


Figure 5. Pin Configuration

Table 7. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V_{DD1}	Supply Voltage, 4.5 V to 5.5 V. This is the supply voltage for the isolated side of the AD7400A and is relative to GND_1.
2	$V_{IN}+$	Positive Analog Input. Specified range of ±250 mV.
3	$V_{IN}−$	Negative Analog Input. Normally connected to GND_1.
4 to 6, 10, 12, 15	NC	No Connect.
7	V_{DD1}/NC	Supply Voltage. 4.5 V to 5.5 V. This is the supply voltage for the isolated side of the AD7400A and is relative to GND_1. No Connect (NC). If desired, Pin 7 of the SOIC device may be allowed to float. It should not be tied to ground. The AD7400A will operate normally provided that the supply voltage is applied to Pin 1.
8	GND_1	Ground 1. This is the ground reference point for all circuitry on the isolated side.
9, 16	GND_2	Ground 2. This is the ground reference point for all circuitry on the nonisolated side.
11	MDAT	Serial Data Output. The single bit modulator output is supplied to this pin as a serial data stream. The bits are clocked out on the rising edge of the MCLKOUT output and are valid on the following MCLKOUT rising edge.
13	MCLKOUT	Main Clock Logic Output (10 MHz Typical). The bit stream from the modulator is valid on the rising edge of MCLKOUT.
14	V_{DD2}	Supply Voltage, 3 V to 5.5 V. This is the supply voltage for the nonisolated side and is relative to GND_2.

TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, using 20 kHz brickwall filter, unless otherwise noted.

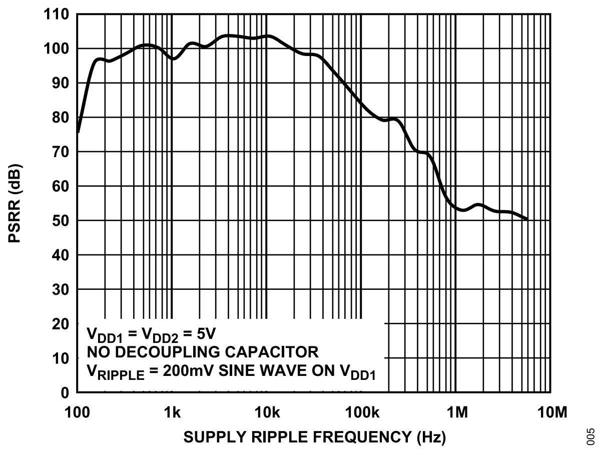


Figure 6. PSRR vs. Supply Ripple Frequency Without Supply Decoupling (1 MHz Filter Used)

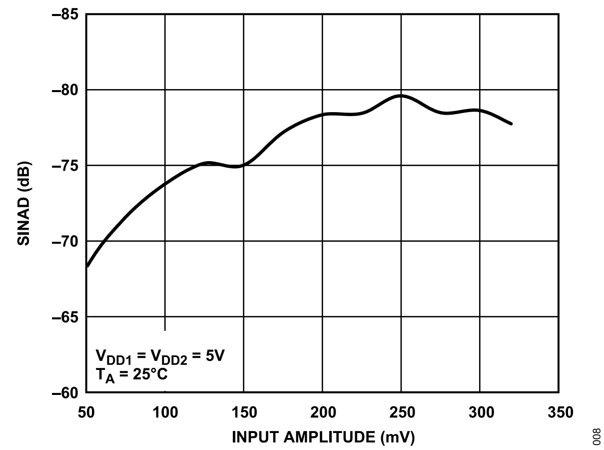


Figure 9. SINAD vs. V_{IN}

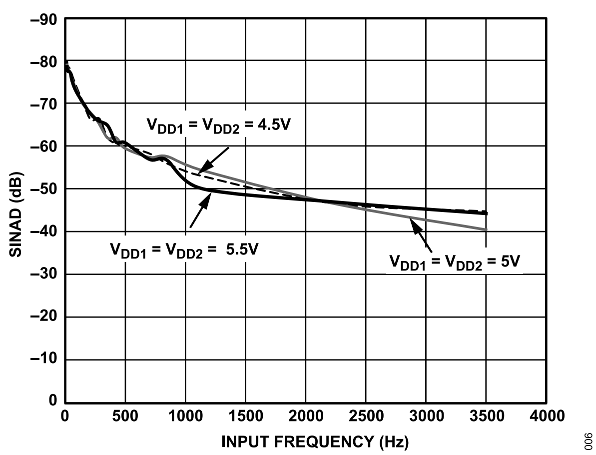


Figure 7. SINAD vs. Analog Input Frequency for Various Supply Voltages

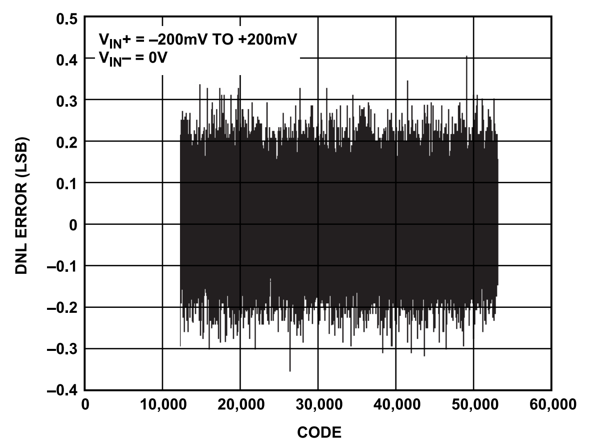


Figure 10. Typical DNL, ±200 mV Range (Using $Sinc^3$ Filter, 256 Decimation Rate)

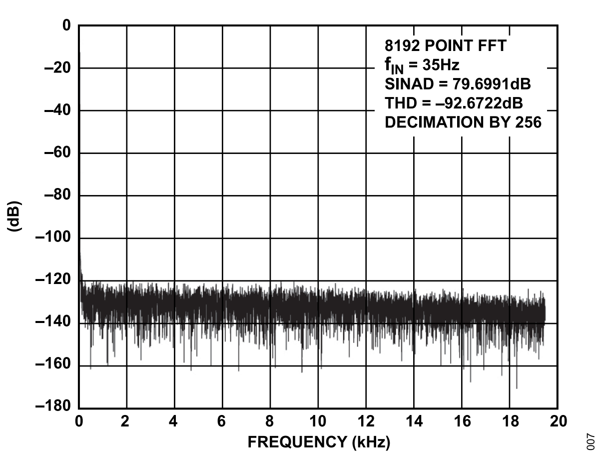


Figure 8. Typical FFT, ±200 mV Range (Using $Sinc^3$ Filter, 256 Decimation Rate)

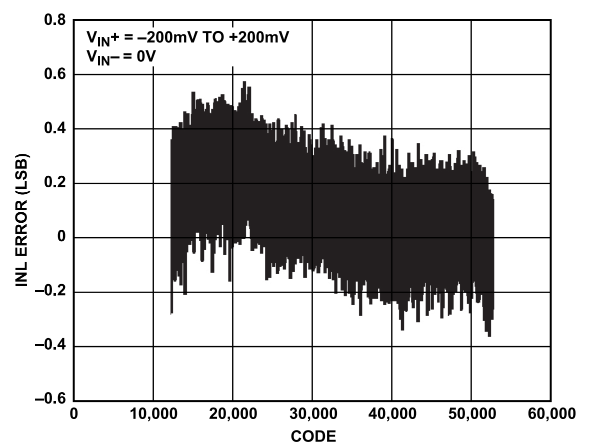


Figure 11. Typical INL, ±200 mV Range (Using $Sinc^3$ Filter, 256 Decimation Rate)

TYPICAL PERFORMANCE CHARACTERISTICS

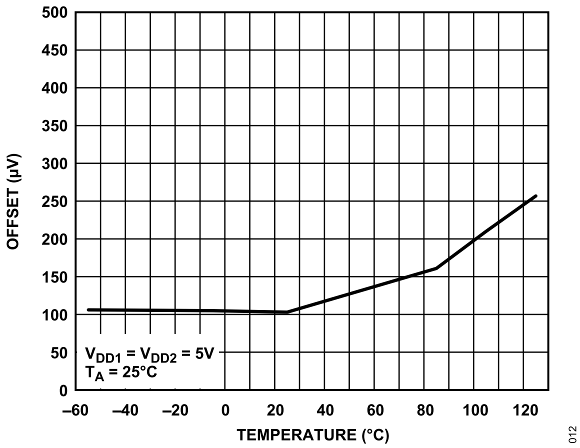


Figure 12. Offset Drift vs. Temperature

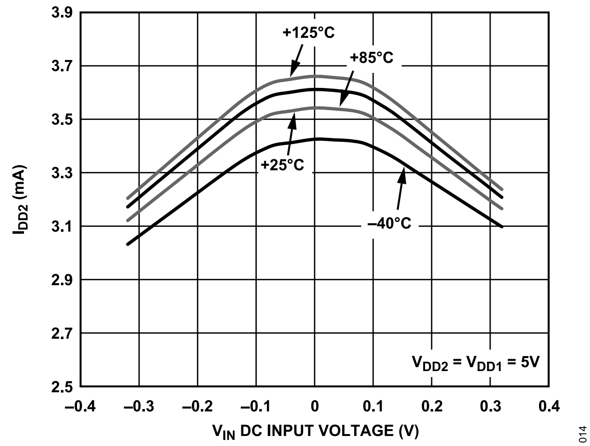


Figure 15. I_{DD2} vs. V_{IN} at Various Temperatures

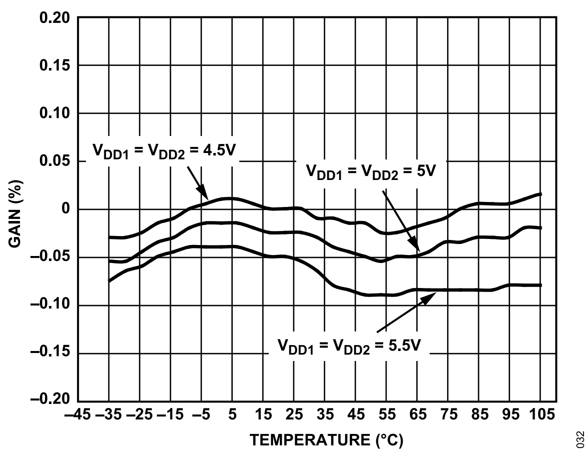


Figure 13. Gain Error Drift vs. Temperature for Various Supply Voltages

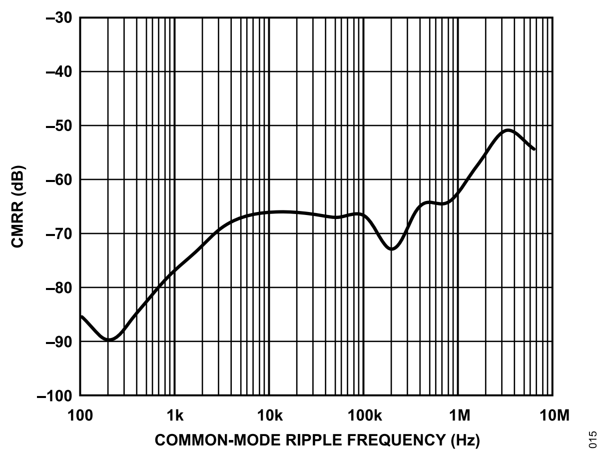


Figure 16. CMRR vs. Common-Mode Ripple Frequency

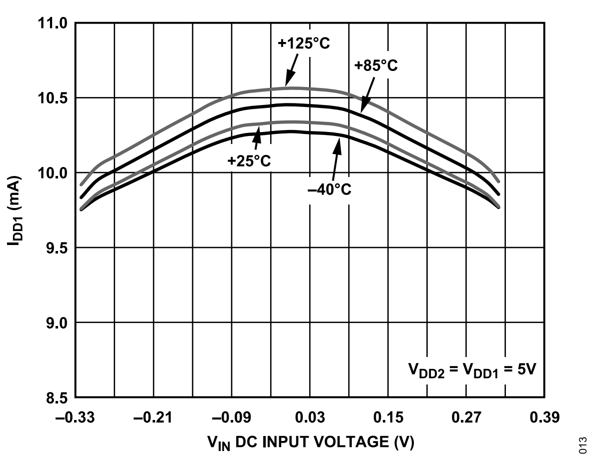


Figure 14. I_{DD1} vs. V_{IN} at Various Temperatures

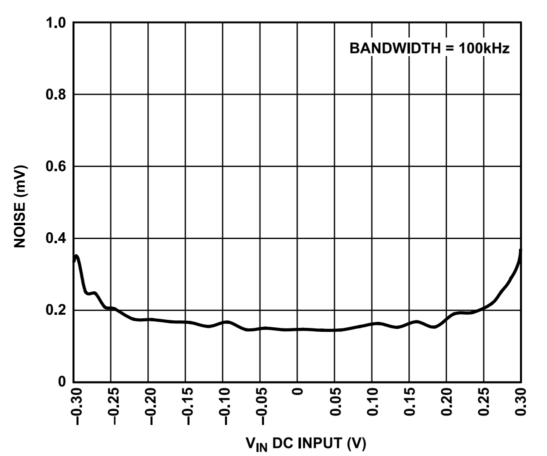


Figure 17. RMS Noise Voltage vs. V_{IN} DC Input

TYPICAL PERFORMANCE CHARACTERISTICS

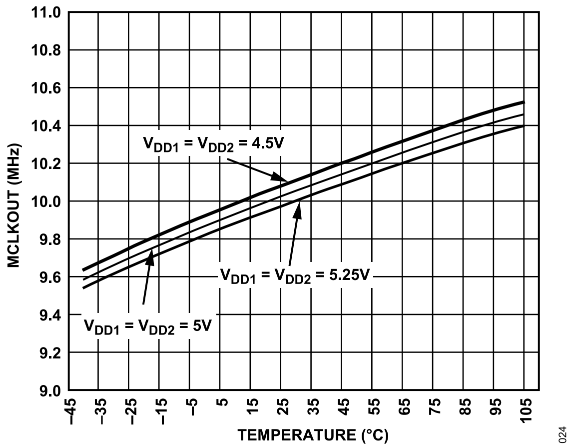


Figure 18. MCLKOUT vs. Temperature for Various Supplies

TERMINOLOGY

Differential Nonlinearity

Differential nonlinearity is the difference between the measured and the ideal 1 LSB change between any two adjacent codes in the ADC.

Integral Nonlinearity

Integral nonlinearity is the maximum deviation from a straight line passing through the endpoints of the ADC transfer function. The endpoints of the transfer function are specified negative full scale, −250 mV (V_{IN}+ − V_{IN}−), Code 7169, and specified positive full scale, +250 mV (V_{IN}+ − V_{IN}−), Code 58,366 for the 16-bit level.

Offset Error

Offset is the deviation of the midscale code (Code 32,768 for the 16-bit level) from the ideal V_{IN}+ − V_{IN}− (that is, 0 V).

Gain Error

Gain error includes both positive full-scale gain error and negative full-scale gain error. Positive full-scale gain error is the deviation of the specified positive full-scale code (58,366 for the 16-bit level) from the ideal V_{IN}+ − V_{IN}− (+250 mV) after the offset error is adjusted out. Negative full-scale gain error is the deviation of the specified negative full-scale code (7169 for the 16-bit level) from the ideal V_{IN}+ − V_{IN}− (−250 mV) after the offset error is adjusted out. Gain error includes reference error.

Signal-to-Noise and Distortion (SINAD) Ratio

This ratio is the measured ratio of signal-to-noise and distortion at the output of the ADC. The signal is the rms amplitude of the fundamental. Noise is the sum of all nonfundamental signals up to half the sampling frequency (f_S/2), excluding dc. The ratio is dependent on the number of quantization levels in the digitization process: the more levels, the smaller the quantization noise. The theoretical signal-to-noise and distortion ratio for an ideal N-bit converter with a sine wave input is given by

$$\textit{Signal-to-Noise and Distortion} = (6.02N + 1.76)\ \text{dB} \tag{1}$$

Therefore, for a 12-bit converter, SINAD is 74 dB.

Effective Number of Bits (ENOB)

The ENOB is defined by

$$ENOB = (SINAD - 1.76)/6.02 \tag{2}$$

Total Harmonic Distortion (THD)

THD is the ratio of the rms sum of harmonics to the fundamental. For the AD7400A, it is defined as

$$THD\left(\text{dB}\right) = 20\log\frac{\sqrt{V_2{}^2 + V_3{}^2 + V_4{}^2 + V_5{}^2 + V_6{}^2}}{V_1} \tag{3}$$

where:
V_1 is the rms amplitude of the fundamental.
V_2, V_3, V_4, V_5, and V_6 are the rms amplitudes of the second through the sixth harmonics.

Peak Harmonic or Spurious Noise

Peak harmonic or spurious noise is defined as the ratio of the rms value of the next largest component in the ADC output spectrum (up to f_S/2, excluding dc) to the rms value of the fundamental. Normally, the value of this specification is determined by the largest harmonic in the spectrum, but for ADCs where the harmonics are buried in the noise floor, it is a noise peak.

Common-Mode Rejection Ratio (CMRR)

CMRR is defined as the ratio of the power in the ADC output at ±250 mV frequency, f, to the power of a 250 mV p-p sine wave applied to the common-mode voltage of V_{IN}+ and V_{IN}− of frequency f_S as

$$CMRR\ (\text{dB}) = 10\log(Pf/Pf_S) \tag{4}$$

where:
Pf is the power at frequency f in the ADC output.
Pf_S is the power at frequency f_S in the ADC output.

Power Supply Rejection Ratio (PSRR)

Variations in power supply affect the full-scale transition but not the converter linearity. PSRR is the maximum change in the specified full-scale (±250 mV) transition point due to a change in power supply voltage from the nominal value (see Figure 6).

Isolation Transient Immunity

The isolation transient immunity specifies the rate of rise/fall of a transient pulse applied across the isolation boundary beyond which clock or data is corrupted. (The AD7400A was tested using a transient pulse frequency of 100 kHz.)

THEORY OF OPERATION

CIRCUIT INFORMATION

The AD7400A isolated Σ-Δ modulator converts an analog input signal into a high speed (10 MHz typical), single-bit data stream; the time average of the single-bit data from the modulator is directly proportional to the input signal. Figure 21 shows a typical application circuit where the AD7400A is used to provide isolation between the analog input, a current sensing resistor, and the digital output, which is then processed by a digital filter to provide an N-bit word.

ANALOG INPUT

The differential analog input of the AD7400A is implemented with a switched capacitor circuit. This circuit implements a second-order modulator stage that digitizes the input signal into a 1-bit output stream. The sample clock (MCLKOUT) provides the clock signal for the conversion process as well as the output data-framing clock. This clock source is internal on the AD7400A. The analog input signal is continuously sampled by the modulator and compared to an internal voltage reference. A digital stream that accurately represents the analog input over time appears at the output of the converter (see Figure 19).

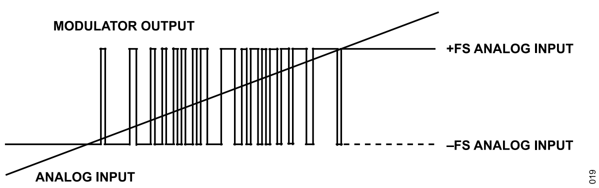


Figure 19. Analog Input vs. Modulator Output

A differential signal of 0 V ideally results in a stream of 1s and 0s at the MDAT output pin. This output is high 50% of the time and low 50% of the time. A differential input of 200 mV produces a stream of 1s and 0s that are high 81.25% of the time (for a +250 mV input, the output stream is high 89.06% of the time). A differential input of −200 mV produces a stream of 1s and 0s that are high 18.75% of the time (for a −250 mV input, the output stream is high 10.94% of the time).

A differential input of 320 mV ideally results in a stream of all 1s. This is the absolute full-scale range of the AD7400A, while 250 mV is the specified full-scale range, as shown in Table 8.

Table 8. Analog Input Range

Analog Input	Voltage Input
Full-Scale Range	+640 mV
Positive Full Scale	+320 mV
Positive Typical Input Range	+250 mV
Positive Specified Input Range	+200 mV
Zero	0 mV
Negative Specified Input Range	−200 mV
Negative Typical Input Range	−250 mV
Negative Full Scale	−320 mV

To reconstruct the original information, this output needs to be digitally filtered and decimated. A $Sinc^3$ filter is recommended because this is one order higher than that of the AD7400A modulator. If a 256 decimation rate is used, the resulting 16-bit word rate is 39 kHz, assuming a 10 MHz internal clock frequency. Figure 20 shows the transfer function of the AD7400A relative to the 16-bit output.

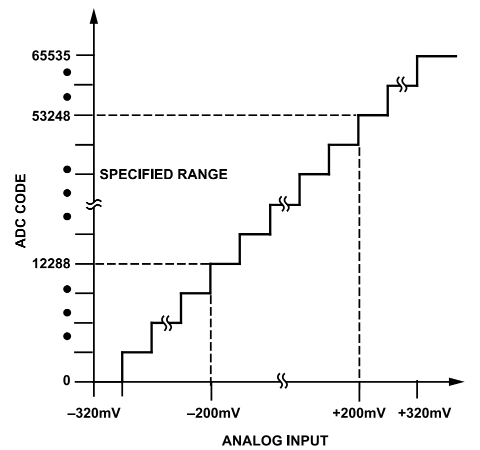


Figure 20. Filtered and Decimated 16-Bit Transfer Characteristic

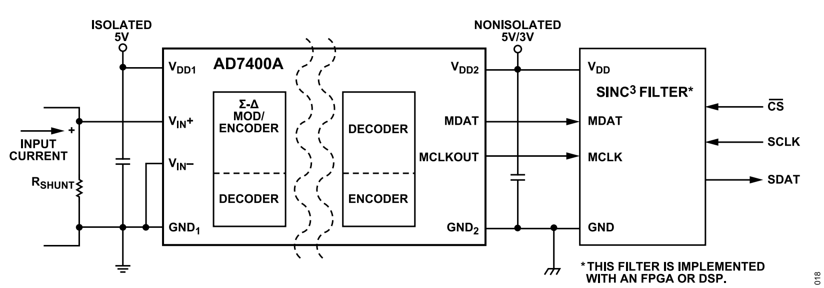


Figure 21. Typical Application Circuit

THEORY OF OPERATION

DIFFERENTIAL INPUTS

The analog input to the modulator is a switched capacitor design. The analog signal is converted into charge by highly linear sampling capacitors. A simplified equivalent circuit diagram of the analog input is shown in Figure 22. A signal source driving the analog input must be able to provide the charge onto the sampling capacitors every half MCLKOUT cycle and settle to the required accuracy within the next half cycle.

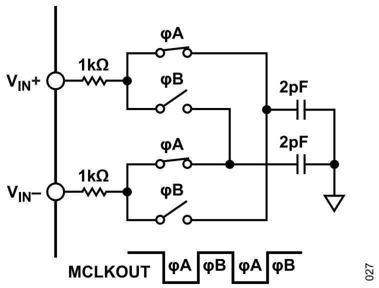


Figure 22. Analog Input Equivalent Circuit

Because the AD7400A samples the differential voltage across its analog inputs, low noise performance is attained with an input circuit that provides low common-mode noise at each input. The amplifiers used to drive the analog inputs play a critical role in attaining the high performance available from the AD7400A.

When a capacitive load is switched onto the output of an op amp, the amplitude drops momentarily. The op amp tries to correct the situation and, in the process, hits its slew rate limit. This nonlinear response, which can cause excessive ringing, can lead to distortion. To remedy the situation, a low-pass RC filter can be connected between the amplifier and the input to the AD7400A. The external capacitor at each input aids in supplying the current spikes created during the sampling process, and the resistor isolates the op amp from the transient nature of the load.

The recommended circuit configuration for driving the differential inputs to achieve best performance is shown in Figure 23. A capacitor between the two input pins sources or sinks charge to allow most of the charge that is needed by one input to be effectively supplied by the other input. The series resistor again isolates any op amp from the current spikes created during the sampling process. Recommended values for the resistors and capacitor are 22 Ω and 47 pF, respectively.

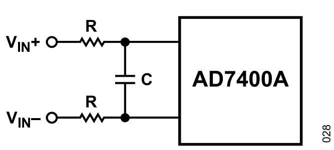


Figure 23. Differential Input RC Network

CURRENT SENSING APPLICATIONS

The AD7400A is ideally suited for current sensing applications where the voltage across a shunt resistor is monitored. The load current flowing through an external shunt resistor produces a voltage at the input terminals of the AD7400A. The AD7400A provides isolation between the analog input from the current sensing resistor and the digital outputs. By selecting the appropriate shunt resistor value, a variety of current ranges can be monitored.

Choosing R_{SENSE}

The shunt resistor values used in conjunction with the AD7400A are determined by the specific application requirements in terms of voltage, current, and power. Small resistors minimize power dissipation, while low inductance resistors prevent any induced voltage spikes, and good tolerance devices reduce current variations. The final values chosen are a compromise between low power dissipation and good accuracy. Low value resistors have less power dissipated in them, but higher value resistors may be required to use the full input range of the ADC, thus achieving maximum SNR performance.

When the peak sense current is known, the voltage range of the AD7400A (±200 mV) is divided by the maximum sense current to yield a suitable shunt value. If the power dissipation in the shunt resistor is too large, the shunt resistor can be reduced, in which case, less of the ADC input range is used. Using less of the ADC input range results in performance that is more susceptible to noise and offset errors because offset errors are fixed and are thus more significant when smaller input ranges are used.

R_{SENSE} must be able to dissipate the I2R power losses. If the power dissipation rating of the resistor is exceeded, its value may drift or the resistor may be damaged, resulting in an open circuit. This can result in a differential voltage across the terminals of the AD400A in excess of the absolute maximum ratings (see Table 6). If I_{SENSE} has a large high frequency component, take care to choose a resistor with low inductance.

VOLTAGE SENSING APPLICATIONS

The AD7400A can also be used for isolated voltage monitoring. For example, in motor control applications, it can be used to sense bus voltage. In applications where the voltage being monitored exceeds the specified analog input range of the AD7400A, a voltage divider network can be used to reduce the voltage being monitored to the required range.

DIGITAL FILTER

The overall system resolution and throughput rate is determined by the filter selected and the decimation rate used. The higher the decimation rate, the greater the system accuracy, as illustrated in Figure 24. However, there is a tradeoff between accuracy and throughput rate and, therefore, higher decimaltion rates result in lower throughput solutions.

THEORY OF OPERATION

A Sinc^3 filter is recommended for use with the AD7400A. This filter can be implemented on an FPGA or a DSP.

$$H\left(z\right) = \left(\frac{\left(1 - z^{DR}\right)}{\left(1 - z^{-1}\right)}\right)^3 \quad (5)$$

where *DR* is the decimation rate.

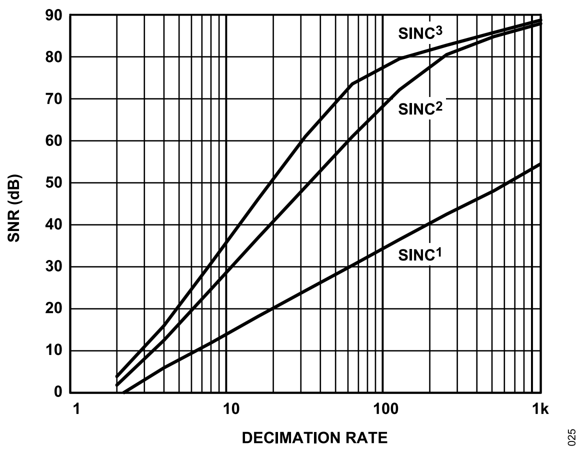


Figure 24. SNR vs. Decimation Rate for Different Filter Types

The following Verilog code provides an example of a Sinc^3 filter implementation on a Xilinx® Spartan-II 2.5 V FPGA. This code can possibly be compiled for another FPGA, such as an Altera® device. Note that the data is read on the negative clock edge in this case, although it can be read on the positive edge, if preferred. Figure 24 shows the effect of using different decimation rates with various filter types.

```
/*`Data is read on negative clk edge*/ mod▶
ule DEC256SINC24B(mdata1, mclk1, reset, DATA);
input  mclk1;        /*used to clk filter*/
input  reset;    /*used to reset filter*/
input  mdata1;           /*ip data to be fil▶
tered*/
output [15:0] DATA;        /*filtered op*/
integer location; integer info_file;
reg [23:0]        ip_data1;
reg [23:0]        acc1;
reg [23:0]        acc2;
reg [23:0]        acc3;
reg [23:0]        acc3_d1;
reg [23:0]        acc3_d2;
reg [23:0]        diff1;
reg [23:0]        diff2;
reg [23:0]        diff3;
reg [23:0]        diff1_d;
reg [23:0]        diff2_d;
reg [15:0]        DATA;
reg [7:0]        word_count;
reg word_clk;
reg init;
```

```
/*Perform the Sinc ACTION*/
always @ (mdata1)
if(mdata1==0)
     ip_data1 <= 0;    /
* change from a 0 to a -1 for 2's comp */  else

     ip_data1 <= 1;
/*ACCUMULATOR (INTEGRATOR) Perform the accumu▶
lation (IIR) at the speed of the modulator.
```

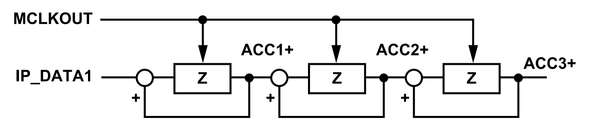


Figure 25. Accumulator

```
Z = one sample delay
MCLKOUT = modulators conversion bit rate */
always @ (negedge mclk1 or posedge re▶
set) if (reset)
  begin
   /*initialize acc registers on reset*/
  acc1 <= 0;
  acc2 <= 0;
  acc3 <= 0;
  end
else
  begin
   /*perform accumulation process*/
  acc1 <= acc1 + ip_data1;
  acc2 <= acc2 + acc1;
  acc3 <= acc3 + acc2;
  end
/*DECIMATION STAGE (MCLKOUT/ WORD_CLK) */
always @ (posedge mclk1 or posedge re▶
set) if (reset)
      word_count <= 0;
else
      word_count <= word_count + 1;
always @ (word_count)
word_clk <= word_count[7];
/*DIFFERENTIATOR (including decimation stage)
Perform the differentia▶
tion stage (FIR) at a lower speed.
```

THEORY OF OPERATION

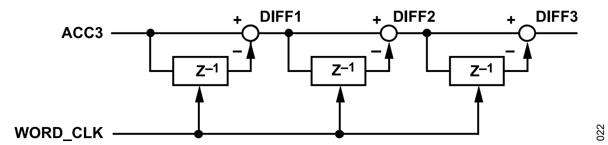


Figure 26. Differentiator

```
Z = one sample delay
WORD_CLK = output word rate
*/


always @ (posedge word_clk or posedge re▶
set) if(reset)
  begin
  acc3_d2 <= 0;
  diff1_d <= 0;
  diff2_d <= 0;
  diff1 <= 0;
  diff2 <= 0;
  diff3 <= 0;
  end

else
  begin
  diff1 <= acc3 - acc3_d2;
  diff2 <= diff1 - diff1_d;
  diff3 <= diff2 - diff2_d;
  acc3_d2 <= acc3;
  diff1_d <= diff1;
  diff2_d <= diff2;
  end
```

```
/* Clock the Sinc output into an output regis▶
ter
```

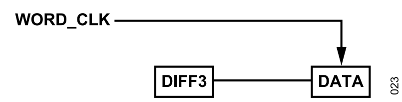


Figure 27. Clocking Sinc Output into an Output Register

```
WORD_CLK = output word rate */

always @ (posedge word_clk) begin

DATA[15] <= diff3[23];
DATA[14] <= diff3[22];
DATA[13] <= diff3[21];
DATA[12] <= diff3[20];
DATA[11] <= diff3[19];
DATA[10] <= diff3[18];
DATA[9]  <= diff3[17];
DATA[8]  <= diff3[16];
DATA[7]  <= diff3[15];
DATA[6]  <= diff3[14];
DATA[5]  <= diff3[13];
DATA[4]  <= diff3[12];
DATA[3]  <= diff3[11];
DATA[2]  <= diff3[10];
DATA[1]  <= diff3[9];
DATA[0]  <= diff3[8];
end
endmodule
```

APPLICATIONS INFORMATION

GROUNDING AND LAYOUT

Supply decoupling with a value of 100 nF is strongly recommended on both V_{DD1} and V_{DD2}. Decoupling on one or both V_{DDx} pins does not significantly affect performance. In applications involving high common-mode transients, ensure that board coupling across the isolation barrier is minimized. Furthermore, the board layout should be designed so that any coupling that occurs equally affects all pins on a given component side. Failure to ensure this may cause voltage differentials between pins to exceed the absolute maximum ratings of the device, thereby leading to latch-up or permanent damage. Any decoupling used should be placed as close to the supply pins as possible.

Series resistance in the analog inputs should be minimized to avoid any distortion effects, especially at high temperatures. If possible, equalize the source impedance on each analog input to minimize offset. Beware of mismatch and thermocouple effects on the analog input PCB tracks to reduce offset drift.

EVALUATING THE AD7400A PERFORMANCE

An AD7400A evaluation board is available with split ground planes and a board split beneath the AD7400A package to ensure isolation. This board allows access to each pin on the device for evaluation purposes.

The evaluation board package includes a fully assembled and tested evaluation board, documentation, and software for controlling the board from the PC via the EVAL-CED1Z. The software also includes a $SINC^3$ filter implemented on an FPGA. The evaluation board is used in conjunction with the EVAL-CED1Z board and can be used as a standalone board. The software allows the user to perform ac (fast Fourier transform) and dc (histogram of codes) tests on the AD7400A. The software and documentation are on a CD that ships with the evaluation board.

OUTLINE DIMENSIONS

Package Drawing (Option)	Package Type	Package Description
RW-16	SOIC_W	16-Lead Standard Small Outline Package

For the latest package outline information and land patterns (footprints), go to Package Index.

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Packing Quantity	Package Option
AD7400AYRWZ	−40°C to +125°C	16-Lead Standard Small Outline Package (SOIC_W)	Tube, 47	RW-16
AD7400AYRWZ-RL	−40°C to +125°C	16-Lead Standard Small Outline Package (SOIC_W)	Reel, 1000	RW-16

[1] Z = RoHS Compliant Part.

EVALUATION BOARDS

Model[1]	Description
EVAL-AD7400AEDZ	Standalone Evaluation Board
EVAL-CED1Z	Development Board

[1] Z = RoHS Compliant Part.