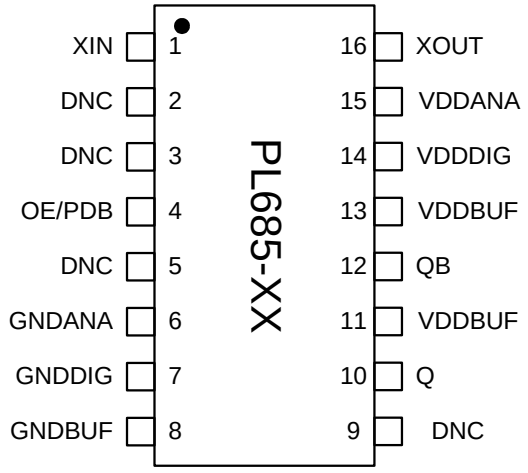
# 19MHz to 800MHz Low Phase-Noise XO

## FEATURES

- < 0.5ps RMS phase jitter (12kHz to 20MHz) at 622.08MHz
- 30ps max peak to peak period jitter
- Ultra Low-Power Consumption
  - o < 90 mA @622MHz PECL output
  - o <10μA at Power Down (PDB) Mode
- Input Frequency:
  - o Fundamental Crystal: 19MHz to 44MHz
- Output Frequency:
  - o 19MHz to 800MHz output.
- Output types: PECL.
- Programmable OE input polarity selection.
- Power Supply: 3.3V, ±10%
- Operating Temperature Ranges:
  - o Commercial: 0°C to 70°C
  - o Industrial: -40°C to 85°C
- Available in Die or Wafer

## PIN CONFIGURATION




**TSSOP-16L**

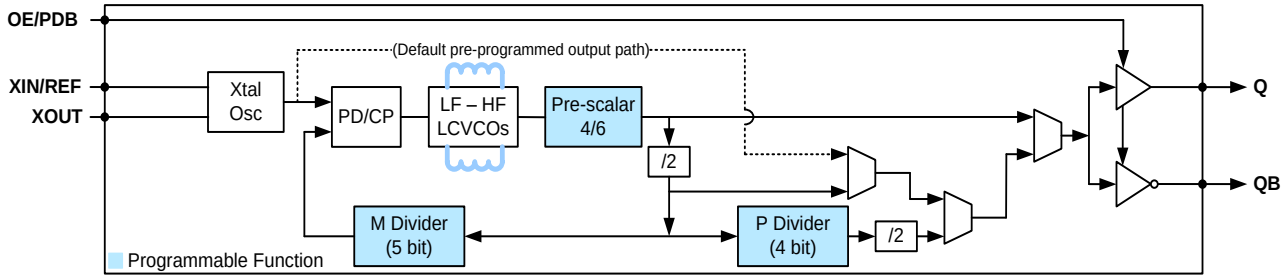
## DESCRIPTION

The PL685 is a Dual LC core monolithic IC clock, capable of maintaining sub-1ps RMS phase jitter, while covering a wide frequency output range up to 800MHz, without the use of external components. The high performance and high frequency output is achieved using a low cost fundamental crystal of between 19MHz and 44 MHz. The PL685 family is designed to address the demanding requirements of high performance applications such Fiber Channel, serial ATA, Ethernet, SAN, SONET/SDH, etc.

## OUTPUT ENABLE CONTROL

| OE Select (Programmable) | OE | State |
|---|---|---|
| 0 | 0 (Default) | Output enabled |
| | 1 | Tri-state |
| 1 (Default) | 0 | Tri-state |
| | 1 (Default) | Output enabled |

## BLOCK DIAGRAM



## PIN ASSIGNMENT

| Name | Pin # | Type | Description |
|---|---|---|---|
| XIN | 1 | I | Crystal input connection. |
| DNC | 2, 3, 5, 9 | - | Do Not Connect. |
| OE/PDB | 4 | I | This pin may be programmed as output enable (OE), or power-down (PDB) pin. This pin incorporates an Internal pull-up resistor of 60KΩ for OE, and PDB, operations. |
| GND_ANA | 6 | P | GND connection for analog circuitry. |
| GND_DIG | 7 | P | GND connection for digital circuitry. |
| GND_BUF | 8 | P | GND connection for buffer circuitry. |
| Q | 10 | O | True Output buffer. |
| QB | 12 | O | Complementary Output buffer. |
| VDD_BUF | 11, 13 | P | VDD connection for buffer circuitry. |
| VDD_DIG | 14 | P | VDD connection for digital circuitry. |
| VDD_ANA | 15 | P | VDD connection for analog circuitry. |
| XOUT | 16 | P | Output connection to crystal. |

## OPTION SELECTION TABLE

PL685 is a fully programmable clock IC. However, for ordering convenience, the following part numbers have been created for when simple multiplication is used, for your convenience. When other features of the IC are exercised (i.e. reverse polarity on OE, power down, etc.), another 3-digit code is used to identify the functionality.

| Input Crystal Frequency Range (MHz) | Multiplication Factor | Output Frequency Range (MHz) | | Part # |
|---|---|---|---|---|
| | | Low Limit | High Limit | |
| 33.750000 ~ 40.000000 | X20 | 675.00 | 800.00 | PL685-P8-020 |
| 33.333333 ~ 42.187500 | X16 | 533.33 | 675.00 | PL685-P8-168 |
| 32.142857 ~ 38.095238 | X14 | 450.00 | 533.33 | PL685-P8-148 |
| 33.333333 ~ 37.500000 | X12 | 400.00 | 450.00 | PL685-P8-128 |
| 33.750000 ~ 40.000000 | X10 | 337.50 | 400.00 | PL685-P8-108 |
| 33.333333 ~ 42.187500 | X8 | 266.67 | 337.50 | PL685-P8-088 |
| 32.142857 ~ 38.095238 | X7 | 225.00 | 266.67 | PL685-P8-078 |
| 33.333333 ~ 37.500000 | X6 | 200.00 | 225.00 | PL685-P8-068 |
| 33.750000 ~ 40.000000 | X5 | 168.75 | 200.00 | PL685-P8-058 |
| 33.333333 ~ 42.187500 | X4 | 133.33 | 168.75 | PL685-P8-048 |
| 32.142857 ~ 38.095238 | X3.5 | 112.50 | 133.33 | PL685-P8-358 |
| 33.333333 ~ 37.500000 | X3 | 100.00 | 112.50 | PL685-P8-038 |
| 33.750000 ~ 40.000000 | X2.5 | 84.375 | 100.00 | PL685-P8-258 |
| 32.812500 ~ 42.187500 | X2 | 65.625 | 84.375 | PL685-P8-028 |

Common functionality for packaged parts in the above table:

- OE function active high polarity.
- Crystal Cload is 12pF.

Please inform your Sales representative for active low OE functionality.

## FUNCTIONAL DESCRIPTION

PL685 family of products is an advanced, programmable LCVCO clock IC that is designed to meet the most stringent performance specifications for phase noise, jitter, and power consumption.

There are two main types of VCOs, a) Ring Oscillator, b) LC Tank oscillator. An LCVCO is made up of LC tank oscillator. Although a Ring Oscillator has very good performance, and has a good tuning range, its phase noise and jitter performance, in particular at higher frequencies, degrades.

On the other hand, an LCVCO has an outstanding phase noise and jitter performance, even at higher frequencies. PL685 family of products takes advantage of this state of the art technology, and incorporates the LC tank on-chip, for optimal performance.

PL685 family exhibit very low phase noise/phase jitter and peak to peak jitter, wide tuning range, and very low-power. All members of the PL685 family accept a low-cost fundamental crystal input of 19MHz to 44MHz or a reference clock input of up to 800MHz and its flexible core is capable of producing any output frequency between 19MHz to 800MHz.

### PLL Programming

The PLL in the PL685 family is fully programmable. The PLL is equipped with a Prescaler to divide down the VCO frequency, and a 5-bit VCO frequency feedback loop divider (M-Counter). The output of the PLL is transferred to a 4-bit post VCO divider (P-Counter), to achieve the desired output frequency.

### OE (Output Enable)

The OE pin in PL685 family, through programming, can be configured to support OE pin activation with a logic '1' or logic '0', to provide you with the desired enable polarity.

| OE Select (Programmable) | OE | State |
|---|---|---|
| 0 | 0 (Default) | Output enabled |
| | 1 | Tri-state |
| 1 (Default) | 0 | Tri-state |
| | 1 (Default) | Output enabled |

The OE pin incorporates a 60KΩ resistor to either pull-up or pull-down to the default state when the OE pin is left open.

## ELECTRICAL SPECIFICATIONS

### 1. ABSOLUTE MAXIMUM RATINGS

| PARAMETERS | SYMBOL | MIN | MAX | UNITS |
|---|---|---|---|---|
| Supply Voltage | $V_{DD}$ | | 4.6 | V |
| Input Voltage, dc | $V_I$ | -0.5 | $V_{DD}$+0.5 | V |
| Output Voltage, dc | $V_O$ | -0.5 | $V_{DD}$+0.5 | V |
| Storage Temperature | $T_S$ | -65 | 150 | °C |
| Ambient Operating Temperature (industrial temperature)* | $T_{AI}$ | -40 | 85 | °C |
| Ambient Operating Temperature (commercial temperature) | $T_{AC}$ | 0 | 70 | °C |
| Junction Temperature | $T_J$ | | 125 | °C |
| ESD Protection, Machine Model | | 200 | | V |
| ESD Protection, Human Body Model | | 2 | | kV |

Exposure of the device under conditions beyond the limits specified by Maximum Ratings for extended periods may cause permanent damage to the device and affect product reliability. These conditions represent a stress rating only, and functional operations of the device at these or any other conditions above the operational limits noted in this specification is not implied. *Operating temperature is guaranteed by design. Parts are tested to commercial grade only.

### 2. GENERAL ELECTRICAL SPECIFICATIONS

| PARAMETERS | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Supply Current, Dynamic | $I_{DDQ}$ | LVPECL, 622.08MHz, 3.3V | | | 90 | mA |
| Supply Current, Dynamic PDB Enabled | | PDB = 0, 3.3V | | | 10 | uA |
| Output Enable Time | $t_{OE}$ | OE logic 0 to logic 1, Ta=25° C. Add one clock period to this measurement for a usable clock output. | | | 50 | ns |
| Power Up Time | $T_{PU}$ | PDB logic 0 to logic 1, Ta=25° C | | | 10 | ms |
| Operating Voltage | $V_{DD}$ | LVPECL | 2.97 | | 3.63 | V |
| Power Up Ramp Rate | $t_{PU}$ | Time for $V_{DD}$ to reach 90% $V_{DD}$. Power ramp must be monotonic. | 0.1 | | 100 | ms |
| Auto-Calibration Time | $t_{AC}$ | At power up | | | 10 | ms |
| Output Clock Duty Cycle | | @ 50% of output waveform | 45 | 50 | 55 | % |

## 4. CRYSTAL SPECIFICATIONS

| PARAMETERS | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Crystal Resonator Frequency | $F_{XIN}$ | Parallel Fundamental Mode | 19 | | 44 | MHz |
| Crystal Cload | $C_{L\_Crystal}$ | $V_{DD}$ = 3.3V, programmable | 8 | | 12 | pF |
| Shunt Capacitance | $C_{0\_Crystal}$ | | | | 3.5 | pF |
| Recommended ESR | $R_E$ | AT cut , up to 40MHz | | | 50 | Ω |
| | | AT cut , up to 44MHz | | | 45 | Ω |

## 5. JITTER SPECIFICATIONS

| PARAMETERS | FREQUENCY | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| RMS Phase Jitter | 622.08MHz | 12kHz to 20MHz, XIN=38.88MHz | | | 0.5 | ps |
| Period Jitter, Pk-to-Pk | 622.08MHz | 10K cycles, XIN=38.88MHz | | | 30 | ps |

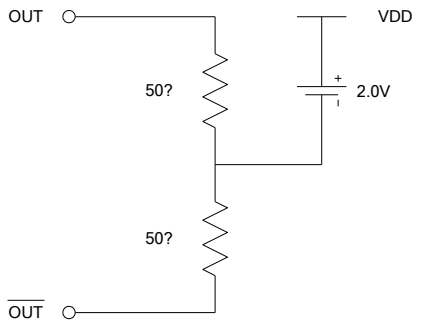
## 6. PHASE NOISE SPECIFICATIONS

| PARAMETERS | FREQUENCY | @10Hz | @100Hz | @1kHz | @10kHz | @100kHz | UNITS |
|---|---|---|---|---|---|---|---|
| Phase Noise, relative to carrier (typical) | 155.52MHz | -61 | -90 | -114 | -123 | -126 | dBc/Hz |
| | 622.08MHz | -46 | -77 | -101 | -111 | -114 | |

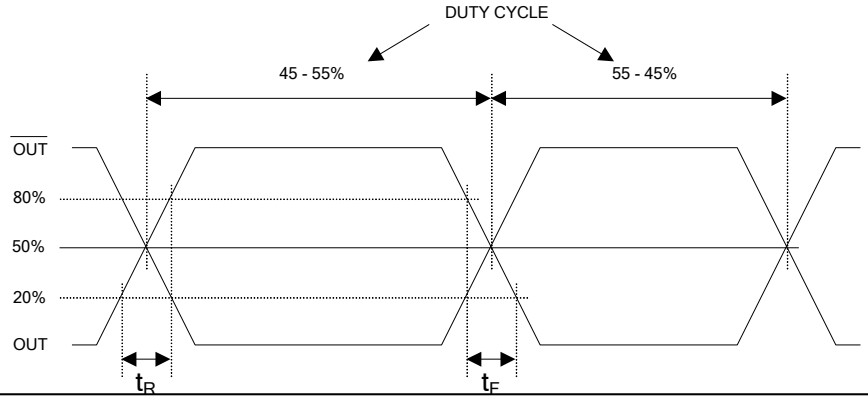
## 7. LVPECL OUTPUTS (Q, QB)

| PARAMETERS | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Output High Voltage | $V_{OH}$ | Q, QB<br>Standard LVPECL Termination, $V_{DD}$ = 3.3V | 2.275 | 2.350 | 2.420 | V |
| Output Low Voltage | $V_{OL}$ | | 1.490 | 1.600 | 1.680 | V |
| Output Frequency | $F_{out}$ | 3.3V | 19 | | 800 | MHz |
| Output Rise, Fall Times | $t_r$, $t_f$ | 20% - 80% of output waveform | | 300 | 500 | ps |
| Output Voltage Swing | $V_{pp}$ | Q, QB | 550 | 800 | 930 | mV |

LVPECL Levels Test Circuit




LVPECL Transistion Time Waveform



## LAYOUT RECOMMENDATIONS

The following guidelines are to assist you with a performance optimized PCB design:

### Signal Integrity and Termination Considerations

- Keep traces short!

- Trace = Inductor. With a capacitive load this equals ringing!

- Long trace = Transmission Line. Without proper termination this will cause reflections (looks like ringing).

- Design long traces (<1 inch) as “striplines” or “microstrips” with defined impedance.

- Match trace at one side to avoid reflections bouncing back and forth.

### Decoupling and Power Supply Considerations

- Place decoupling capacitors as close as possible to the $V_{DD}$ pin(s) to limit noise from the power supply

- Multiple $V_{DD}$ pins should be decoupled separately for best performance.

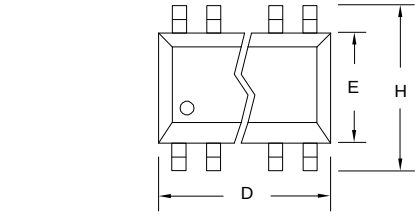
- Addition of a ferrite bead in series with $V_{DD}$ can help prevent noise from other board sources

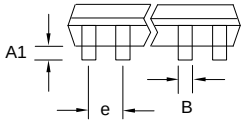
- Value of decoupling capacitor is frequency dependant. Typical values to use are 0.1μF for designs using frequencies < 50MHz and 0.01μF for designs using frequencies > 50MHz.

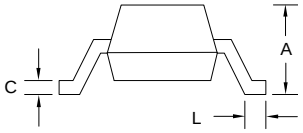
## PACKAGE DRAWINGS (GREEN PACKAGE COMPLIANT)

### TSSOP-16L

| Symbol | Dimension in MM | |
|---|---|---|
| | Min. | Max. |
| A | - | 1.20 |
| A1 | 0.05 | 0.15 |
| b | 0.19 | 0.30 |
| C | 0.09 | 0.20 |
| D | 4.90 | 5.10 |
| E | 4.30 | 4.50 |
| H | 6.20 | 6.60 |
| L | 0.45 | 0.75 |
| e | 0.65 BSC | |



## ORDERING INFORMATION

***For part ordering, please contact our Sales Department:***

2180 Fortune Drive, San Jose, CA 95131, USA

Tel: (408) 944-0800 Fax: (408) 474-1000

***PART NUMBER***

The order number for this device is a combination of the following:

Part number, Package type, Thickness and Operating temperature range

**PL685-XX-XXX XX**

**Part Number**

**Programming Code**

***Packaging Option***

*O = TSSOP*

**Temperature Range**

C=Commercial (0°C to 70°C)

I= Industrial (-45°C to +85°C)

| Part Number/Order Number | Marking† | Package Option |
|---|---|---|
| PL685-XX-XXXOC | P685-XX<br>XXX(I)<br>LLLLL | 16-Pin TSSOP (Tube) |
| PL685-XX-XXXOC-R | | 16-Pin TSSOP (Tape and Reel) |

† **Marking Notes:**

1) The "I" after the 3 digit programming code will be marked for Industrial Temperature grade products only. Commercial grade products will not have a character in this position.

2) LLLLL represents the production lot number