3.3 V Clock Synthesizer for DLP™ Systems

FEATURES

- **High-Performance Clock Synthesizer**
- **Uses a 20 MHz Crystal Input to Generate Multiple Output Frequencies**
- **Integrated Load Capacitance for 20 MHz Oscillator Reducing System Cost**
- **All PLL Loop Filter Components are Integrated**
- **Generates the Following Clocks:**
  - **REF CLK 20 MHz (Buffered)**
  - **XCG CLK 100 MHz With SSC**
  - **DMD CLK 200-400 MHz With Selectable SSC**
- **Very Low Period Jitter Characteristic:**
  - **±100 ps at 20 MHz Output**
  - **±75 ps at 100 MHz and 200–400 MHz Outputs**
- **Includes Spread-Spectrum Clocking (SSC), With Down Spread for 100 MHz and Center Spread for 200–400 MHz**
- **HCLK Differential Outputs for the 100 MHz and the 200–400 MHz Clock**
- **Operates From Single 3.3-V Supply**
- **Packaged in TSSOP20**
- **Characterized for the Industrial Temperature Range -40°C to 85°C**
- **ESD Protection Exceeds JESD22**
- **2000-V Human-Body Model (A114-C) – MIL-STD-883, Method 3015**

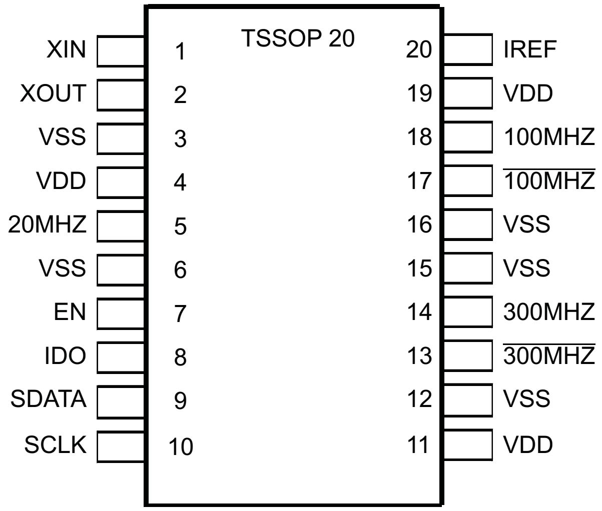
TYPICAL APPLICATIONS

- **Central Clock Generator for DLP™ Systems**

DESCRIPTION

The CDCDLP223 is a PLL-based high performance clock synthesizer that is optimized for use in DLP™ systems. It uses a 20 MHz crystal to generate the fundamental frequency and derives the frequencies for the 100 MHz HCLK and the 300 MHz HCLK output. Further, the CDCDLP223 generates a buffered copy of the 20 MHz Crystal Oscillator Frequency at the 20 MHz output terminal.

CDCDLP223 PIN ASSIGNMENTS



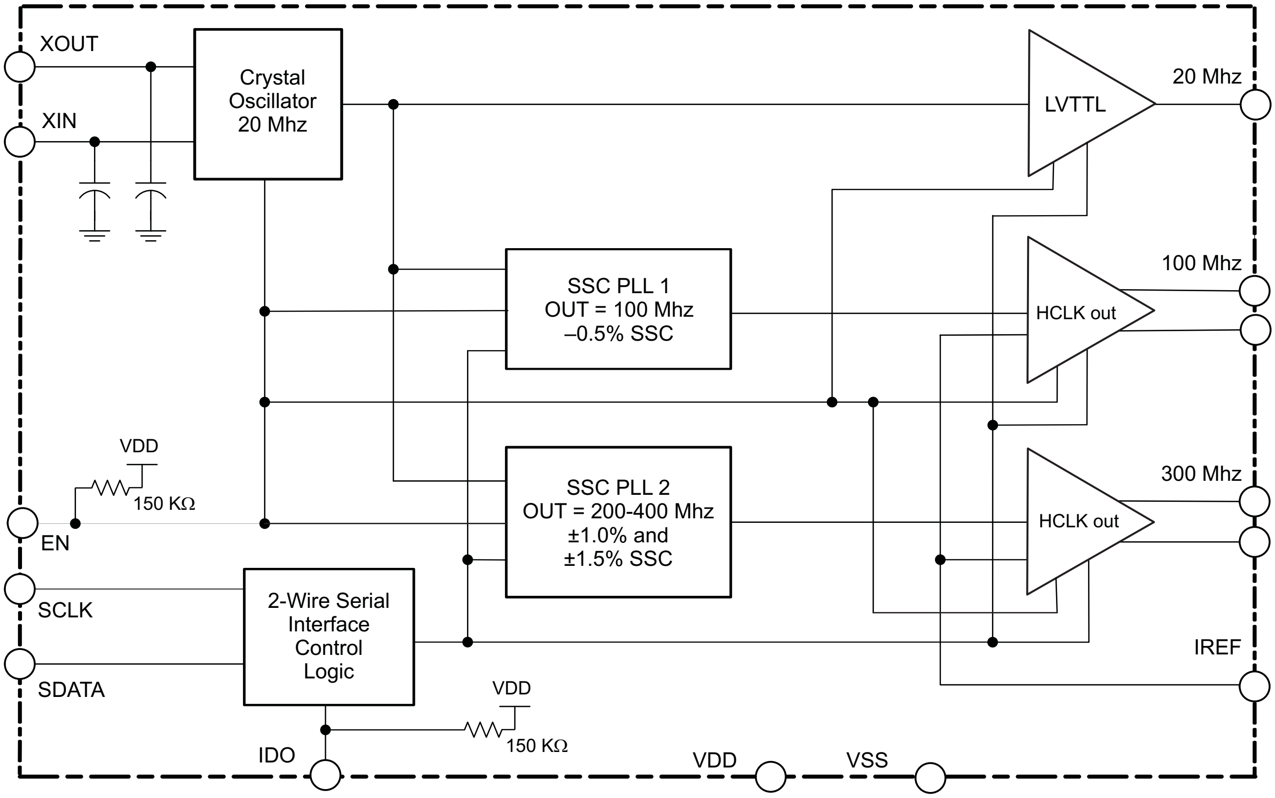
The 100 MHz HCLK output provides the reference clock for the XDR Clock Generator (CDCD5704). Spread-spectrum clocking with 0.5% down spread, which reduces Electro Magnetic Interference (EMI), is applied in the default configuration. The spread-spectrum clocking (SSC) is turned on and off via the serial control interface.

The 300 MHz HCLK output provides a 200-400 MHz clock signal for the DMD Control Logic of the DLP™ Control ASIC. Frequency selection in 20 MHz steps is possible via the serial control interface. Spread-spectrum clocking with ±1.0% or ±1.5% center spread is applied, which can be disabled via the serial control interface

The CDCDLP223 features a fail safe start-up circuit, which enables the PLLs only if a sufficient supply voltage is applied and a stable oscillation is delivered from the crystal oscillator. After the crystal start-up time and the PLL stabilization time, all outputs are ready for use.

The CDCDLP223 works from a single 3.3-V supply and is characterized for operation from –40°C to 85°C.

FUNCTIONAL BLOCK DIAGRAM



TERMINAL FUNCTIONS

TERMINAL	PIN	TYPE	DESCRIPTION
XIN	1	I	Crystal oscillator input for 20-MHz crystal in parallel resonance
XOUT	2	O	Crystal oscillator output for 20-MHz crystal in parallel resonance
SDATA	9	I/O Open drain	Data I/O, 2-wire serial interface controller, internal 1-MΩ pullup
SCLK	10	I Interface Clock	Clock input, 2-wire serial interface controller, internal 1-MΩ pullup
20 MHz	5	O LVTTL	Clock output, 20 MHz (buffered output from crystal oscillator)
100 MHz	18	O HCLK	Clock output for XDR clock generator
$\overline{\text{100 MHz}}$	17	O $\overline{\text{HCLK}}$	Clock output for XDR clock generator
300 MHz	14	O HCLK	Clock output for DMD system
$\overline{\text{300 MHz}}$	13	O $\overline{\text{HCLK}}$	Clock output for DMD system
VDD	4,11,19	Power	3.3 V Power supply
VSS	3,6,12,15,16	Ground	Ground
IREF	20	O R_{REF} to GND	IREF pin for HCLK output drive-current biasing
EN	7	I LVTTL	Output enable, 20 MHz, 100 MHz and 200–400 MHz outputs, 150 kΩ pullup, default = logic high
IDO	8	I LVTTL	Sets 2-wire serial interface ID address bit A0, 150 kΩ pull-up resistor, default = logic high

Table 1. EN Pin (20 MHz, 100 MHz and 300 MHz Clocks)

EN PIN	DESCRIPTION
1	All HCLK outputs, and 20-MHz outputs enabled, detailed device configurations are determined by 2-wire serial interface settings.
0	All HCLK = true Hi-Z, both PLLs are powered down and 20-MHz output in Hi-Z and Crystal Oscillator disabled, EN overrides 2-wire serial interface settings.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) (1)

		VALUE	UNIT
V_{DD}	Supply voltage range	–0.5 to 4.6	V
V_I	Input voltage range (2)	–0.5 to VDD + 0.5	V
V_O	Output voltage range (2)	–0.5 to VDD + 0.5	V
	Input current ($V_I < 0$, $V_I > V_{DD}$)	±20	mA
I_O	Continuous output current	±17.5	mA
Tstg	Storage temperature range	–65 to 150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output negative voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

PACKAGE THERMAL IMPEDANCE FOR TSSOP20 PACKAGE (1)

Airflow (lfm)	θ_{JA} (°C/W)	θ_{JC} (°C/W)	θ_{JB} (°C/W)	Ψ_{JT} (°C/W)
0	83.0	32	54	0.25
150	77.9	–	–	
250	75.4	–	–	
500	71.4	–	–	

(1) The package thermal impedance is calculated in accordance with JESD 51 and JEDEC2S2P (high-k board).

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
T_A	Operating free-air temperature	-40		85	°C
V_{DD}	Supply voltage	3.0	3.3	3.6	V
V_{IH}	High level input voltage SDATA and SCLK	$0.7 \times V_{DD}$		V_{DD}	V
V_{IL}	Low level input voltage SDATA and SCLK	–0.15		$0.3 \times V_{DD}$	V
V_{IL}	Low level input voltage LVTTL			0.8	V
V_I	thresh Input Voltage threshold LVTTL		1.40		V
V_{IH}	High level input voltage LVTTL	2.0			V
I_{OH}	High-level output current LVTTL			–8	mA
I_{OL}	Low-level output current LVTTL			8	mA
I_{OH}	High-level output current HCLK/$\overline{\text{HCLK}}$			–20	mA
I_{OL}	Low-level output current HCLK/$\overline{\text{HCLK}}$			0	mA
t_{PU}	Power-up time for all VDDs to reach minimum specified voltage (power ramps must be monotonic)	0.05		500	ms

RECOMMENDED CRYSTAL SPECIFICATION (1)

		MIN	NOM	MAX	UNIT
f_{xtal}	Crystal input frequency (fundamental)		20		MHz
ESR	Effective series resistance			100	Ω
P_{drive}	Maximum power handling (drive level)	100			μW
C_L	Load capacitance		20		pF

(1) See DLP™ Control ASIC DDP2230 datasheet for additional requirements.

TIMING REQUIREMENTS(1)

over recommended ranges of supply voltage, load and operating free air temperature

PARAMETER		MIN	TYP	MAX	UNIT
XIN, XOUT REQUIREMENTS					
f_{XIN}	Frequency of crystal attached to XIN, XOUT, with C_L = 20 pF (2 × 40 pF) on-die capacitance		20		MHz
2 WIRE SERIAL INTERFACE REQUIREMENTS STANDARD MODE					
f_{SCLK}	SCLK frequency	0		100	kHz
$t_{h(START)}$	START hold time (see Figure 1)	4.0			µs
$t_{w(SCLL)}$	SCLK low-pulse duration (see Figure 1)	4.7			µs
$t_{w(SCLH)}$	SCLK high-pulse duration (see Figure 1)	4.0			µs
$t_{su(START)}$	START setup time (see Figure 1)	4.7			µs
$t_{h(SDATA)}$	SDATA hold time (see Figure 1)	0		3.45	µs
$t_{su(SDATA)}$	SDATA setup time (see Figure 1)	250			ns
$t_{r(SDATA)}$	SCLK / SDATA input rise time (see Figure 1)			1000	ns
$t_{f(SDATA)}$	SCLK / SDATA input fall time (see Figure 1)			300	ns
$t_{su(STOP)}$	STOP setup time (see Figure 1)	4.0			µs
t_{BUS}	Bus free time	4.7			µs
2 WIRE SERIAL INTERFACE REQUIREMENTS FAST MODE					
f_{SCLK}	SCLK frequency	0		400	kHz
$t_{h(START)}$	START hold time (see Figure 1)	0.6			µs
$t_{w(SCLL)}$	SCLK low-pulse duration (see Figure 1)	1.3			µs
$t_{w(SCLH)}$	SCLK high-pulse duration (see Figure 1)	0.6			µs
$t_{su(START)}$	START setup time (see Figure 1)	0.6			µs
$t_{h(SDATA)}$	SDATA hold time (see Figure 1)	0		0.9	µs
$t_{su(DATA)}$	SDATA setup time (see Figure 1)	100			ns
$t_{r(SDATA)}$	SCLK / SDATA input rise time (see Figure 1)	20		300	ns
$t_{f(SDATA)}$	SCLK / SDATA input fall time (see Figure 1)	20		300	ns
$t_{su(STOP)}$	STOP setup time (see Figure 1)	0.6			µs
t_{BUS}	Bus free time	1.3			µs

(1) The CDCDLP223 2-wire serial interface in Send-Mode meets both I^2C and SMBus *set up time* t_{su} and *hold time* t_h requirements.

APPLICATION INFORMATION

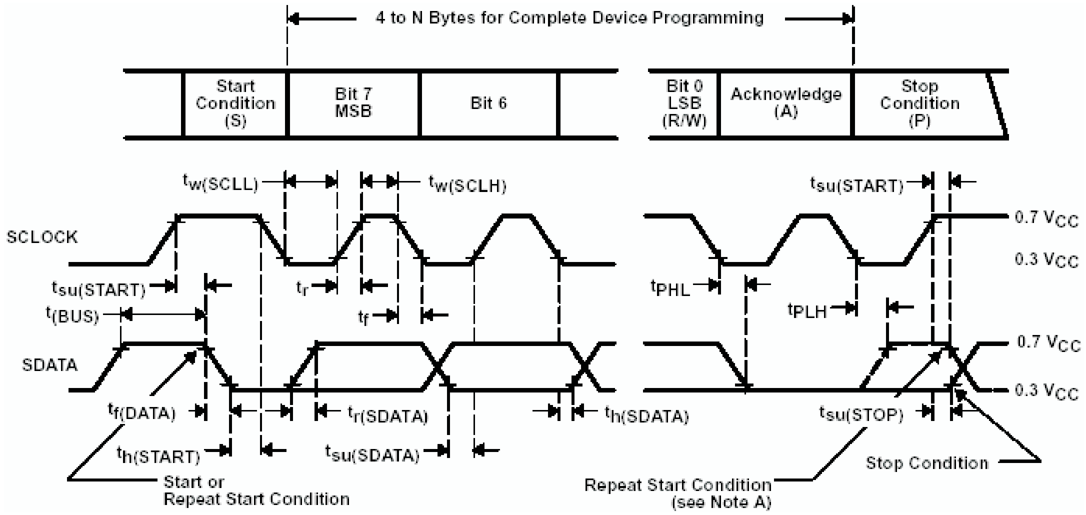


Figure 1. Timing Diagram, Serial Control Interface

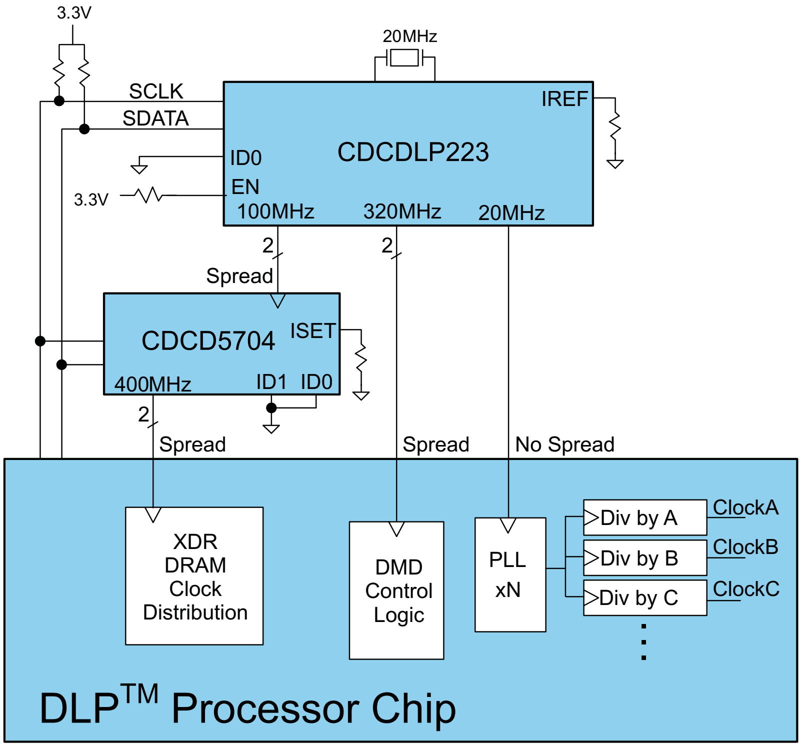
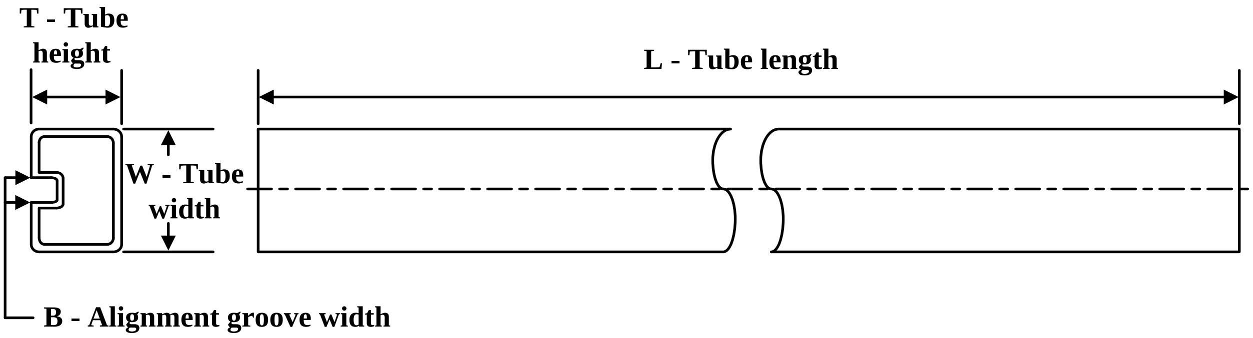


Figure 2. Typical CDCDLP223 Application

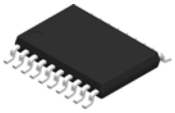
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
CDCDLP223PW	PW	TSSOP	20	70	530	10.2	3600	3.5

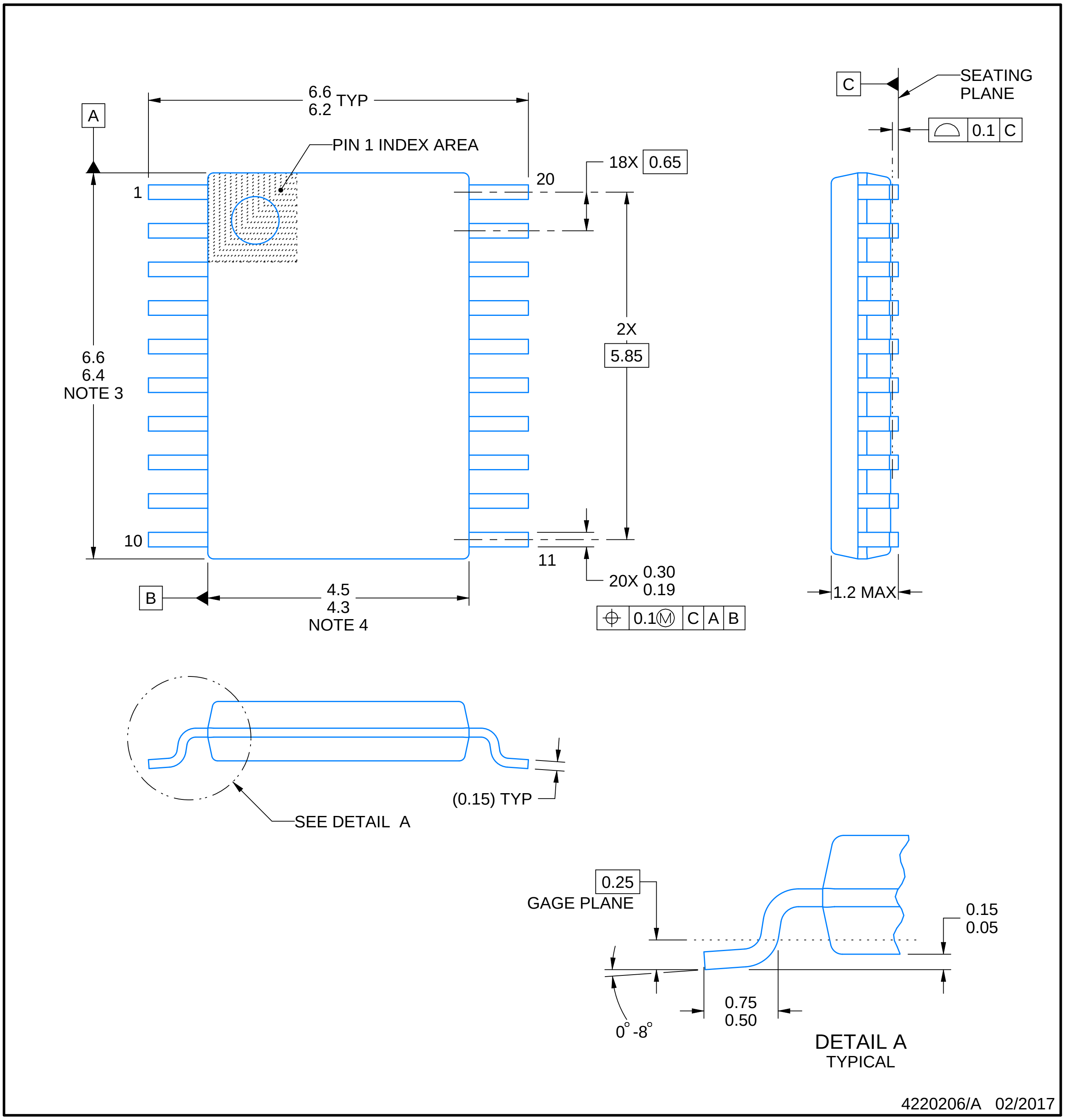
PACKAGE OUTLINE



PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



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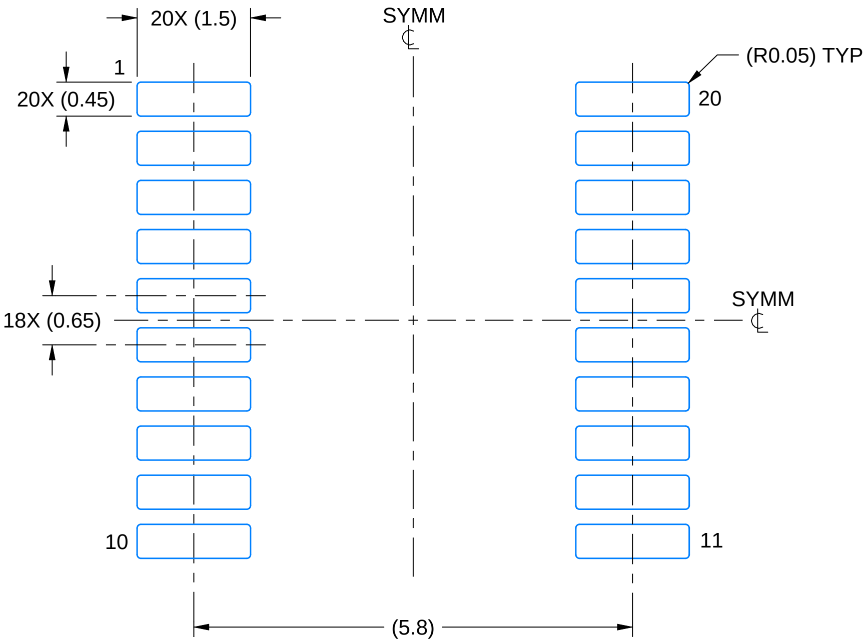
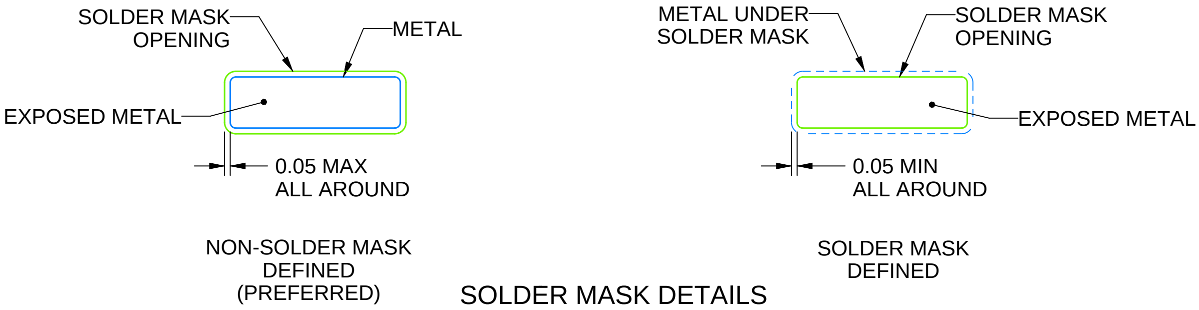
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

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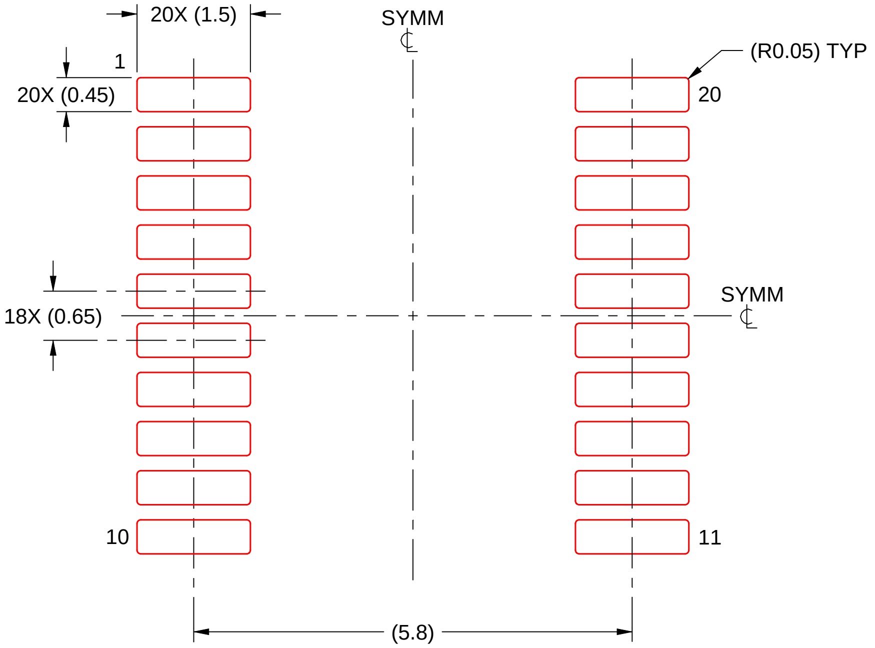
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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