

# 2.5V / 3.3V Differential 2:1 Mux Input to 1:6 LVPECL Clock/Data Fanout Buffer / Translator

Multi-Level Inputs w/ Internal Termination

## NB7L585

### Description

The NB7L585 is a differential 1:6 LVPECL Clock/Data distribution chip featuring a 2:1 Clock/Data input multiplexer with an input select pin. The  $IN_x/\overline{IN}_x$  inputs incorporate internal  $50\ \Omega$  termination resistors and will accept LVPECL, CML, or LVDS logic levels.

The NB7L585 produces six identical output copies of Clock or Data operating up to 5 GHz or 8 Gb/s, respectively. As such, NB7L585 is ideal for SONET, GigE, Fiber Channel, Backplane and other Clock/Data distribution applications.

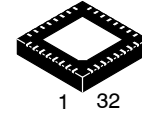
The NB7L585 is powered with either 2.5 V or 3.3 V supply and is offered in a low profile 5mm x 5mm 32-pin QFN package.

Application notes, models, and support documentation are available at [www.onsemi.com](http://www.onsemi.com).

The NB7L585 is a member of the GigaComm™ family of high performance clock products.

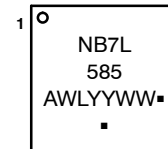
### Features

- Maximum Input Data Rate > 8 Gb/s
- Data Dependent Jitter < 15 ps
- Maximum Input Clock Frequency > 5 GHz
- Random Clock Jitter < 0.8 ps RMS
- Low Skew 1:6 LVPECL Outputs, 20 ps max
- 2:1 Multi-Level Mux Inputs
- 175 ps Typical Propagation Delay
- 55 ps Typical Rise and Fall Times
- Differential LVPECL Outputs, 800 mV peak-to-peak, typical
- Operating Range:  $V_{CC} = 2.375\text{ V to }3.6\text{ V}$  with  $GND = 0\text{ V}$
- Internal  $50\ \Omega$  Input Termination Resistors
- VREFAC Reference Output
- QFN-32 Package, 5mm x 5mm
- $-40^\circ\text{C to }+85^\circ\text{C}$  Ambient Operating Temperature
- These Devices are Pb-Free and are RoHS Compliant



QFN32  
MN SUFFIX  
CASE 488AM

### MARKING DIAGRAM



- A = Assembly Location
- WL = Wafer Lot
- YY = Year
- WW = Work Week
- = Pb-Free Package

(Note: Microdot may be in either location)

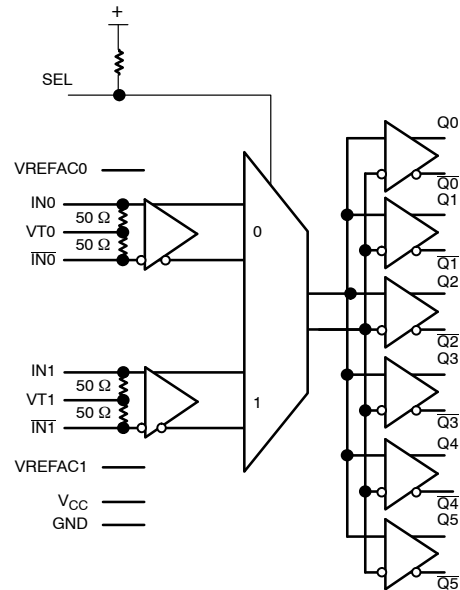


Figure 1. Simplified Block Diagram

### ORDERING INFORMATION

See detailed ordering and shipping information on page 8 of this data sheet.

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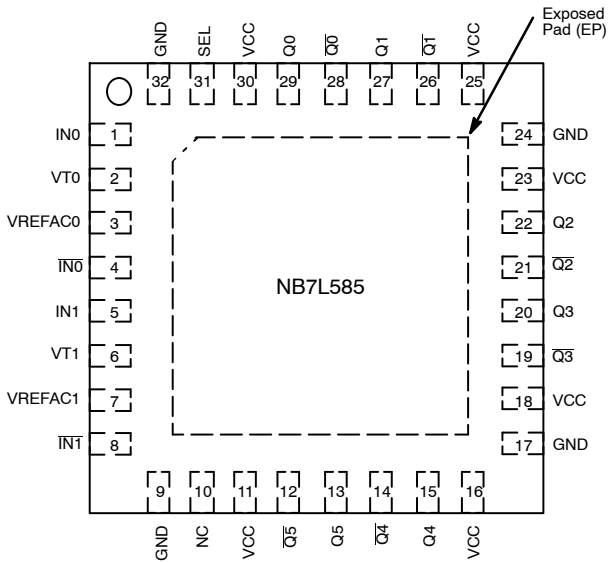


Figure 2. Pinout: QFN-32 (Top View)

Table 1. INPUT SELECT FUNCTION TABLE

SEL*	CLK Input Selected
0	IN0
1	IN1

\*Defaults HIGH when left open.

Table 2. PIN DESCRIPTION

Pin Number	Pin Name	I/O	Pin Description
1,4 5,8	IN0, $\overline{\text{IN0}}$ IN1, $\overline{\text{IN1}}$	LVPECL, CML, LVDS Input	Non-inverted, Inverted, Differential Data Inputs internally biased to $V_{CC}/2$
2,6	VT0, VT1		Internal 100 $\Omega$ Center-tapped Termination Pin for IN0 / $\overline{\text{IN0}}$ and IN1 / $\overline{\text{IN1}}$
31	SEL	LVTTTL/LVCMOS Input	Input Select pin; LOW for IN0 Inputs, HIGH for IN1 Inputs; defaults HIGH when left open
10	NC	-	No Connect
11, 16, 18 23, 25, 30	V <sub>CC</sub>	-	Positive Supply Voltage. All V <sub>CC</sub> pins must be connected to the positive power supply for correct DC and AC operation.
29, 28 27, 26 22, 21 20, 19 15, 14 13, 12	Q0, $\overline{\text{Q0}}$ Q1, $\overline{\text{Q1}}$ Q2, $\overline{\text{Q2}}$ Q3, $\overline{\text{Q3}}$ Q4, $\overline{\text{Q4}}$ Q5, $\overline{\text{Q5}}$	LVPECL Output	Non-inverted, Inverted Differential Outputs Note 1.
9, 17, 24, 32	GND		Negative Supply Voltage, connected to Ground
3 7	VREFAC0 VREFAC1	-	Output Voltage Reference for Capacitor-Coupled Inputs
-	EP	-	The Exposed Pad (EP) on the QFN-32 package bottom is thermally connected to the die for improved heat transfer out of package. The exposed pad must be attached to a heat-sinking conduit. The pad is electrically connected to the die, and must be electrically and thermally connected to GND on the PC board.

1. In the differential configuration when the input termination pins (VT0, VT1) are connected to a common termination voltage or left open, and if no signal is applied on INn/ $\overline{\text{INn}}$  input, then the device will be susceptible to self-oscillation.
2. All V<sub>CC</sub> and GND pins must be externally connected to a power supply for proper operation.

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**Table 3. ATTRIBUTES**

Characteristics		Value
ESD Protection	Human Body Model Machine Model	> 2 kV > 200 V
R <sub>PU</sub> – SEL Input Pullup Resistor		75 kΩ
Moisture Sensitivity (Note 3)	QFN–32	Level 1
Flammability Rating	Oxygen Index: 28 to 34	UL 94 V–0 @ 0.125 in
Transistor Count		288
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test		

3. For additional information, see Application Note AND8003/D.

**Table 4. MAXIMUM RATINGS**

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
V <sub>CC</sub>	Positive Power Supply	GND = 0 V		+4.0	V
V <sub>IO</sub>	Input/Output Voltage	GND = 0 V		–0.5 to V <sub>CC</sub> +0.5	V
V <sub>INPP</sub>	Differential Input Voltage  I <sub>N</sub> – I <sub>N</sub>			1.89	V
I <sub>IN</sub>	Input Current Through R <sub>T</sub> (50 Ω Resistor)			± 40	mA
I <sub>out</sub>	Output Current	Continuous Surge		50 100	mA
I <sub>VREFAC</sub>	VREFAC Sink or Source Current			± 1.5	mA
T <sub>A</sub>	Operating Temperature Range			–40 to +85	°C
T <sub>stg</sub>	Storage Temperature Range			–65 to +150	°C
θ <sub>JA</sub>	Thermal Resistance (Junction–to–Ambient) (Note 4)	0 lfpm 500 lfpm	QFN32 QFN32	31 27	°C/W
θ <sub>JC</sub>	Thermal Resistance (Junction–to–Case) (Note 4)		QFN32	12	°C/W
T <sub>sol</sub>	Wave Solder			265	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

4. JEDEC standard multilayer board – 2S2P (2 signal, 2 power) with 8 filled thermal vias under exposed pad.

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**Table 5. DC CHARACTERISTICS POSITIVE LVPECL OUTPUT**  $V_{CC} = 2.375\text{ V to }3.6\text{ V}$ ;  $GND = 0\text{ V}$ ;  $T_A = -40^\circ\text{C to }85^\circ\text{C}$   
(Note 5)

Symbol	Characteristic	Min	Typ	Max	Unit
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## POWER SUPPLY

$V_{CC}$	Power Supply Voltage	$V_{CC} = 3.3\text{ V}$ $V_{CC} = 2.5\text{ V}$	3.0 2.375	3.3 2.5	3.6 2.625	V
$I_{CC}$	Power Supply Current (Inputs and Outputs Open)			185	225	mA

## LVPECL Outputs

$V_{OH}$	Output HIGH Voltage (Note 6)	$V_{CC} = 3.3\text{ V}$ $V_{CC} = 2.5\text{ V}$	$V_{CC} - 1145$ 2155 1355		$V_{CC} - 800$ 2500 1700	mV
$V_{OL}$	Output LOW Voltage (Note 6)	$V_{CC} = 3.3\text{ V}$ $V_{CC} = 2.5\text{ V}$	$V_{CC} - 2000$ 1300 500		$V_{CC} - 1500$ 1800 1000	mV

## DIFFERENTIAL CLOCK INPUTS DRIVEN SINGLE-ENDED (Note 7) (Figures 5 & 6)

$V_{IH}$	Single-ended Input HIGH Voltage		$V_{th} + 100$		$V_{CC}$	mV
$V_{IL}$	Single-ended Input LOW Voltage		GND		$V_{th} - 100$	mV
$V_{th}$	Input Threshold Reference Voltage Range (Note 8)		1100		$V_{CC} - 100$	mV
$V_{ISE}$	Single-ended Input Voltage ( $V_{IH} - V_{IL}$ )		200		1200	mV

## VREFACx (for Capacitor- Coupled Inputs, Only)

$V_{REFAC}$	Output Reference Voltage @100 $\mu\text{A}$ for Capacitor- Coupled Inputs, Only		$V_{CC} - 1500$	$V_{CC} - 1200$	$V_{CC} - 1000$	mV
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## DIFFERENTIAL INPUTS DRIVEN DIFFERENTIALLY (Figures 7 & 8) (Note 9)

$V_{IHD}$	Differential Input HIGH Voltage ( $I_N, \bar{I}_N$ )		1200		$V_{CC}$	mV
$V_{ILD}$	Differential Input LOW Voltage ( $I_N, \bar{I}_N$ )		GND		$V_{IHD} - 100$	mV
$V_{ID}$	Differential Input Voltage ( $I_N, \bar{I}_N$ ) ( $V_{IHD} - V_{ILD}$ )		100		1200	mV
$V_{CMR}$	Input Common Mode Range (Differential Configuration, Note 10) (Figure 9)		1050		$V_{CC} - 50$	mV
$I_{IH}$	Input HIGH Current $I_N/\bar{I}_N$ ( $V_{TIN}/\bar{V}_{TIN}$ Open)		-150		150	$\mu\text{A}$
$I_{IL}$	Input LOW Current $I_N/\bar{I}_N$ ( $V_{TIN}/\bar{V}_{TIN}$ Open)		-150		150	$\mu\text{A}$

## CONTROL INPUT (SEL Pin)

$V_{IH}$	Input HIGH Voltage for Control Pin		2.0		$V_{CC}$	mV
$V_{IL}$	Input LOW Voltage for Control Pin		GND		0.8	mV
$I_{IH}$	Input HIGH Current		-150		150	$\mu\text{A}$
$I_{IL}$	Input LOW Current		-150		150	$\mu\text{A}$

## TERMINATION RESISTORS

$R_{TIN}$	Internal Input Termination Resistor (Measured from $I_N$ to $V_{Tx}$ )		45	50	55	$\Omega$
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NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm.

- Input and output parameters vary 1:1 with  $V_{CC}$ .
- LVPECL outputs ( $Q_n/\bar{Q}_n$ ) loaded with  $50\ \Omega$  to  $V_{CC} - 2\text{ V}$  for proper operation.
- $V_{th}$ ,  $V_{IH}$ ,  $V_{IL}$ , and  $V_{ISE}$  parameters must be complied with simultaneously.
- $V_{th}$  is applied to the complementary input when operating in single-ended mode.
- $V_{IHD}$ ,  $V_{ILD}$ ,  $V_{ID}$  and  $V_{CMR}$  parameters must be complied with simultaneously.
- $V_{CMR}$  min varies 1:1 with GND,  $V_{CMR}$  max varies 1:1 with  $V_{CC}$ . The  $V_{CMR}$  range is referenced to the most positive side of the differential input signal.

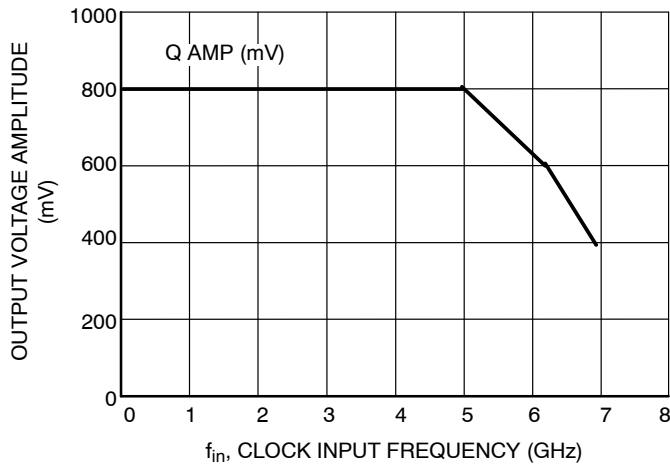
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**Table 6. AC CHARACTERISTICS**  $V_{CC} = 2.375\text{ V to }3.6\text{ V}$ ;  $GND = 0\text{ V}$ ;  $T_A = -40^\circ\text{C to }85^\circ\text{C}$  (Note 11)

Symbol	Characteristic	Min	Typ	Max	Unit	
$f_{MAX}$	Maximum Input Clock Frequency; $V_{OUTpp} \geq 400\text{ mV}$	5	7		GHz	
$f_{DATAMAX}$	Maximum Operating Data Rate (PRBS23)	8	10		Gbps	
$f_{SEL}$	Maximum Toggle Frequency, SEL	1.0	1.5		GHz	
$V_{OUTpp}$	Output Voltage Amplitude (@ $V_{INPPmin}$ ) (Note 12) (Figures 8 and 10)	$f_{in} \leq 4\text{ GHz}$ 400	800 650		mV	
$t_{PLH}$ , $t_{PHL}$	Propagation Delay to Differential Outputs, @ 1 GHz, measured at differential crosspoint	IN/ $\bar{I}$ N to Q/ $\bar{Q}$ SEL to Q	125 75	175 200	250 300	ps
$t_{PLH\ TC}$	Propagation Delay Temperature Coefficient		50		$\Delta\text{fs}/^\circ\text{C}$	
tskew	Output – Output skew (within device) (Note 13) Device – Device skew (tpd max – tpdmin)			20 100	ps	
$t_{DC}$	Output Clock Duty Cycle (Reference Duty Cycle = 50%)	$f_{in} \leq 5.0\text{ GHz}$	45	50	55	%
$\Phi_N$	Phase Noise, $f_{in} = 1\text{ GHz}$	10 kHz 100 kHz 1 MHz 10 MHz 20 MHz 40 MHz		-135 -137 -149 -150 -150 -151		dBc
$t_{f\Phi N}$	Integrated Phase Jitter (Figure x) $f_{in} = 1\text{ GHz}$ , 12 kHz – 20 MHz Offset (RMS)		36			fs
$t_{JITTER}$	RJ – Output Random Jitter (Note 14) DJ – Residual Output Deterministic Jitter (Note 15)	$f_{in} \leq 5.0\text{ GHz}$ $\leq 8\text{ Gbps}$		0.2 5	0.8 15	ps rms ps pk-pk
	Crosstalk Induced Jitter (Adjacent Channel) (Note 17)			0.7		psRMS
$V_{INPP}$	Input Voltage Swing (Differential Configuration) (Note 16)		100		1200	mV
$t_r$ , $t_f$	Output Rise/Fall Times @ 1 GHz (20% – 80%), Q, $\bar{Q}$		25	55	85	ps

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm.

11. Measured using a 400 mV pk-pk source, 50% duty cycle clock source. All output loading with external  $50\ \Omega$  to  $V_{CC} - 2\text{ V}$ . Input edge rates 40 ps (20% – 80%).
12. Output voltage swing is a single-ended measurement operating in differential mode.
13. Skew is measured between outputs under identical transitions and conditions. Duty cycle skew is defined only for differential operation when the delays are measured from cross-point of the inputs to the crosspoint of the outputs.
14. Additive RMS jitter with 50% duty cycle clock signal.
15. Additive Peak-to-Peak data dependent jitter with input NRZ data at PRBS23.
16. Input voltage swing is a single-ended measurement operating in differential mode.
17. Crosstalk is measured at the output while applying two similar clock frequencies that are asynchronous with respect to each other at the inputs.



**Figure 3. Clock Output Voltage Amplitude ( $V_{OUTpp}$ ) vs. Input Frequency ( $f_{in}$ ) at Ambient Temperature (Typical)**

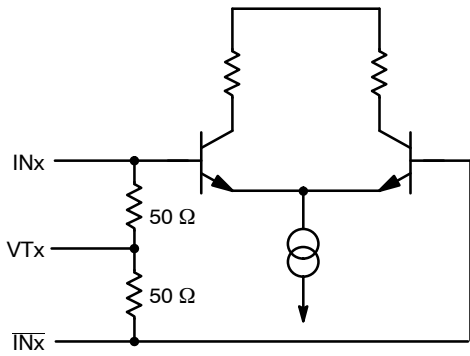


Figure 4. Input Structure

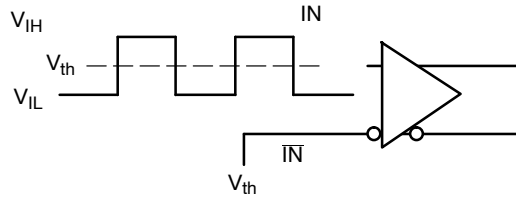


Figure 5. Differential Input Driven Single-Ended

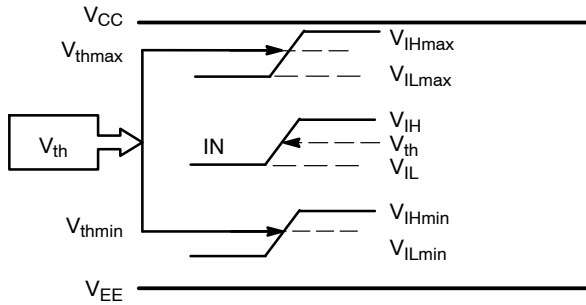


Figure 6.  $V_{th}$  Diagram

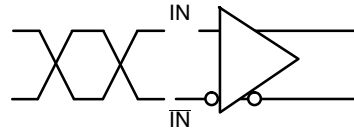


Figure 7. Differential Inputs Driven Differentially

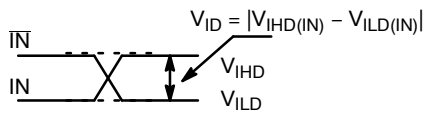


Figure 8. Differential Inputs Driven Differentially

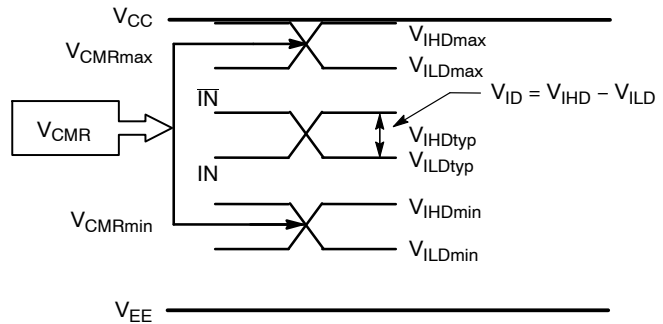


Figure 9. VCMR Diagram

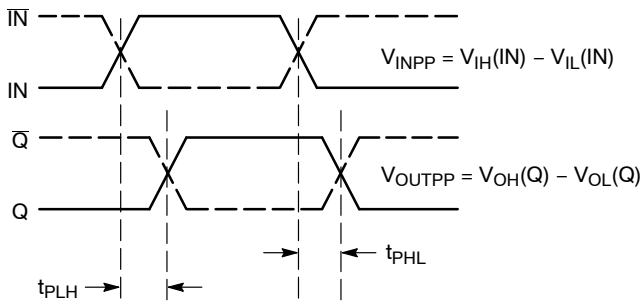


Figure 10. AC Reference Measurement

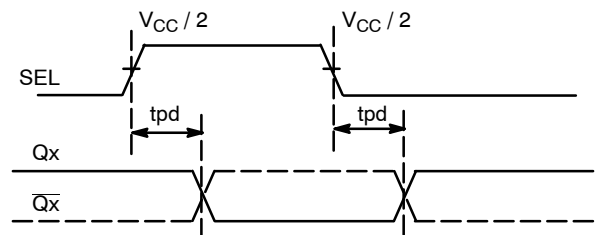


Figure 11. SEL to Qx Timing Diagram

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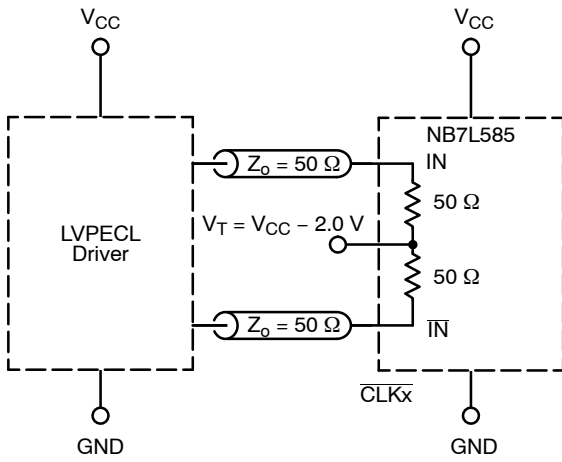


Figure 12. LVPECL Interface

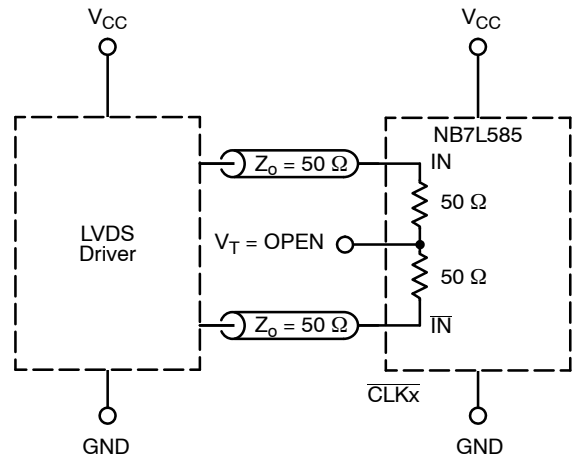


Figure 13. LVDS Interface

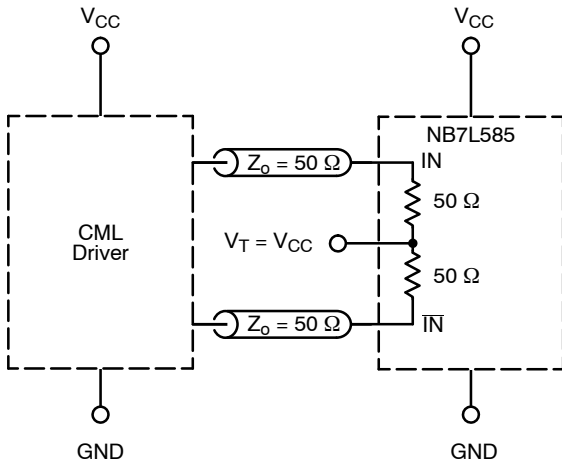


Figure 14. Standard 50 Ω Load CML Interface

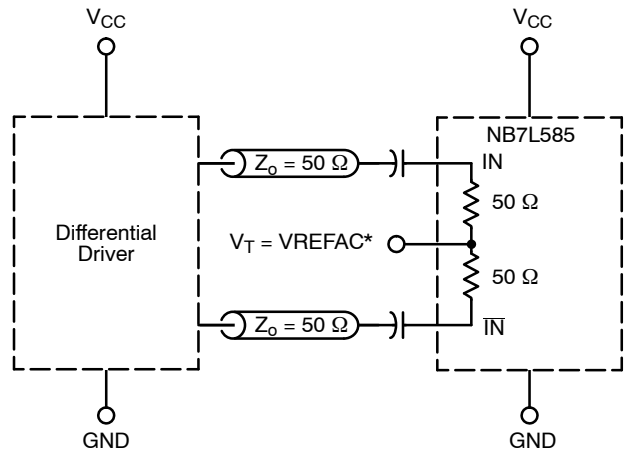


Figure 15. Capacitor-Coupled Differential Interface ( $V_T$  Connected to  $V_{REFAC}$ )

\* $V_{REFAC}$  bypassed to ground with a 0.01  $\mu\text{F}$  capacitor.

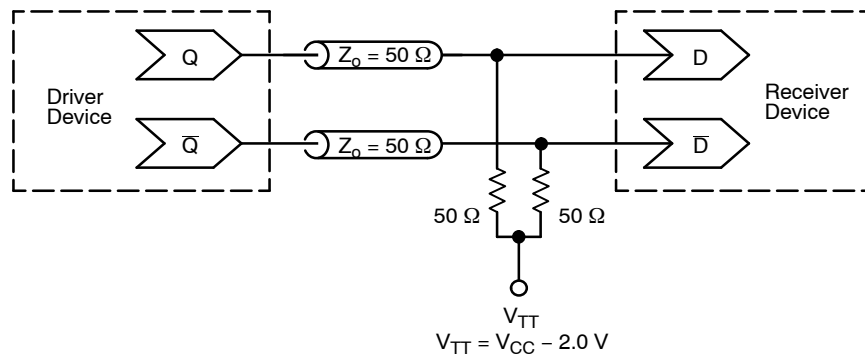


Figure 16. Typical Termination for Output Driver and Device Evaluation (See Application Note AND8020/D – Termination of ECL Logic Devices.)

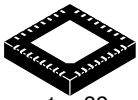
# NB7L585

## DEVICE ORDERING INFORMATION

Device	Package	Shipping <sup>†</sup>
NB7L585MNG	QFN-32 (Pb-Free)	74 Units / Tube
NB7L585MNR4G	QFN-32 (Pb-Free)	1000 / Tape & Reel
NB7L585MNTWG	QFN-32 (Pb-Free)	1000 / Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

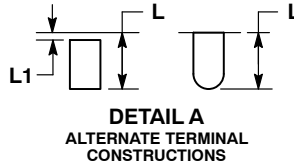
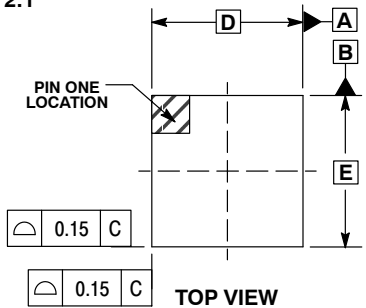




1 32  
SCALE 2:1

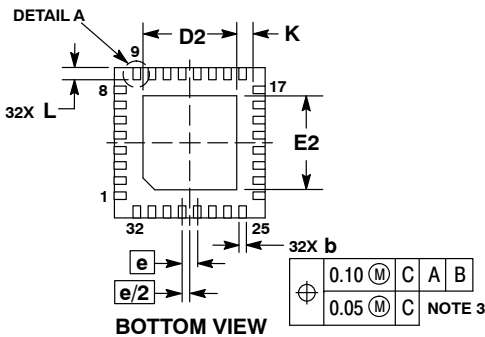
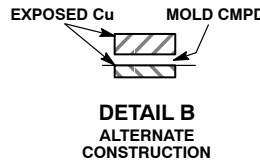
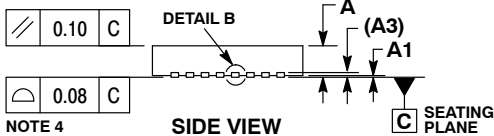
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CASE 488AM  
ISSUE A

DATE 23 OCT 2013

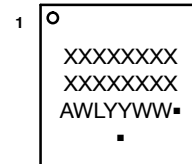


- NOTES:
1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
  2. CONTROLLING DIMENSION: MILLIMETERS.
  3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30MM FROM THE TERMINAL TIP.
  4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

MILLIMETERS		
DIM	MIN	MAX
A	0.80	1.00
A1	---	0.05
A3	0.20	REF
b	0.18	0.30
D	5.00	BSC
D2	2.95	3.25
E	5.00	BSC
E2	2.95	3.25
e	0.50	BSC
K	0.20	---
L	0.30	0.50
L1	---	0.15



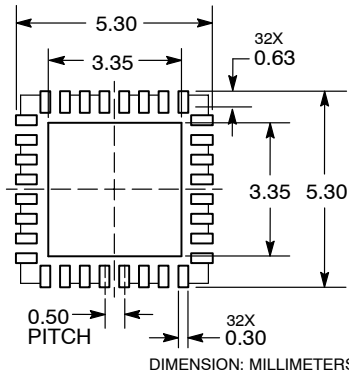
GENERIC MARKING DIAGRAM\*



- XXXXX = Specific Device Code
- A = Assembly Location
- WL = Wafer Lot
- YY = Year
- WW = Work Week
- = Pb-Free Package

(Note: Microdot may be in either location)  
\*This information is generic. Please refer to device data sheet for actual part marking.  
Pb-Free indicator, "G" or microdot "▪", may or may not be present.

RECOMMENDED SOLDERING FOOTPRINT\*



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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DESCRIPTION:	QFN32 5x5 0.5P	PAGE 1 OF 1

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