

2.5 V/3.3 V 1:8 LVPECL Fanout Buffer

Multi-Level Inputs w/ Internal Termination

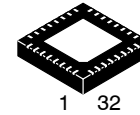
NB7L1008

Description

The NB7L1008 is a high performance differential 1:8 Clock/Data fanout buffer. The NB7L1008 produces eight identical output copies of Clock or Data operating up to 7 GHz or 12 Gb/s, respectively. As such, the NB7L1008 is ideal for SONET, GigE, Fiber Channel, Backplane and other Clock/Data distribution applications. The differential inputs incorporate internal 50 Ω termination resistors that are accessed through the VT pin. This feature allows the NB7L1008 to accept various logic standards, such as LVPECL, CML, LVDS logic levels. The V_{REFAC} reference output can be used to rebias capacitor-coupled differential or single-ended input signals. The 1:8 fanout design was optimized for low output skew applications. The NB7L1008 is a member of the GigaComm™ family of high performance clock products.

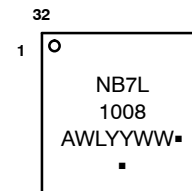
Features

- Typical Maximum Input Data Rate > 12 Gb/s Typical
- Data Dependent Jitter < 15 ps
- Maximum Input Clock Frequency > 7 GHz Typical
- Random Clock Jitter < 0.8 ps RMS
- Low Skew 1:8 LVPECL Outputs, < 20 ps max
- Multi-Level Inputs, accepts LVPECL, CML, LVDS
- 160 ps Typical Propagation Delay
- 50 ps Typical Rise and Fall Times
- Differential LVPECL Outputs, 750 mV Peak-to-Peak, Typical
- Operating Range: V_{CC} = 2.375 V to 3.6 V, GND = 0 V
- Internal Input Termination Resistors, 50 Ω
- V_{REFAC} Reference Output
- QFN-32 Package, 5 mm x 5 mm
- -40°C to +85°C Ambient Operating Temperature
- These are Pb-Free and Halide-Free Devices



QFN32
MN SUFFIX
CASE 488AM

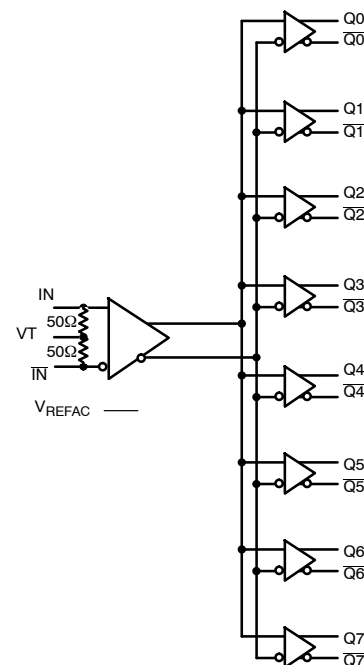
MARKING DIAGRAM



- A = Assembly Location
- WL = Wafer Lot
- YY = Year
- WW = Work Week
- = Pb-Free Package

(Note: Microdot may be in either location)

SIMPLIFIED LOGIC DIAGRAM



ORDERING INFORMATION

See detailed ordering and shipping information on page 9 of this data sheet.

NB7L1008

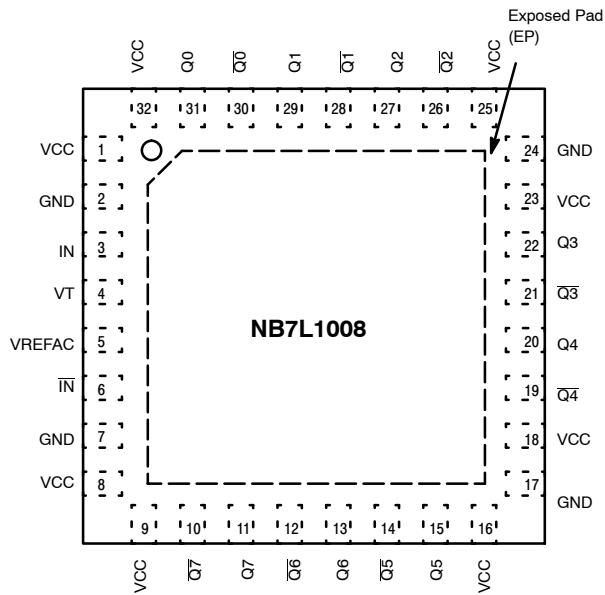


Figure 1. 32-Lead QFN Pinout (Top View)

Table 1. PIN DESCRIPTION

Pin	Name	I/O	Description
3, 6	IN, $\overline{\text{IN}}$	LVPECL, CML, LVDS Input	Non-inverted / Inverted Differential Clock/Data Input. Note 1
4	VT		Internal 50 Ω Termination Pin for IN and $\overline{\text{IN}}$
2, 7 17,24	GND		Negative Supply Voltage, Note 2
1, 8, 9, 16, 18, 23, 25, 32	V _{CC}		Positive Supply Voltage, Note 2
31, 30, 29, 28, 27, 26, 22, 21, 20, 19, 15, 14, 13, 12, 11, 10	Q0, $\overline{\text{Q0}}$, Q1, $\overline{\text{Q1}}$, Q2, $\overline{\text{Q2}}$, Q3, $\overline{\text{Q3}}$, Q4, $\overline{\text{Q4}}$, Q5, $\overline{\text{Q5}}$, Q6, $\overline{\text{Q6}}$, Q7, $\overline{\text{Q7}}$	LVPECL	Non-inverted / Inverted Differential Output.
5	VREFAC		Output Voltage Reference for Capacitor-Coupled Inputs, only
-	EP	-	The Exposed Pad (EP) on the QFN-32 package bottom is thermally connected to the die for improved heat transfer out of package. The exposed pad must be attached to a heat-sinking conduit. The pad is electrically connected to GND and is recommended to be electrically connected to GND on the PC board.

1. In the differential configuration when the input termination pin (V_T) is connected to a common termination voltage or left open, and if no signal is applied on IN/ $\overline{\text{IN}}$, then the device will be susceptible to self-oscillation.
2. All V_{CC} and GND pins must be externally connected to the same power supply voltage to guarantee proper device operation.

NB7L1008

Table 2. ATTRIBUTES

Characteristics		Value
ESD Protection	Human Body Model	> 2 kV
	Machine Model	> 200 V
Moisture Sensitivity (Note 3) Indefinite Time of the Drypack QFN-32		Level 1
Flammability Rating	Oxygen Index: 28 to 34	UL 94 V-0 @ 0.125 in
Transistor Count		263
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test		

3. For additional information, refer to Application Note AND8003/D.

Table 3. MAXIMUM RATINGS

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
V_{CC}	Positive Power Supply	GND = 0 V		4.0	V
V_{IN}	Input Voltage	GND = 0 V		-0.5 to V_{CC}	V
V_{INPP}	Differential Input Voltage $ I_N - \bar{I}_N $			1.89	V
I_{IN}	Input Current Through R_T (50 Ω Resistor)			± 40	mA
I_{out}	Output Current	Continuous Surge		34 40	mA
$I_{VFREFAC}$	V_{REFAC} Sink/Source Current			± 1.5	mA
T_A	Operating Temperature Range			-40 to +85	$^{\circ}\text{C}$
T_{stg}	Storage Temperature Range			-65 to +150	$^{\circ}\text{C}$
θ_{JA}	Thermal Resistance (Junction-to-Ambient) (Note 4) TGSD 51-6 (2S2P Multilayer Test Board) with Filled Thermal Vias	500 lfp/m	QFN-32	27	$^{\circ}\text{C}/\text{W}$
θ_{JC}	Thermal Resistance (Junction-to-Case)	Standard Board	QFN-32	12	$^{\circ}\text{C}/\text{W}$
T_{sol}	Wave Solder Pb-Free			265	$^{\circ}\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

4. JEDEC standard multilayer board – 2S2P (2 signal, 2 power) with 8 filled thermal vias under exposed pad.

NB7L1008

Table 4. DC CHARACTERISTICS – LVPECL OUTPUT $V_{CC} = 2.375\text{ V to }3.6\text{ V}$; $GND = 0\text{ V}$ $T_A = -40^\circ\text{C to }85^\circ\text{C}$ (Note 6)

Symbol	Characteristic	Min	Typ	Max	Unit
POWER SUPPLY CURRENT					
I_{CC}	Power Supply Current, Inputs and Outputs Open		165	215	mA
LVPECL OUTPUTS (Note 5, Figure 11)					
V_{OH}	Output HIGH Voltage $V_{CC} = 3.3\text{ V}$ $V_{CC} = 2.5\text{ V}$	$V_{CC} - 1025$ 2275 1475		$V_{CC} - 775$ 2525 1725	mV
V_{OL}	Output LOW Voltage $V_{CC} = 3.3\text{ V}$ $V_{CC} = 2.5\text{ V}$	$V_{CC} - 2000$ 1300 500		$V_{CC} - 1500$ 1800 1000	mV
DIFFERENTIAL INPUTS DRIVEN SINGLE-ENDED (Notes 7 and 8) (Figures 7 and 9)					
V_{IH}	Single-Ended Input HIGH Voltage	$V_{th} + 100$		V_{CC}	mV
V_{IL}	Single-Ended Input LOW Voltage	GND		$V_{th} - 100$	mV
V_{th}	Input Threshold Reference Voltage Range	1100		$V_{CC} - 100$	mV
V_{ISE}	Single-Ended Input Voltage ($V_{IH} - V_{IL}$)	200		1200	mV
V_{REFAC}					
V_{REFAC}	Output Reference Voltage @ 100 μA for Capacitor – Coupled Inputs, Only $V_{CC} = 3.3\text{ V}$ $V_{CC} = 2.5\text{ V}$	$V_{CC} - 1150$ $V_{CC} - 1150$	$V_{CC} - 1050$ $V_{CC} - 1050$	$V_{CC} - 950$ $V_{CC} - 950$	mV
DIFFERENTIAL INPUTS DRIVEN DIFFERENTIALLY (IN, $\bar{\text{IN}}$) (Note 9) (Figures 5 and 8)					
V_{IHD}	Differential Input HIGH Voltage	1100		V_{CC}	mV
V_{ILD}	Differential Input LOW Voltage	GND		$V_{IHD} - 100$	mV
V_{ID}	Differential Input Voltage ($V_{IHD} - V_{ILD}$)	100		1200	mV
I_{IH}	Input HIGH Current	-150	40	+150	μA
I_{IL}	Input LOW Current	-150	0	+150	μA
TERMINATION RESISTORS					
R_{TIN}	Internal Input Termination Resistor	45	50	55	Ω

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm.

- LVPECL outputs loaded with 50 Ω to $V_{CC} - 2\text{ V}$ for proper operation.
- Input and output parameters vary 1:1 with V_{CC} .
- V_{th} , V_{IH} , V_{IL} , and V_{ISE} parameters must be complied with simultaneously.
- V_{th} is applied to the complementary input when operating in single-ended mode.
- V_{IHD} , V_{ILD} , V_{ID} and V_{CMR} parameters must be complied with simultaneously.

NB7L1008

Table 5. AC CHARACTERISTICS $V_{CC} = 2.375\text{ V to }3.6\text{ V}$; $GND = 0\text{ V}$ $TA = -40^{\circ}\text{C to }85^{\circ}\text{C}$ (Note 10)

Symbol	Characteristic	Min	Typ	Max	Unit
f_{DATA}	Maximum Operating Input Data Rate (Note 17)	10	12		Gb/s
f_{INCLK}	Maximum Input Clock Frequency, $V_{\text{OUTPP}} \geq 400\text{ mV}$ (Note 17)	5	7		GHz
V_{OUTPP}	Output Voltage Amplitude (see Figures 2 and 6, Notes 11, 17) $f_{\text{in}} \leq 5\text{ GHz}$	400			mV
V_{CMR}	Input Common Mode Range (Differential Configuration, Note 12, Figure 10)	600		$V_{\text{CC}} - 50$	mV
$t_{\text{PLH}}, t_{\text{PHL}}$	Propagation Delay to Output Differential, $\text{IN}/\overline{\text{IN}}$ to $\text{Qn}/\overline{\text{Qn}}$	100	160	220	ps
$t_{\text{PLH TC}}$	Propagation Delay Temperature Coefficient $-40^{\circ}\text{C to }+85^{\circ}\text{C}$		25		fs/ $^{\circ}\text{C}$
t_{DC}	Output Clock Duty Cycle $f_{\text{in}} \leq 5\text{ GHz}$	45	49/51	55	%
t_{SKEW}	Within Device Skew (Note 13) Device to Device Skew (Note 14)			20 100	ps
T_{jitter}	Clock Jitter RMS, 1000 Cycles (Note 17) $f_{\text{in}} \leq 6\text{ GHz}$ Data Dependent Jitter (DDJ) (Note 17) $\leq 10\text{ Gb/s}$		0.2 3	0.8 15	ps
T_{jitter} (additive)	622 MHz @ Integration Range of 12 kHz to 20 MHz		0.025		ps
V_{INPP}	Input Voltage Swing (Differential Configuration) (Note 16) (Figure 6)	100		1200	mV
$t_{\text{r}}, t_{\text{f}}$	Output Rise/Fall Times (20% – 80%) $\text{Qn}, \overline{\text{Qn}}$	20	50	80	ps

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm.

10. All outputs must be loaded with external $50\ \Omega$ to $V_{\text{CC}} - 2\text{ V}$.
11. Output voltage swing is a single-ended measurement operating in differential mode.
12. $V_{\text{IHDMIN}} \geq 1100\text{ mV}$.
13. Within device skew compares coincident edges.
14. Device to device skew is measured between outputs under identical transition
15. Additive CLOCK jitter with 50% duty cycle clock signal input.
16. Input voltage swing is a single-ended measurement operating in differential mode.
17. V_{CC} of 2.5–3.3, input = $800\text{ mV}_{\text{p-p}}$

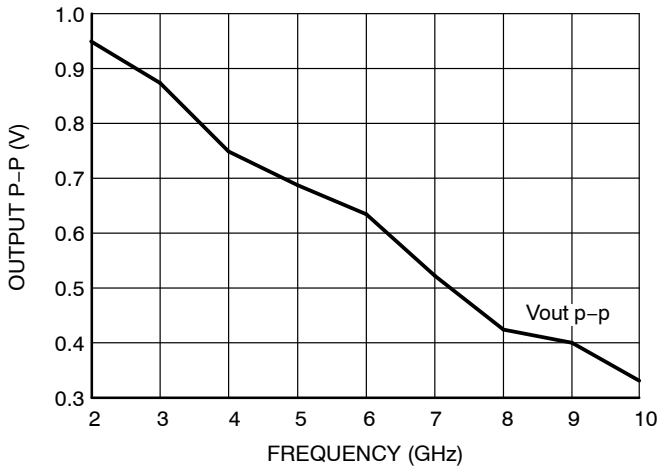


Figure 2. Typical $V_{\text{OUT P-P}}$ vs. Frequency at 25°C

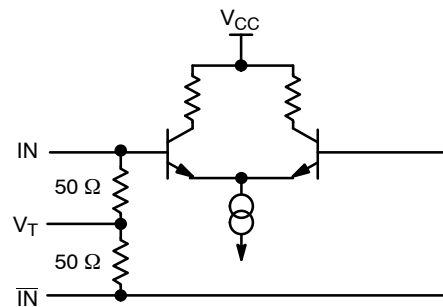


Figure 3. Input Structure

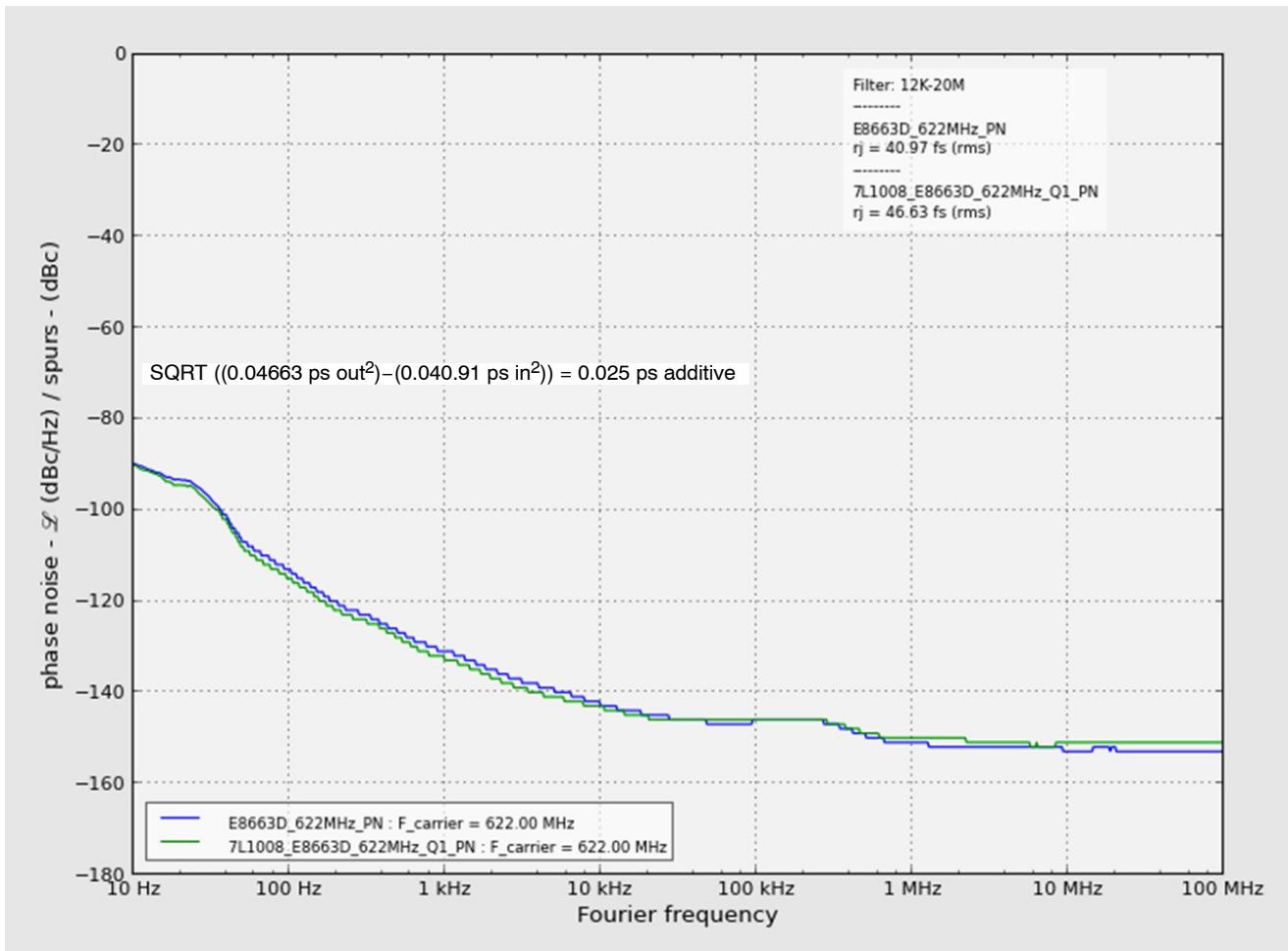


Figure 4. Additive Phase Jitter RMS from 12 kHz to 20 MHz @ 622 MHz, Typical 0.025 ps

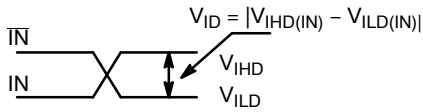


Figure 5. Differential Inputs Driven Differentially

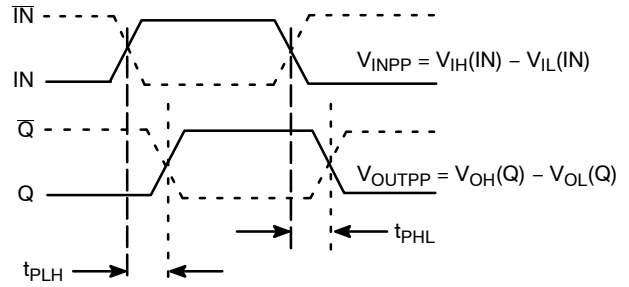


Figure 6. AC Reference Measurement

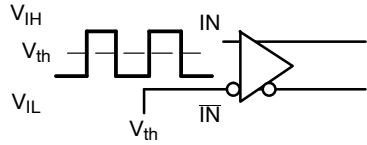


Figure 7. Differential Input Driven Single-Ended

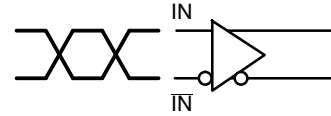


Figure 8. Differential Inputs Driven Differentially

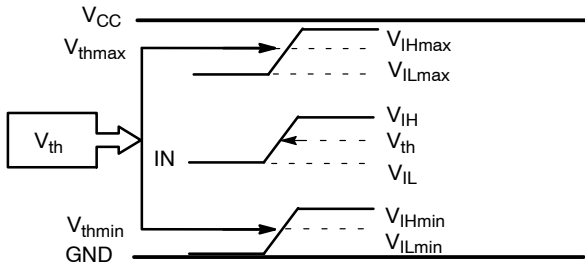


Figure 9. V_{th} Diagram

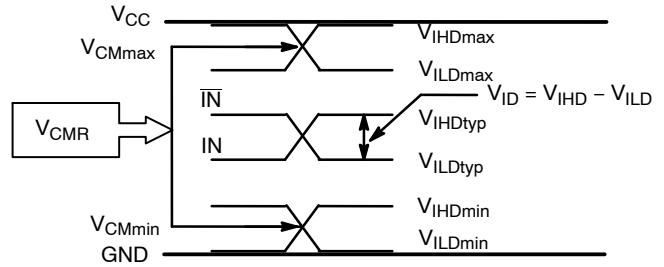


Figure 10. V_{CM} Diagram

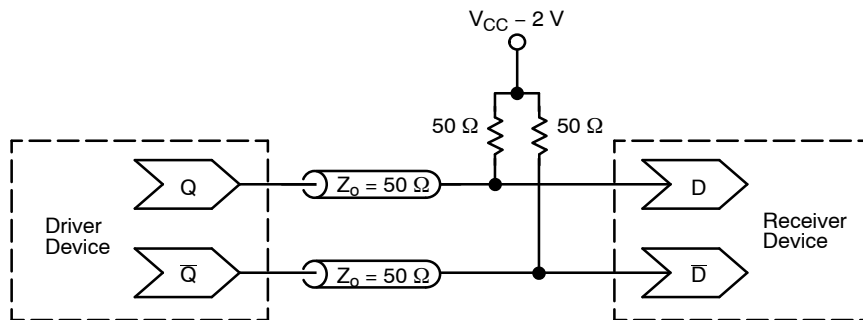


Figure 11. Typical Termination for Output Driver and Device Evaluation
(See Application Note AND8173/D)

NB7L1008

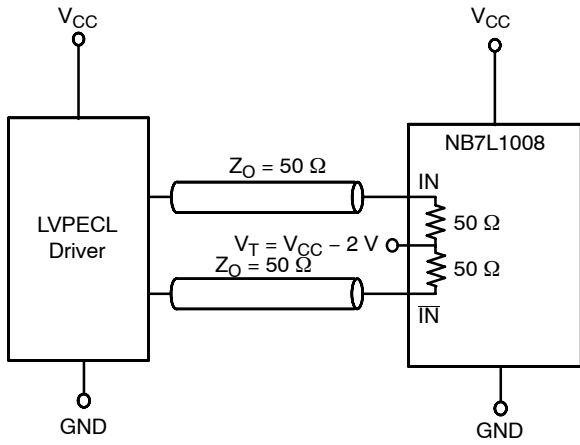


Figure 12. LVPECL Interface

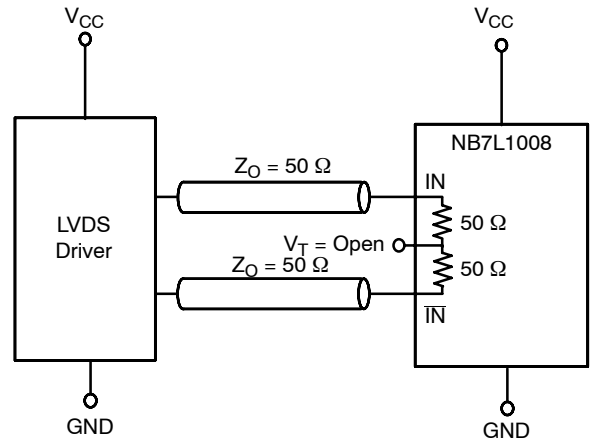


Figure 13. LVDS Interface

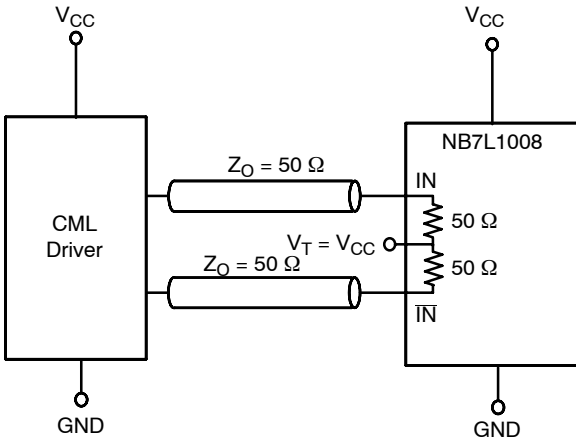


Figure 14. Standard 50 Ω Load CML Interface

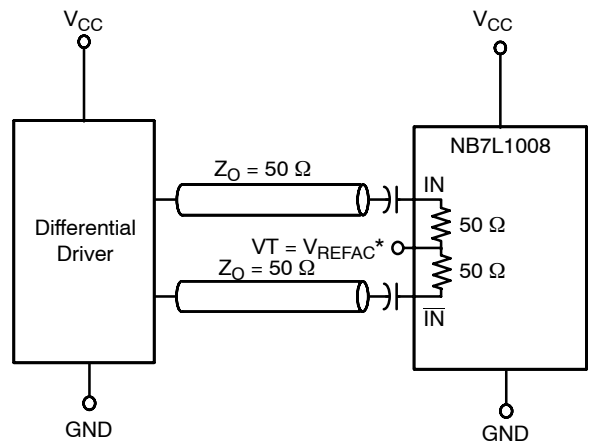


Figure 15. Capacitor-Coupled Differential Interface (V_T Connected to V_{REFAC})

* V_{REFAC} bypassed to ground with a 0.01 μF capacitor

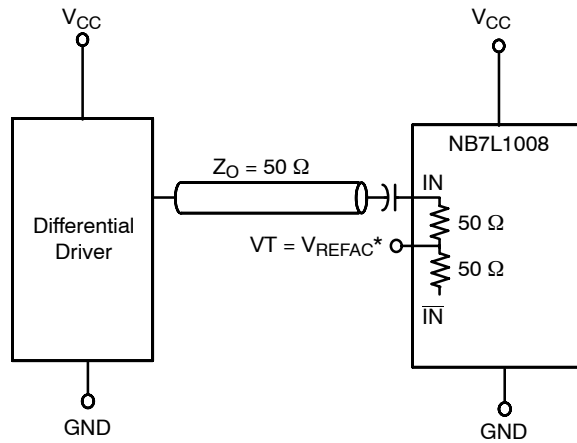


Figure 16. Capacitor-Coupled Single-Ended Interface (V_T Connected to V_{REFAC})

NB7L1008

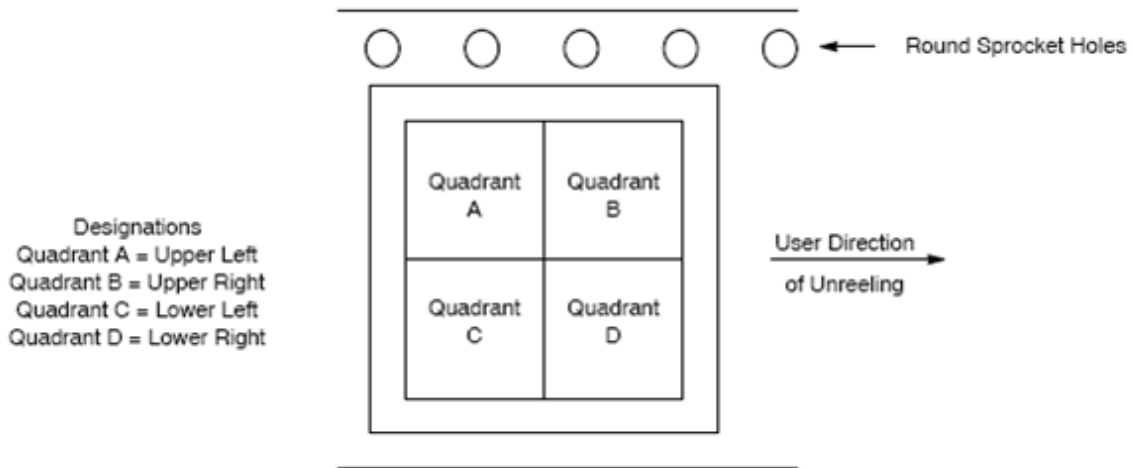
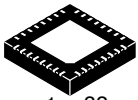


Figure 17. Tape and Reel Pin 1 Quadrant Orientation

ORDERING INFORMATION

Device	Package	Shipping [†]
NB7L1008MNG	QFN32 (Pb-Free, Halide-Free)	74 Units / Rail
NB7L1008MNTXG	QFN32 (Pb-Free, Halide-Free)	1,000 / Tape & Reel (Pin 1 Orientation in Quadrant B, Figure 17)

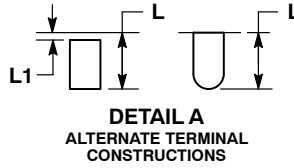
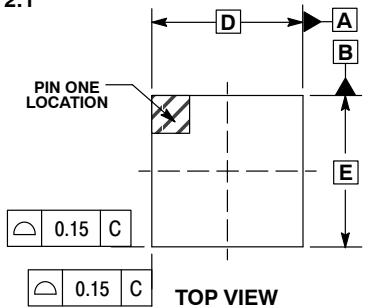
[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).



1 32
SCALE 2:1

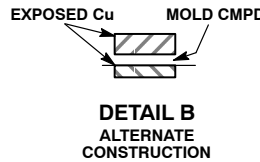
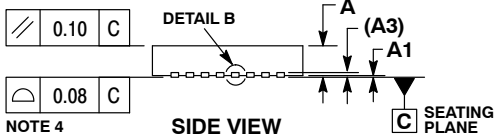
QFN32 5x5, 0.5P
CASE 488AM
ISSUE A

DATE 23 OCT 2013

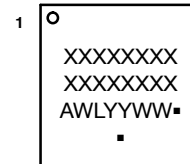
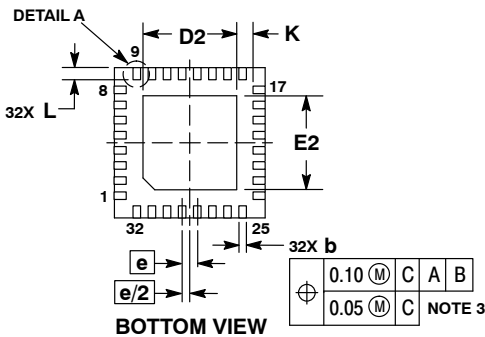


- NOTES:
1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
 2. CONTROLLING DIMENSION: MILLIMETERS.
 3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30MM FROM THE TERMINAL TIP.
 4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

MILLIMETERS		
DIM	MIN	MAX
A	0.80	1.00
A1	---	0.05
A3	0.20	REF
b	0.18	0.30
D	5.00	BSC
D2	2.95	3.25
E	5.00	BSC
E2	2.95	3.25
e	0.50	BSC
K	0.20	---
L	0.30	0.50
L1	---	0.15



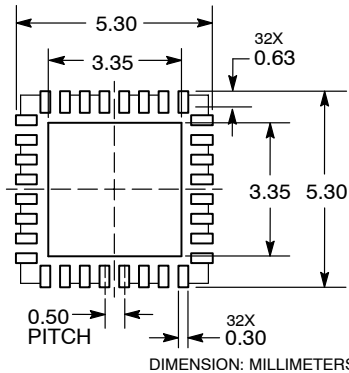
GENERIC
MARKING DIAGRAM*



- XXXXX = Specific Device Code
- A = Assembly Location
- WL = Wafer Lot
- YY = Year
- WW = Work Week
- = Pb-Free Package

(Note: Microdot may be in either location)
*This information is generic. Please refer to device data sheet for actual part marking.
Pb-Free indicator, "G" or microdot "▪", may or may not be present.

RECOMMENDED
SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

DOCUMENT NUMBER:	98AON20032D	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	QFN32 5x5 0.5P	PAGE 1 OF 1

onsemi and Onsemi are trademarks of Semiconductor Components Industries, LLC dba onsemi or its subsidiaries in the United States and/or other countries. onsemi reserves the right to make changes without further notice to any products herein. onsemi makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does onsemi assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. onsemi does not convey any license under its patent rights nor the rights of others.

onsemi, **Onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:

Technical Library: www.onsemi.com/design/resources/technical-documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support

For additional information, please contact your local Sales Representative at www.onsemi.com/support/sales