LMH2180 75 MHz Dual Clock Buffer

Check for Samples: LMH2180

FEATURES

- **(Typical Values are: V_{SUPPLY} = 2.7V and C_L = 10 pF, unless Otherwise Specified.)**
- **Small Signal Bandwidth 78 MHz**
- **Supply Voltage Range 2.4V to 5V**
- **Phase Noise (V_{IN} = 1 V_{PP}, f_C = 38.4 MHz, Δf = 1 kHz) −123 dBc/Hz**
- **Slew Rate 106 V/µs**
- **Total Supply Current 2.3 mA**
- **Shutdown Current 30 µA**
- **Rail-to-Rail Input and Output**
- **Individual Buffer Enable Pins**
- **Rapid T_{on} Technology**
- **Crosstalk Rejection Circuitry**
- **Packages:**
  - **8-Pin WSON, Solder Bump and no Pullback**
  - **8-Bump DSBGA**
- **Temperature Range −40°C to 85°C**

APPLICATIONS

- **3G Mobile Applications**
- **WLAN–WiMAX Modules**
- **TD_SCDMA Multi-Mode MP3 and Camera**
- **GSM Modules**
- **Oscillator Modules**

DESCRIPTION

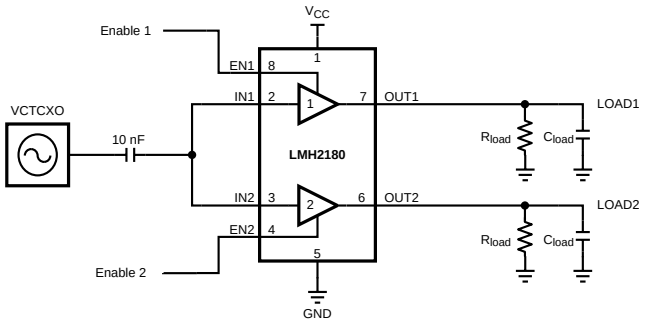
The LMH2180 is a high speed dual clock buffer designed for portable communications and applications requiring multiple accurate multi-clock systems. The LMH2180 integrates two 75 MHz low noise buffers with independent shutdown pins into a small package. The LMH2180 ensures superb system operation between the baseband and the oscillator signal path by eliminating crosstalk between the multiple clock signals.

Unique technology and design provides the LMH2180 with the ability to accurately drive both large capacitive and resistive loads. Low supply current combined with shutdown pins for each channel means the LMH2180 is ideal for battery powered applications. This part does not use an internal ground reference, thus providing additional system flexibility.

The flexible buffers provide system designers the capacity to manage complex clock signals in the latest wireless applications. Each buffer delivers 106 V/µs internal slew rate with independent shutdown and duty cycle precision. Each input is internally biased to 1V, removing the need for external resistors. Both channels have rail-to-rail inputs and outputs, a gain of one, and are AC coupled with the use of one capacitor.

Replacing a discrete buffer solution with the LMH2180 provides many benefits: simplified board layout, minimized parasitic components, simplified BOM, design durability across multiple applications, simplification of clock paths, and the ability to reduce the number of clock signal generators in the system. The LMH2180 is produced in the tiny packages minimizing the required PCB space.

TYPICAL APPLICATION



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CONNECTION DIAGRAMS

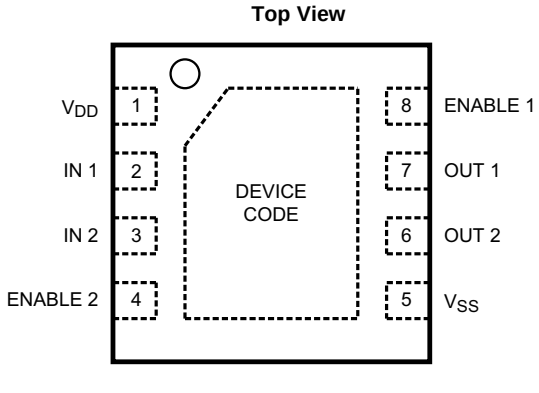


Figure 1. 8-Pin WSON Package
See Package Number NGW0008A or NGQ0008A

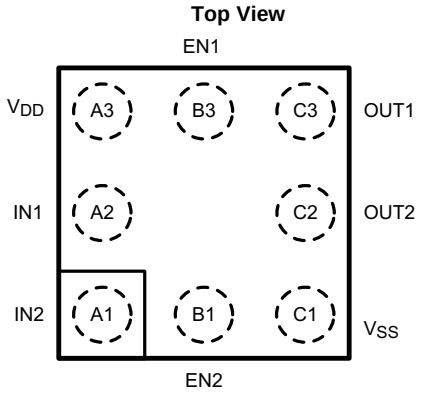


Figure 2. 8-Bump DSBGA Package
See Package Number YFQ0008AAA

PIN DESCRIPTIONS

Pin No. WSON	Pin No. DSBGA	Pin Name	Description
1	A3	V_{DD}	Voltage supply connection
2	A2	IN 1	Input 1
3	A1	IN 2	Input 2
4	B1	ENABLE 2	Enable buffer 2
5	C1	V_{SS}	Ground connection
6	C2	OUT 2	Output 2
7	C3	OUT 1	Output 1
8	B3	ENABLE 1	Enable buffer 1

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS (1)(2)

Supply Voltages ($V^+ – V^-$)	5.5V
ESD Tolerance	
Human Body (3)	2000V
Machine Model (4)	200V
Charged Device Model	1000V
Storage Temperature Range	−65°C to 150°C
Junction Temperature (5)	150°C
Soldering Information	
Infrared or Convection (35 sec.)	235°C

(1) "Absolute Maximum Ratings" indicate limits beyond which damage to the device may occur, including inoperability and degradation of the device reliability and/or performance. Functional operation of the device and/or non-degradation at the Absolute Maximum Ratings or other conditions beyond those indicated in the Recommended Operating Conditions is not implied. The Recommended Operating Conditions indicate conditions at which the device is functional and the device should not be operated beyond such conditions. All voltages are measured with respect to the ground pin, unless otherwise specified.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(3) Human body model, applicable std. JESD22–A114C.
(4) Machine model, applicable std. JESD22–A115–A.
(5) The maximum power dissipation must be derated at elevated temperatures and is dictated by $T_{J(MAX)}$, θ_{JA} , and the ambient temperature T_A. The maximum allowable power dissipation is $P_{DMAX} = (T_{JMAX} - T_A) / \theta_{JA}$ or the number given in the *Absolute Maximum Ratings*, whichever is lower.

OPERATING RATINGS (1)

Supply Voltage ($V^+ - V^-$)	2.4V to 5.0V
Temperature Range (2)(3)	−40°C to 85°C
Package Thermal Resistance (2)(3)	
8-Pin WSON (θ_{JA})	217°C/W
8-Bump DSBGA (θ_{JA})	90°C/W

(1) "Absolute Maximum Ratings" indicate limits beyond which damage to the device may occur, including inoperability and degradation of the device reliability and/or performance. Functional operation of the device and/or non-degradation at the Absolute Maximum Ratings or other conditions beyond those indicated in the Recommended Operating Conditions is not implied. The Recommended Operating Conditions indicate conditions at which the device is functional and the device should not be operated beyond such conditions. All voltages are measured with respect to the ground pin, unless otherwise specified.
(2) The Electrical Characteristics tables show performance under the specified Recommended Operating Conditions except as otherwise modified by the Electrical Characteristics Conditions and/or Notes. Typical values represent typical performance as measured by production tests. Individual parts may vary.
(3) The maximum power dissipation must be derated at elevated temperatures and is dictated by $T_{J(MAX)}$, θ_{JA} , and the ambient temperature T_A. The maximum allowable power dissipation is $P_{DMAX} = (T_{JMAX} - T_A) / \theta_{JA}$ or the number given in the *Absolute Maximum Ratings*, whichever is lower.

2.7V ELECTRICAL CHARACTERISTICS

Unless otherwise specified, all limits are specified for T_A = 25°C, V_{DD} = 2.7V, V_{SS} = 0V, V_{CM} = 1V, $Enable_{1,2} = V_{DD}$, C_L = 10 pF, R_L = 30 kΩ, Load is connected to V_{SS}, $C_{COUPLING}$ = 10 nF. **Boldface** limits apply at temperature range extremes of operating condition.(1)

Parameter		Test Conditions	Min (2)	Typ (3)	Max (2)	Units
Frequency Domain Response						
SSBW	Small Signal Bandwidth	V_{IN} = 100 mV_{PP}; −3 dB		78		MHz
LSBW	Large Signal Bandwidth	V_{IN} = 1.0 V_{PP}; −3 dB		60		MHz
GFN	Gain Flatness < 0.1 dB	f > 100 kHz		4.9		MHz
Distortion and Noise Performance						
φ_n	Phase Noise	V_{IN} = 1 V_{PP}, f_C = 38.4 MHz, Δf = 1 kHz		−123		dBc/Hz
		V_{IN} = 1 V_{PP}, f_C = 38.4 MHz, Δf = 10 kHz		−132		dBc/Hz
e_n	Input-Referred Voltage Noise	f = 1 MHz, R_{SOURCE} = 50Ω		13		$nV/\sqrt{Hz}$
$I_{SOLATION}$	Output to Input	f = 1 MHz, R_{SOURCE} = 50Ω		84		dB
CT	Crosstalk Rejection	f = 38.4 MHz, V_{IN} = 1 V_{PP}		41		dB
Time Domain Response						
t_r	Rise Time	0.1 V_{PP} Step (10-90%)		6		ns
t_f	Fall Time			5		ns
t_s	Settling Time to 0.1%	1 V_{PP} Step		120		ns
OS	Overshoot	0.1 V_{PP} Step		37		%
SR	Slew Rate (4)	V_{IN} = 2 V_{PP}		106		V/µs
Static DC Performance						
I_S	Supply Current	$Enable_{1,2} = V_{DD}$; No Load		2.3	2.7 **2.9**	mA
		$Enable_1 = V_{DD}$, $Enable_2 = V_{SS}$, No Load		1.3	1.5 **1.6**	mA
		$Enable_{1,2} = V_{SS}$; No Load		30	41 **46**	µA
PSRR	Power Supply Rejection Ratio	DC (3.0V to 5.0V)	65 **64**	68		dB

(1) The Electrical Characteristics tables show performance under the specified Recommended Operating Conditions except as otherwise modified by the Electrical Characteristics Conditions and/or Notes. Typical values represent typical performance as measured by production tests. Individual parts may vary.
(2) Datasheet min/max limits are specified by test or statistical analysis.
(3) Typical values represent the most likely parametric norms at T_A = +25°C, and at the Recommended Operation Conditions at the time of product characterization.
(4) Slew rate is the average of the rising and falling slew rates.

2.7V ELECTRICAL CHARACTERISTICS (continued)

Unless otherwise specified, all limits are specified for T_A = 25°C, V_{DD} = 2.7V, V_{SS} = 0V, V_{CM} = 1V, $Enable_{1,2}$ = V_{DD}, C_L = 10 pF, R_L = 30 kΩ, Load is connected to V_{SS}, $C_{COUPLING}$ = 10 nF. **Boldface** limits apply at temperature range extremes of operating condition.(1)

Parameter		Test Conditions	Min (2)	Typ (3)	Max (2)	Units
A_{CL}	Small Signal Voltage Gain	V_{IN} = 0.2 V_{PP}	**0.95**	1.0	**1.05**	V/V
V_{OS}	Output Offset Voltage			-0.5	17 **18**	mV
TC V_{OS}	Temperature Coefficient Output Offset Voltage (5)			2.8		µV/°C
R_{OUT}	Output Resistance	f = 100 kHz		0.6		Ω
		f = 38.4 MHz		166		
		disabled		High Impedance		
Miscellaneous Performance						
R_{IN}	Input Resistance per Buffer	Enable = V_{DD}		137		kΩ
		Enable = V_{SS}		137		
C_{IN}	Input Capacitance per Buffer	Enable = V_{DD}		1.3		pF
		Enable = V_{SS}		1.3		
Z_{IN}	Input Impedance	f = 38.4 MHz, Enable = V_{DD}		4.5		kΩ
		f = 38.4 MHz, Enable = V_{SS}		4.2		
V_O	Output Swing Positive	V_{IN} = V_{DD}	2.66 **2.65**	2.69		V
	Output Swing Negative	V_{IN} = V_{SS}		19	35 **37**	mV
I_{SC}	Output Short-Circuit Current (6)(7)	Sourcing, V_{IN} = V_{DD}, V_{OUT} = V_{SS}	−21 **−18**	−25		mA
		Sinking, V_{IN} = V_{SS}, V_{OUT} = V_{DD}	23 **15**	25		
V_{en_hmin}	Enable High Active Minimum Voltage			1.2		V
V_{en_lmax}	Enable Low Inactive Maximum Voltage			0.6		

(5) Average Temperature Coefficient is determined by dividing the changing in a parameter at temperature extremes by the total temperature change.
(6) Short−Circuit test is a momentary test. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C.
(7) Positive current corresponds to current flowing into the device.

5V ELECTRICAL CHARACTERISTICS

Unless otherwise specified, all limits are specified for T_A = 25°C, V_{DD} = 5V, V_{SS} = 0V, V_{CM} = 1V, $Enable_{1,2}$ = V_{DD}, C_L = 10 pF, R_L = 30 kΩ, Load is connected to V_{SS}, $C_{COUPLING}$ = 10 nF. **Boldface** limits apply at temperature range extremes of operating condition.(1)

Parameter		Test Conditions	Min (2)	Typ (3)	Max (2)	Units
Frequency Domain Response						
SSBW	Small Signal Bandwidth	V_{IN} = 100 mV_{PP}; −3 dB		87		MHz
LSBW	Large Signal Bandwidth	V_{IN} = 1.0 V_{PP}; −3 dB		68		MHz
GFN	Gain Flatness < 0.1 dB	f > 100 kHz		25		MHz
Distortion and Noise Performance						
φ_n	Phase Noise	V_{IN} = 1 V_{PP}, f_C = 38.4 MHz, Δf = 1 kHz		−123		dBc/Hz
		V_{IN} = 1 V_{PP}, f_C = 38.4 MHz, Δf = 10 kHz		−132		dBc/Hz

(1) The Electrical Characteristics tables show performance under the specified Recommended Operating Conditions except as otherwise modified by the Electrical Characteristics Conditions and/or Notes. Typical values represent typical performance as measured by production tests. Individual parts may vary.
(2) Datasheet min/max limits are specified by test or statistical analysis.
(3) Typical values represent the most likely parametric norms at T_A = +25°C, and at the Recommended Operation Conditions at the time of product characterization.

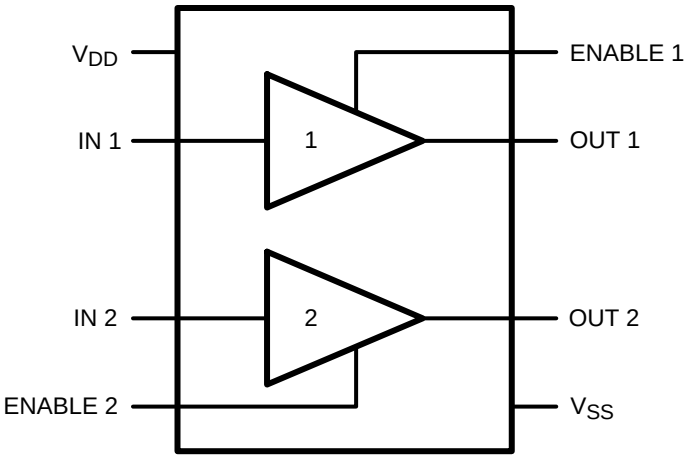
5V ELECTRICAL CHARACTERISTICS (continued)

Unless otherwise specified, all limits are specified for T_A = 25°C, V_{DD} = 5V, V_{SS} = 0V, V_{CM} = 1V, $Enable_{1,2}$ = V_{DD}, C_L = 10 pF, R_L = 30 kΩ, Load is connected to V_{SS}, $C_{COUPLING}$ = 10 nF. **Boldface** limits apply at temperature range extremes of operating condition.(1)

Parameter		Test Conditions	Min (2)	Typ (3)	Max (2)	Units
e_n	Input-Referred Voltage Noise	f = 1 MHz, R_{SOURCE} = 50Ω		12		nV/√Hz
$I_{SOLATION}$	Output to Input	f = 1 MHz, R_{SOURCE} = 50Ω		84		dB
CT	Crosstalk Rejection	f = 38.4 MHz, P_{IN} = 0 dBm		59		dB
Time Domain Response						
t_r	Rise Time	0.1 V_{PP} Step (10-90%)		6		ns
t_f	Fall Time			6		ns
t_s	Settling Time to 0.1%	1 V_{PP} Step		70		ns
OS	Overshoot	0.1V_{PP} Step		13		%
SR	Slew Rate (4)	V_{IN} = 2 V_{PP}		124		V/µs
Static DC Performance						
I_S	Supply Current	$Enable_{1,2}$ = V_{DD} ; No Load		3.4	4.0 **4.1**	mA
		$Enable_1$ = V_{DD}, $Enable_2$ = V_{SS} ; No Load		1.8	2.2 **2.3**	mA
		$Enable_{1,2}$ = V_{SS} ; No Load		32	43 **49**	µA
PSRR	Power Supply Rejection Ratio	DC (3.0V to 5.0V)	65 **64**	68		dB
A_{CL}	Small Signal Voltage Gain	V_{IN} = 0.2 V_{PP}	**0.95**	1.0	**1.05**	V/V
V_{OS}	Output Offset Voltage			−1.4	21 **22**	mV
TC V_{OS}	Temperature Coefficient Output Offset Voltage (5)			2.4		µV/°C
R_{OUT}	Output Resistance	f = 100 kHz		0.5		Ω
		f = 38.4 MHz		126		
		disabled	High Impedance			
Miscellaneous Performance						
R_{IN}	Input Resistance per Buffer	Enable = V_{DD}		138		kΩ
		Enable = V_{SS}		138		
C_{IN}	Input Capacitance per Buffer	Enable = V_{DD}		1.3		pF
		Enable = V_{SS}		1.3		
Z_{IN}	Input Impedance	f = 38.4 MHz, Enable = V_{DD}		4.3		kΩ
		f = 38.4 MHz, Enable = V_{SS}		4.2		
V_O	Output Swing Positive	V_{IN} = V_{DD}	4.96 **4.95**	4.99		V
	Output Swing Negative	V_{IN} = V_{SS}		10	35 **50**	mV
I_{SC}	Output Short-Circuit Current (6)(7)	Sourcing, V_{IN} = V_{DD}, V_{OUT} = V_{SS}	−80 **−62**	−90		mA
		Sinking, V_{IN} = V_{SS}, V_{OUT} = V_{DD}	60 **43**	65		
V_{en_hmin}	Enable High Active Minimum Voltage			1.2		V
V_{en_lmax}	Enable Low Inactive Maximum Voltage			0.6		

(4) Slew rate is the average of the rising and falling slew rates.
(5) Average Temperature Coefficient is determined by dividing the changing in a parameter at temperature extremes by the total temperature change.
(6) Short−Circuit test is a momentary test. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C.
(7) Positive current corresponds to current flowing into the device.

BLOCK DIAGRAM



TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_{DD} = 2.7V, V_{SS} = 0V, $Enable_{1,2}$ = V_{DD}, C_L = 10 pF, R_L = 30 kΩ and $C_{COUPLING}$ = 10 nF, unless otherwise specified.

Frequency Response

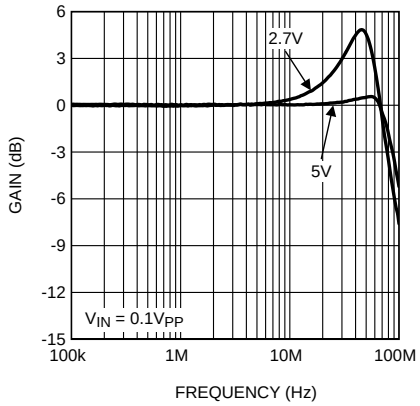


Figure 3.

Phase Response

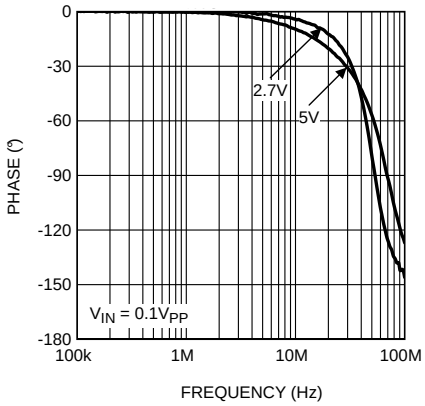


Figure 4.

Frequency Response Over Temperature

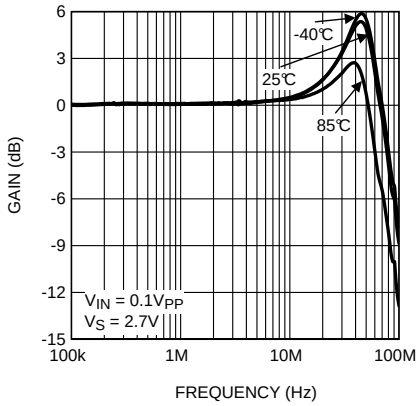


Figure 5.

Frequency Response Over Temperature

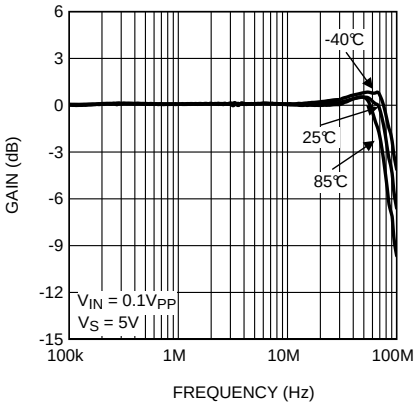


Figure 6.

Phase Response Over Temperature

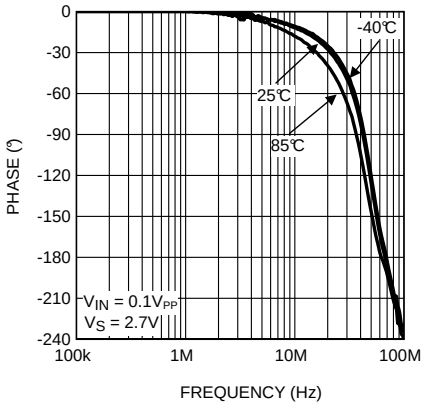


Figure 7.

Phase Response Over Temperature

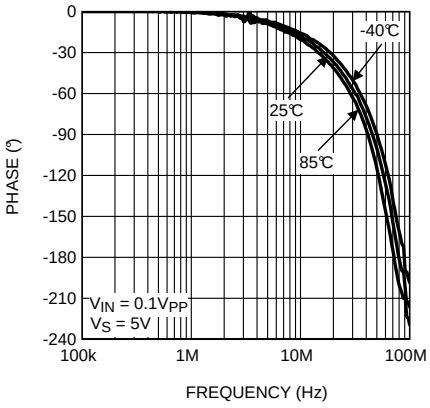


Figure 8.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = 25°C, V_{DD} = 2.7V, V_{SS} = 0V, $Enable_{1,2}$ = V_{DD}, C_L = 10 pF, R_L = 30 kΩ and $C_{COUPLING}$ = 10 nF, unless otherwise specified.

Large Signal Bandwidth

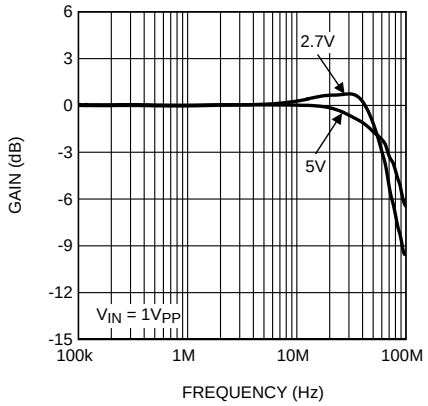


Figure 9.

Gain Flatness < 0.1 dB (GFN)

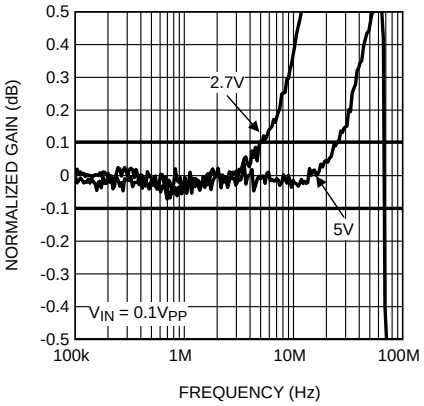


Figure 10.

Voltage Noise

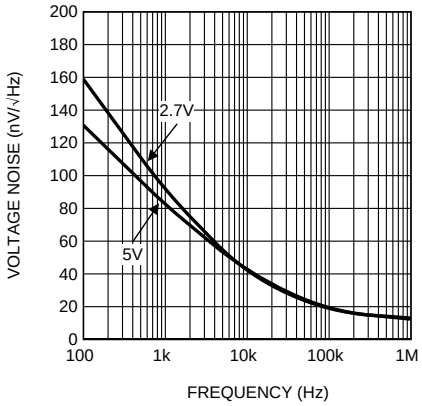


Figure 11.

Phase Noise

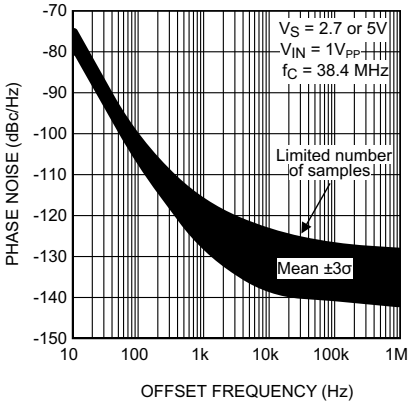


Figure 12.

Isolation Output to Input vs. Frequency

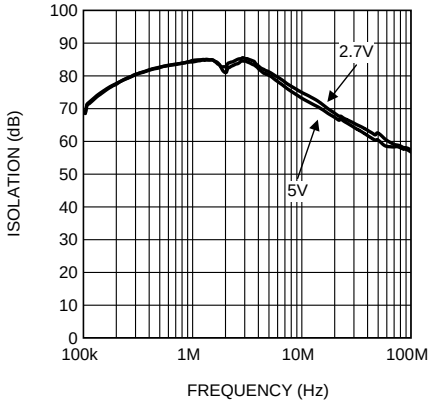


Figure 13.

Crosstalk Rejection vs. Frequency

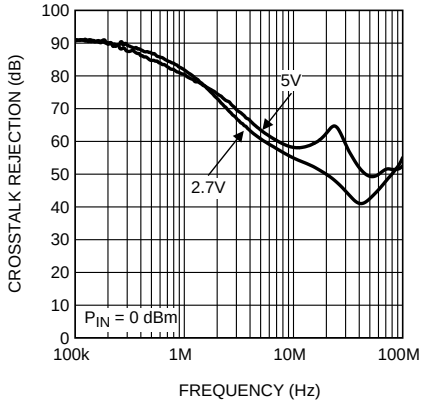


Figure 14.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = 25°C, V_{DD} = 2.7V, V_{SS} = 0V, $Enable_{1,2}$ = V_{DD}, C_L = 10 pF, R_L = 30 kΩ and $C_{COUPLING}$ = 10 nF, unless otherwise specified.

Transient Response Positive

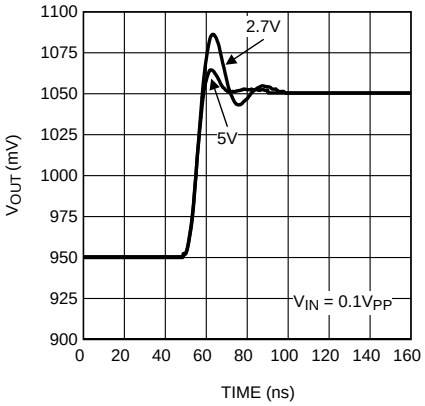


Figure 15.

Transient Response Negative

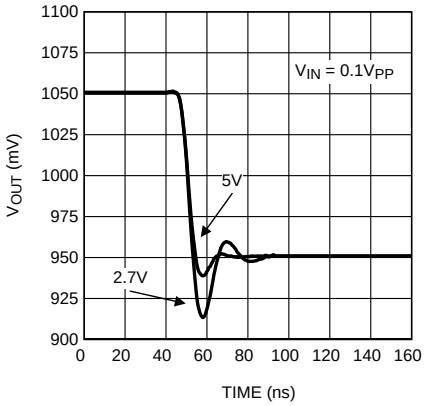


Figure 16.

Small Signal Pulse Response

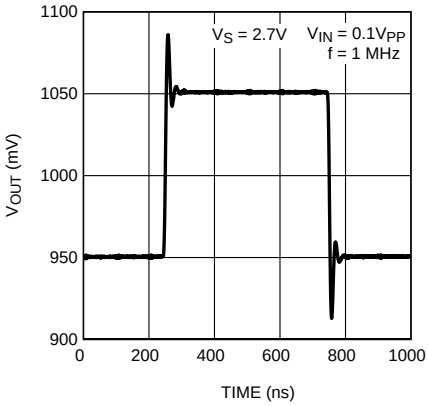


Figure 17.

Small Signal Pulse Response

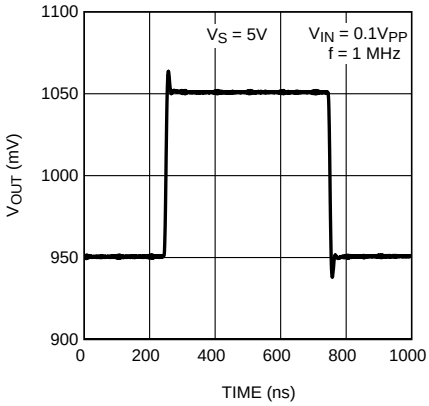


Figure 18.

Large Signal Response

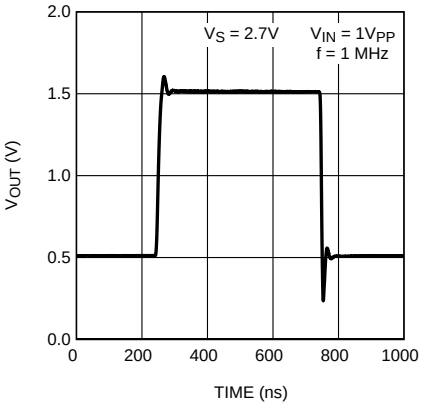


Figure 19.

Large Signal Response

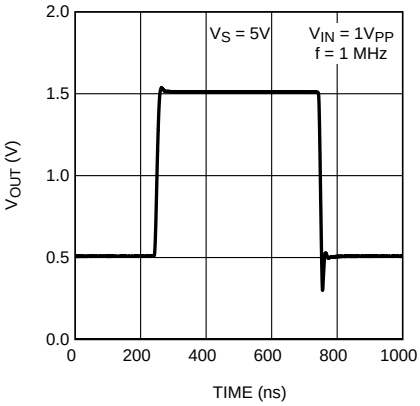


Figure 20.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = 25°C, V_{DD} = 2.7V, V_{SS} = 0V, $Enable_{1,2} = V_{DD}$, C_L = 10 pF, R_L = 30 kΩ and $C_{COUPLING}$ = 10 nF, unless otherwise specified.

I_{SUPPLY} vs. V_{SUPPLY}

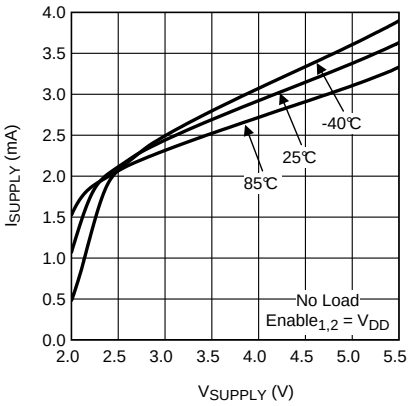


Figure 21.

I_{SUPPLY} vs. V_{SUPPLY}

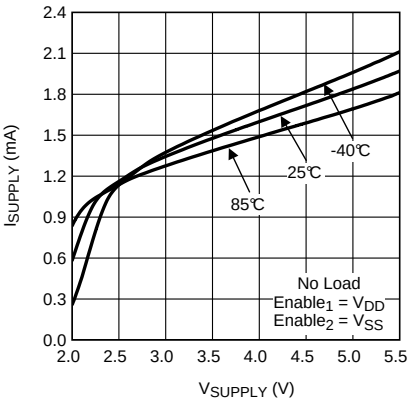


Figure 22.

I_{SUPPLY} vs. V_{SUPPLY}

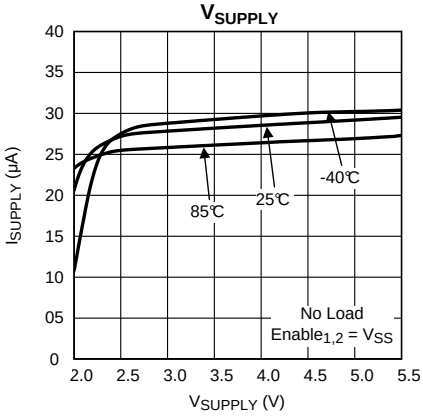


Figure 23.

PSRR vs. Frequency

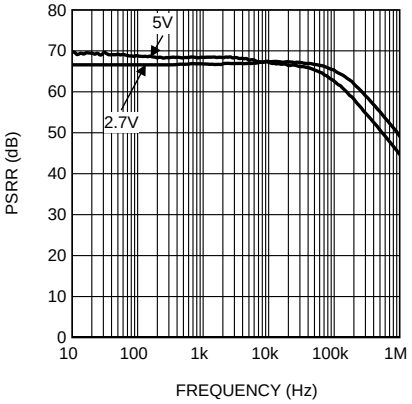


Figure 24.

V_{OS} vs. V_{SUPPLY}

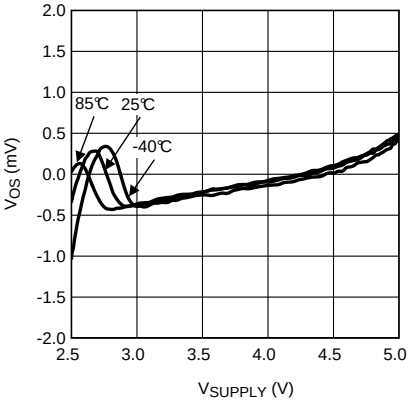


Figure 25.

R_{OUT} vs. Frequency

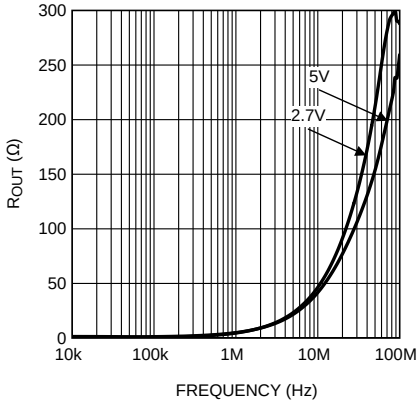


Figure 26.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = 25°C, V_{DD} = 2.7V, V_{SS} = 0V, $Enable_{1,2}$ = V_{DD}, C_L = 10 pF, R_L = 30 kΩ and $C_{COUPLING}$ = 10 nF, unless otherwise specified.

Input Impedance vs. Frequency

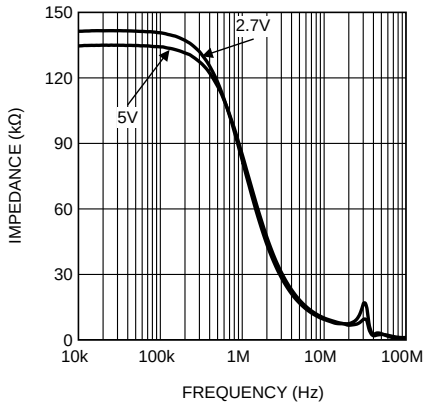


Figure 27.

V_{OUT} vs. I_{OUT} (Sourcing)

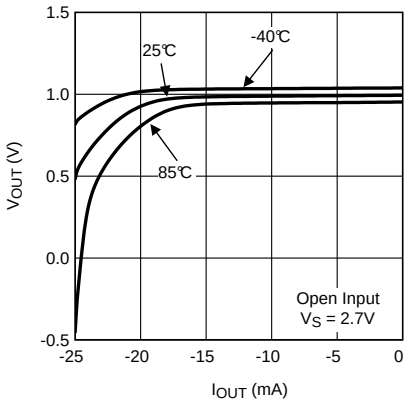


Figure 28.

V_{OUT} vs. I_{OUT} (Sourcing)

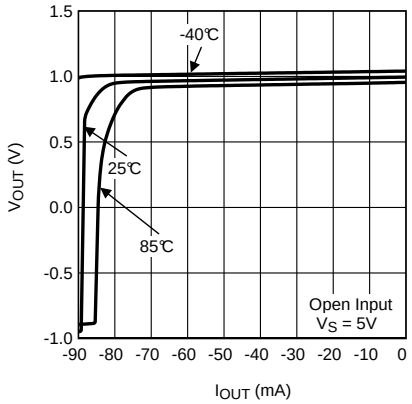


Figure 29.

V_{OUT} vs. I_{OUT} (Sinking)

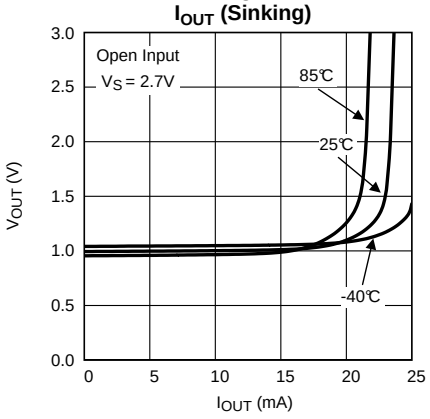


Figure 30.

V_{OUT} vs. I_{OUT} (Sinking)

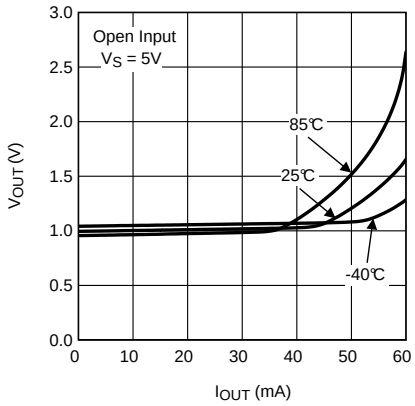


Figure 31.

I_{SC} Sourcing vs. V_{SUPPLY} Over Temperature

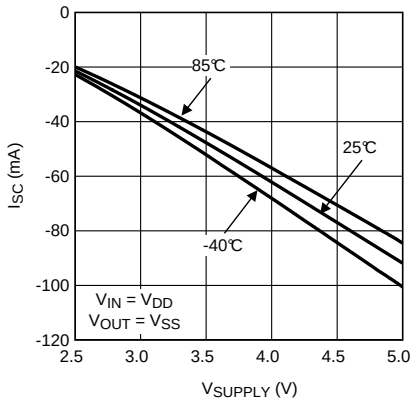


Figure 32.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = 25°C, V_{DD} = 2.7V, V_{SS} = 0V, $Enable_{1,2}$ = V_{DD}, C_L = 10 pF, R_L = 30 kΩ and $C_{COUPLING}$ = 10 nF, unless otherwise specified.

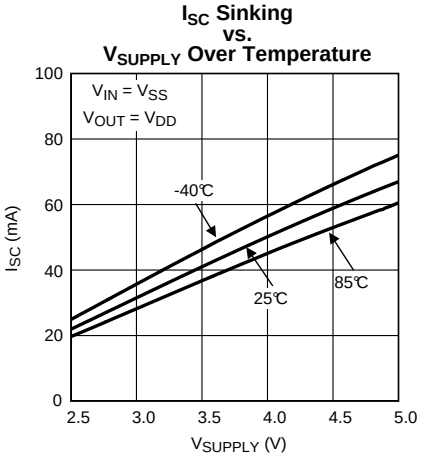


Figure 33.

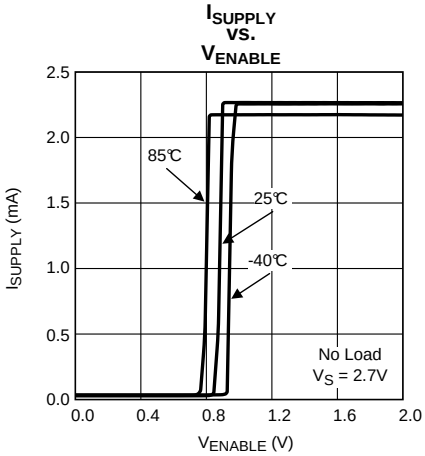


Figure 34.

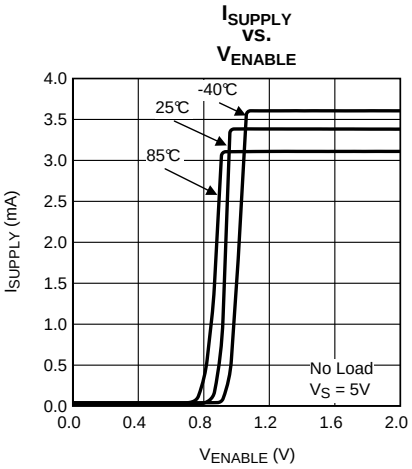


Figure 35.

APPLICATION INFORMATION

GENERAL

The LMH2180 is designed to minimize the effects of spurious signals from the base chip to the oscillator. Also the influence of varying load resistance and capacitance to the oscillator is minimized, while the drive capability is increased.

The inputs of the LMH2180 are internally biased at 1V, making AC coupling possible without external bias resistors.

To optimize current consumption, a buffer that is not in use can be disabled by connecting it's enable pin to V_{SS}.

The LMH2180 has no internal ground reference; therefore, either single or split supply configurations can be used.

The LMH2180 is an easy replacement for discrete circuitry. It simplifies board layout and minimizes the effect of layout related parasitic components.

INPUT CONFIGURATION

The internal 1V input biasing allows AC coupling of the input signal. This biasing avoids the use of external resistors, as depicted in Figure 36. The biasing prevents a large DC load at the oscillators output that creates a load impedance and may affect it's oscillating frequency. As a result of this biasing, the maximum amplitude of the AC signal is $2V_{PP}$.

The coupling capacitance C1 should be large enough to let the AC signal pass. This is a unity gain buffer with rail-to-rail inputs and outputs.

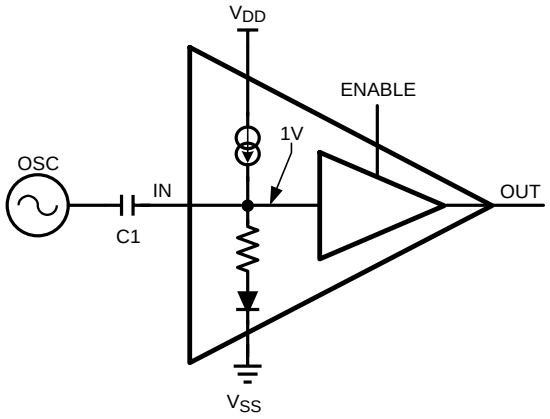


Figure 36. Input Configuration

FREQUENCY PULLING

Frequency pulling is the frequency variation of an oscillator caused by a varying load. In the typical application, the load of the oscillator is a fixed capacitor (C1) in series with the input impedance of the buffer.

To keep the input impedance as constant as possible, the input is biased at 1V, even when the part is disabled. A simplified schematic of the input configuration is shown in Figure 36.

ISOLATION AND CROSSTALK

Output to input isolation prevents the clock signal of the oscillator from being affected by spurious signals generated by the digital blocks behind the output buffer. See Figure 13.

A block diagram of the isolation is shown in Figure 37. Crosstalk rejection between buffers prevents signals from affecting each other. Figure 37 shows a Baseband IC and a Bluetooth module as an example. See Figure 14 for more information.

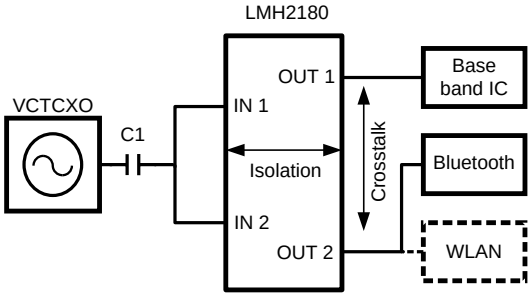


Figure 37. Isolation Block Diagram

DRIVING CAPACITIVE LOADS

Each buffer can drive a capacitive load. Be aware that every capacitor directly connected to the output becomes part of the loop of the buffer. In most applications the load consists of the capacitance of copper tracks and the input capacitance of the application blocks. Capacitance reduces the gain/phase margin and decreases the stability. This leads to peaking in the frequency response and in extreme situations oscillations can occur. To drive a large capacitive load it is recommended to include a series resistor between the buffer and the load capacitor. The best value for this isolation resistance can be found by experimentation.

The LMH2180 datasheet reflects measurements with capacitive loads of 10 pF at the output of the buffers. Most common applications will probably use a lower capacitive load, which will result in lower peaking and significantly greater bandwidth, see Figure 38.

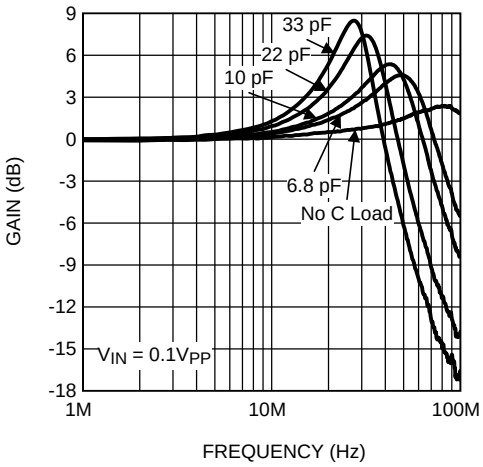


Figure 38. Bandwidth and Peaking

PHASE NOISE

A clock buffer adds noise to the clock signal. This noise causes uncertainty in the phase of the clock signal. This uncertainty is described by jitter (time domain) or phase noise (frequency domain). Communication systems, such as Wireless LAN, require a low jitter/phase noise clock signal to obtain a low Bit Error Rate. Figure 39 shows the frequency domain representation of a clock signal with frequency f_C. Without Phase Noise the entire signal power would only be located at the frequency f_C. Phase Noise spreads some of the power to adjacent frequencies. Phase Noise is usually specified in dBc/Hz at a given frequency offset Δf from the carrier, where dBc is the power level in dB relative to the carrier. The noise power is measured within a 1 Hz bandwidth.

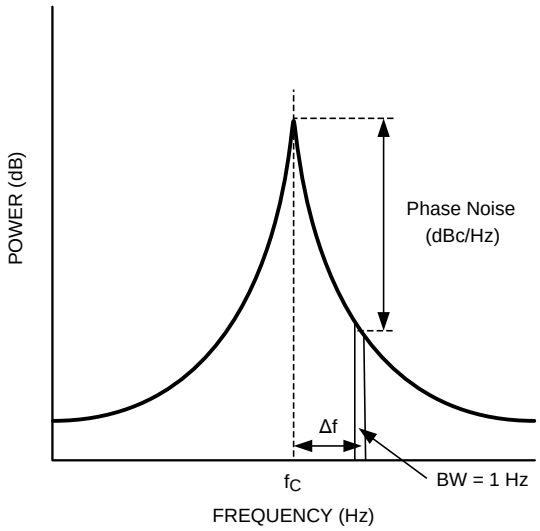


Figure 39. Phase Noise

Figure 40 shows the setup used to measure the LMH2180 phase noise. The clock driving the LMH2180 is a state of the art 38.4MHz TCXO. Both the TCXO phase noise and the phase noise at the LMH2180 output were measured. At offset frequencies of 1 kHz and higher from the carrier, the TCXO phase noise is sufficiently low to accurately calculate the LMH2180 contribution to the phase noise at the output. The LMH6559, whose phase noise contribution can be neglected, is used to drive the 50Ω input impedance of the Signal Source Analyzer.

LAYOUT DESIGN RECOMMENDATION

Careful consideration during circuit design and PCB layout will eliminate problems and will optimize the performance of the LMH2180. It is best to have the same ground plane on the PCB for all decoupling and other ground connections.

To ensure a clean supply voltage it is best to place decoupling capacitors close to the LMH2180, between V_{DD} and V_{SS}.

Another important issue is the value of the components, because this also determines the sensitivity to disturbances. Resistor values have to be low enough to avoid a significant noise contribution and large enough to avoid a significant increase in power consumption while loading inputs or outputs to heavily.

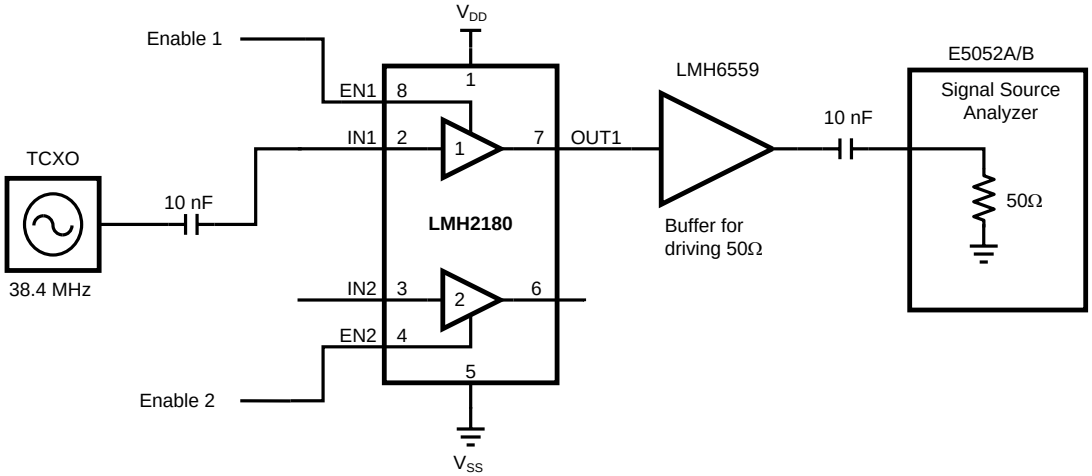


Figure 40. Measurement Setup

REVISION HISTORY

Changes from Revision C (March 2013) to Revision D	Page
• Changed layout of National Data Sheet to TI format	15

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMH2180SD/NOPB	ACTIVE	WSON	NGQ	8	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	2180S	Samples
LMH2180SDE/NOPB	ACTIVE	WSON	NGQ	8	250	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	2180S	Samples
LMH2180TM/NOPB	ACTIVE	DSBGA	YFQ	8	250	RoHS & Green	SNAGCU	Level-1-260C-UNLIM		A	Samples
LMH2180TMX/NOPB	ACTIVE	DSBGA	YFQ	8	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM		A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

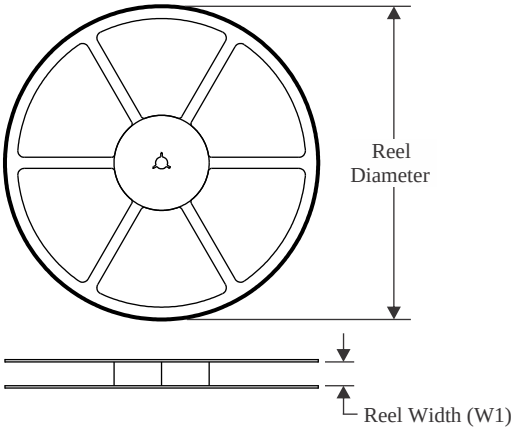
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals.
TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

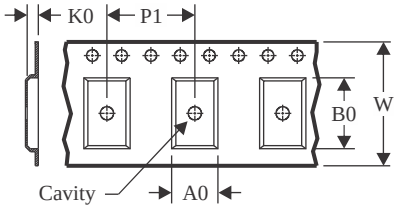
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

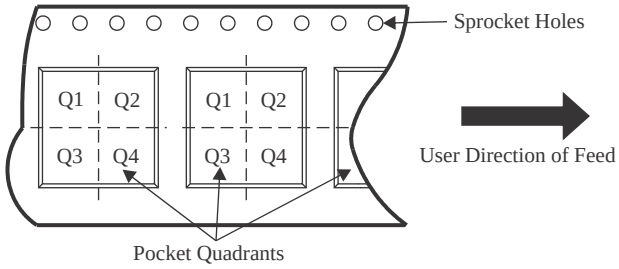


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

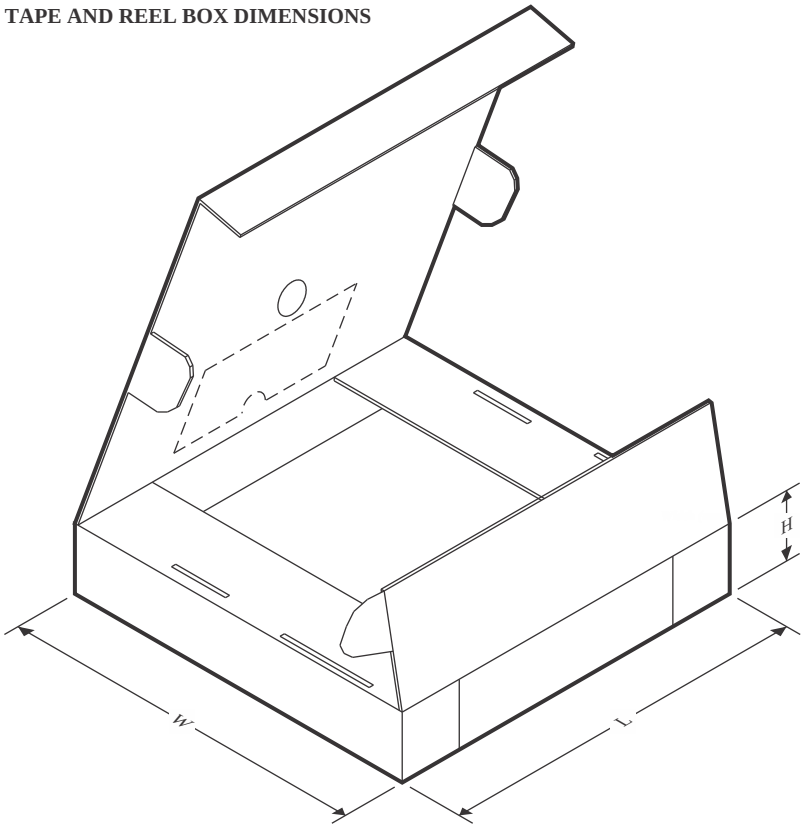
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMH2180SD/NOPB	WSON	NGQ	8	1000	178.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
LMH2180SDE/NOPB	WSON	NGQ	8	250	178.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
LMH2180TM/NOPB	DSBGA	YFQ	8	250	178.0	8.4	1.35	1.35	0.76	4.0	8.0	Q1
LMH2180TMX/NOPB	DSBGA	YFQ	8	3000	178.0	8.4	1.35	1.35	0.76	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

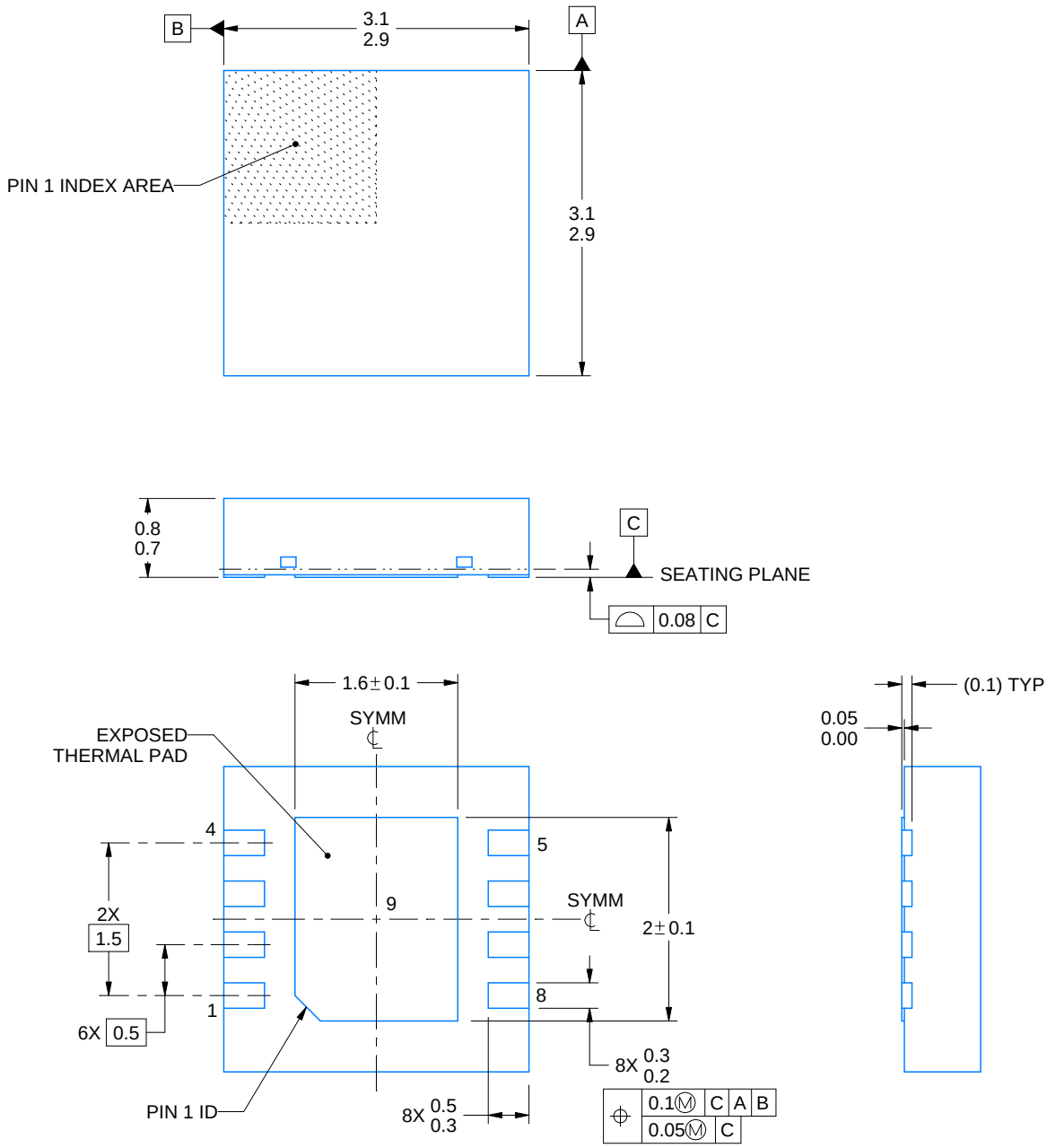
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMH2180SD/NOPB	WSON	NGQ	8	1000	208.0	191.0	35.0
LMH2180SDE/NOPB	WSON	NGQ	8	250	208.0	191.0	35.0
LMH2180TM/NOPB	DSBGA	YFQ	8	250	208.0	191.0	35.0
LMH2180TMX/NOPB	DSBGA	YFQ	8	3000	208.0	191.0	35.0

PACKAGE OUTLINE

NGQ0008A

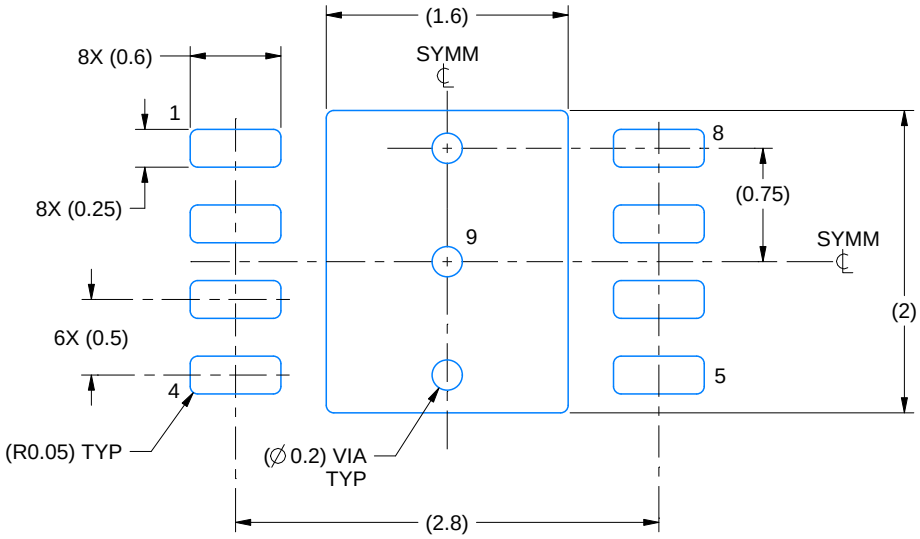
WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

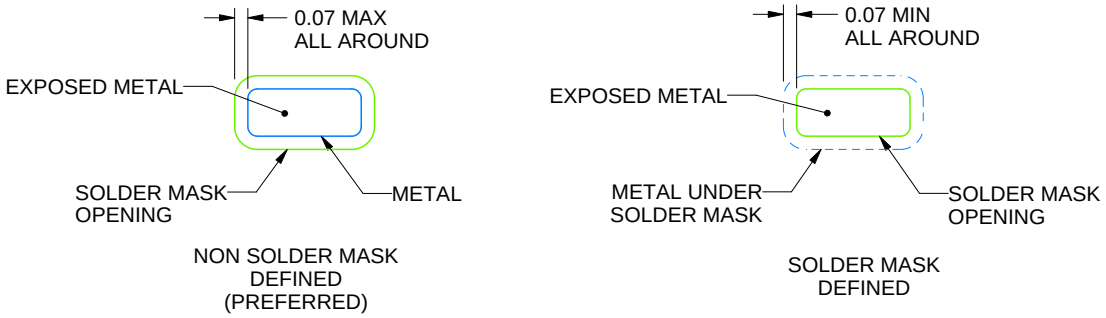


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X

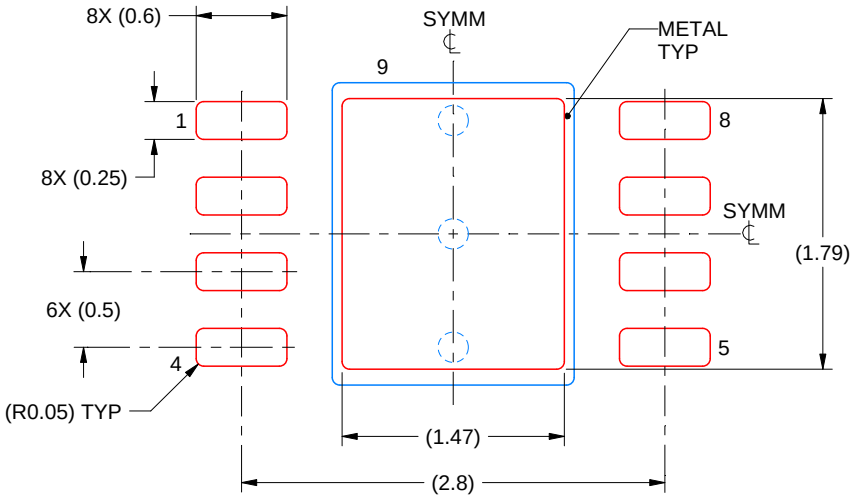


SOLDER MASK DETAILS

4214922/A 03/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

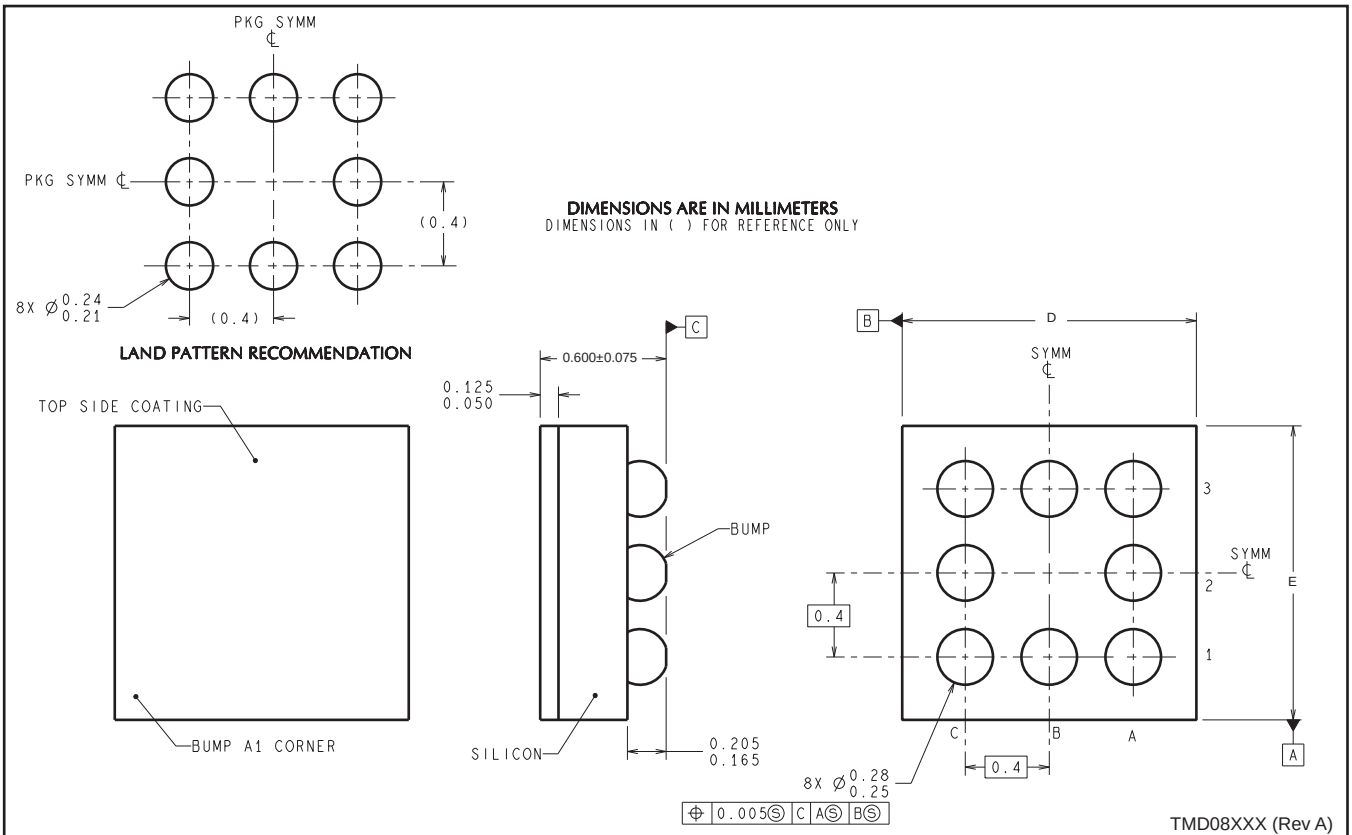
EXPOSED PAD 9:
82% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4214922/A 03/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

YFQ0008



D: Max = 1.24 mm, Min = 1.18 mm

E: Max = 1.24 mm, Min = 1.18 mm

4215076/A 12/12

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.

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