

2.5 V / 3.3 V 2:1:10 Differential ECL/PECL/HSTL Clock Driver

MC100LVEP111

Description

The MC100LVEP111 is a low skew 2:1:10 differential driver, designed with clock distribution in mind, accepting two clock sources into an input multiplexer. The PECL input signals can be either differential or single-ended (if the V_{BB} output is used). HSTL inputs can be used when the LVEP111 is operating under PECL conditions.

The LVEP111 specifically guarantees low output-to-output skew. Optimal design, layout, and processing minimize skew within a device and from device to device.

To ensure tightest skew, both sides of differential outputs identically terminate into $50\ \Omega$ even if only one output is being used. If an output pair is unused, both outputs may be left open (unterminated) without affecting skew.

The MC100LVEP111, as with most other ECL devices, can be operated from a positive V_{CC} supply in PECL mode. This allows the LVEP111 to be used for high performance clock distribution in +3.3 V or +2.5 V systems. Single-ended CLK input operation is limited to a $V_{CC} \geq 3.0\text{ V}$ in PECL mode, or $V_{EE} \leq -3.0\text{ V}$ in NECL mode when using V_{BB} (See Figure 11). Full operating range is available when using an external voltage reference (See Figure 10). Designers can take advantage of the LVEP111's performance to distribute low skew clocks across the backplane or the board.

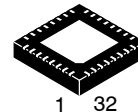
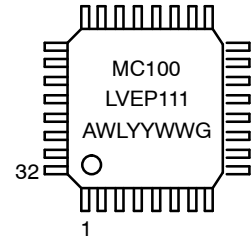
Features

- 85 ps Typical Device-to-Device Skew
- 20 ps Typical Output-to-Output Skew
- Jitter Less than 1 ps RMS
- Additive RMS Phase Jitter: 60 fs @ 156.25 MHz, Typ.
- Maximum Frequency > 3 GHz Typical
- V_{BB} Output
- 430 ps Typical Propagation Delay
- The 100 Series Contains Temperature Compensation
- PECL and HSTL Mode Operating Range: $V_{CC} = 2.375\text{ V}$ to 3.8 V with $V_{EE} = 0\text{ V}$
- NECL Mode Operating Range: $V_{CC} = 0\text{ V}$ with $V_{EE} = -2.375\text{ V}$ to -3.8 V
- Open Input Default State
- LVDS Input Compatible
- Fully Compatible with MC100EP111
- These are Pb-Free Devices

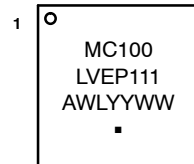
MARKING DIAGRAMS*



LQFP-32, 7x7
CASE 561AB



QFN32
MN SUFFIX
CASE 488AM



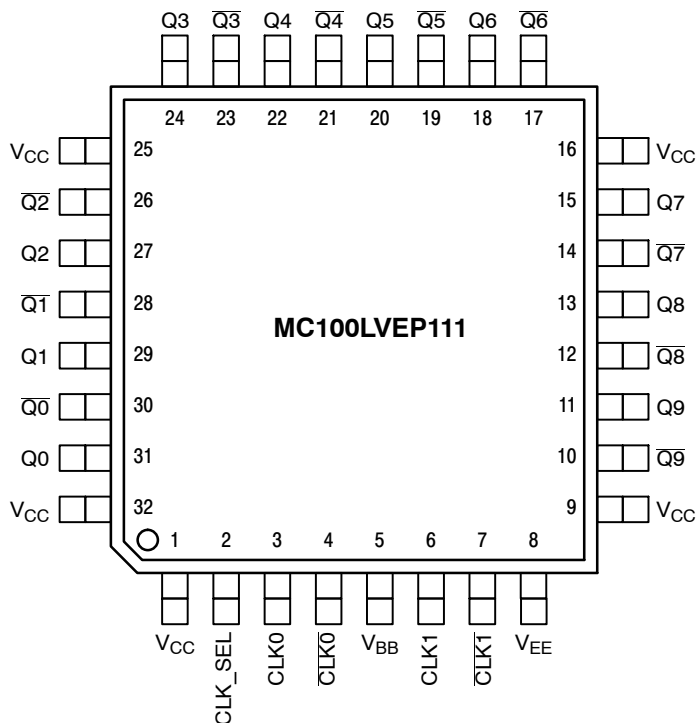
A	= Assembly Location
WL	= Wafer Lot
YY	= Year
WW	= Work Week
G or ■	= Pb-Free Package

*For additional marking information, refer to Application Note AND8002/D.

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 11 of this data sheet.

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Warning: All V_{CC} and V_{EE} pins must be externally connected to Power Supply to guarantee proper operation.

Figure 1. LQFP-32 Pinout (Top View)

Table 1. PIN DESCRIPTION

PIN	FUNCTION
CLK0*, $\overline{\text{CLK0}}^{**}$	ECL/PECL/HSTL CLK Input
CLK1*, $\overline{\text{CLK1}}^{**}$	ECL/PECL/HSTL CLK Input
Q0:9, $\overline{\text{Q0}}:9$	ECL/PECL Outputs
CLK_SEL*	ECL/PECL Active Clock Select Input
V _{BB}	Reference Voltage Output
V _{CC}	Positive Supply
V _{EE}	Negative Supply
EP	The exposed pad (EP) on the package bottom must be attached to a heat-sinking conduit. The exposed pad may only be electrically connected to V _{EE} .

* Pins will default LOW when left open.

** Pins will default to 2/3V_{CC} when left open.

Table 2. FUNCTION TABLE

CLK_SEL	Active Input
L	CLK0, $\overline{\text{CLK0}}$
H	CLK1, $\overline{\text{CLK1}}$

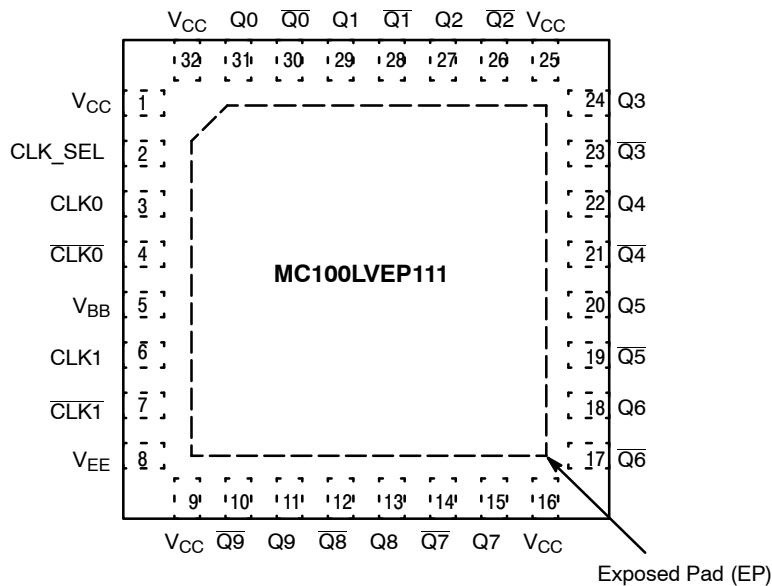


Figure 2. QFN-32 Pinout (Top View)

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Table 3. ATTRIBUTES

Characteristics		Value	
Internal Input Pulldown Resistor		75 kΩ	
Internal Input Pullup Resistor		37.5 kΩ	
ESD Protection	Human Body Model Machine Model Charged Device Model	> 2 kV > 100 V > 2 kV	
Moisture Sensitivity (Note 1)		Pb Pkgs	Pb-Free Pkgs
LQFP		Level 2	Level 2
QFN		Level 1	Level 1
Flammability Rating	Oxygen Index: 28 to 34	UL 94 V-0 @ 0.125 in	
Transistor Count		602 Devices	
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test			

1. For additional information, refer to Application Note AND8003/D.

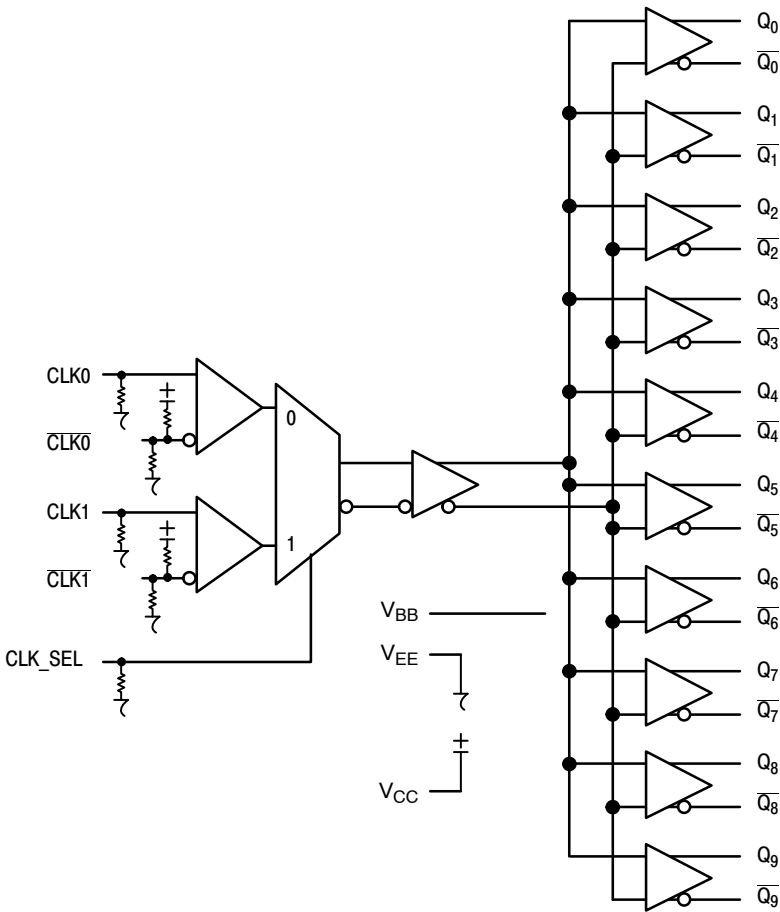


Figure 3. Logic Diagram

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Table 4. MAXIMUM RATINGS

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
V_{CC}	PECL Mode Power Supply	$V_{EE} = 0\text{ V}$		6	V
V_{EE}	NECL Mode Power Supply	$V_{CC} = 0\text{ V}$		-6	V
V_I	PECL Mode Input Voltage	$V_{EE} = 0\text{ V}$	$V_I \leq V_{CC}$	6	V
	NECL Mode Input Voltage	$V_{CC} = 0\text{ V}$	$V_I \geq V_{EE}$	-6	V
I_{out}	Output Current	Continuous Surge		50	mA
				100	mA
I_{BB}	V_{BB} Sink/Source			± 0.5	mA
T_A	Operating Temperature Range			-40 to +85	°C
T_{stg}	Storage Temperature Range			-65 to +150	°C
θ_{JA}	Thermal Resistance (Junction-to-Ambient)	0 lfpm	LQFP-32	80	°C/W
		500 lfpm	LQFP-32	55	°C/W
θ_{JC}	Thermal Resistance (Junction-to-Case)	Standard Board	LQFP-32	12 to 17	°C/W
θ_{JA}	Thermal Resistance (Junction-to-Ambient)	0 lfpm	QFN-32	31	°C/W
		500 lfpm	QFN-32	27	°C/W
θ_{JC}	Thermal Resistance (Junction-to-Case)	2S2P	QFN-32	12	°C/W
T_{sol}	Wave Solder	< 3 sec @ 248°C < 3 sec @ 260°C		265	°C
	Pb-Free (QFN-32 Only)			265	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

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Table 5. PECL DC CHARACTERISTICS $V_{CC} = 2.5 \text{ V}$; $V_{EE} = 0 \text{ V}$ (Note 2)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current	60	90	120	60	90	120	60	90	120	mA
V_{OH}	Output HIGH Voltage (Note 3)	1355	1480	1605	1355	1480	1605	1355	1480	1605	mV
V_{OL}	Output LOW Voltage (Note 3)	505	730	900	505	730	900	505	730	900	mV
V_{IH}	Input HIGH Voltage (Single-Ended) (Note 4)	1335		1620	1335		1620	1275		1620	mV
V_{IL}	Input LOW Voltage (Single-Ended) (Note 4)	505		875	505		875	505		875	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 5)	1.2		2.5	1.2		2.5	1.2		2.5	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current CLK CLK	0.5 -150			0.5 -150			0.5 -150			μA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

2. Input and output parameters vary 1:1 with V_{CC} . V_{EE} can vary + 0.125 V to -1.3 V.

3. All loading with 50 Ω to V_{EE} .

4. Do not use V_{BB} at $V_{CC} < 3.0 \text{ V}$.

5. V_{IHCMR} min varies 1:1 with V_{EE} ; V_{IHCMR} max varies 1:1 with V_{CC} . The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

Table 6. PECL DC CHARACTERISTICS $V_{CC} = 3.3 \text{ V}$; $V_{EE} = 0 \text{ V}$ (Note 6)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current	60	90	120	60	90	120	60	90	120	mA
V_{OH}	Output HIGH Voltage (Note 7)	2155	2280	2405	2155	2280	2405	2155	2280	2405	mV
V_{OL}	Output LOW Voltage (Note 7)	1305	1530	1700	1305	1530	1700	1305	1530	1700	mV
V_{IH}	Input HIGH Voltage (Single-Ended)	2135		2420	2135		2420	2135		2420	mV
V_{IL}	Input LOW Voltage (Single-Ended)	1305		1675	1305		1675	1305		1675	mV
V_{BB}	Output Reference Voltage (Note 8)	1775	1875	1975	1775	1875	1975	1775	1875	1975	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 9)	1.2		3.3	1.2		3.3	1.2		3.3	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current CLK CLK	0.5 -150			0.5 -150			0.5 -150			μA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

6. Input and output parameters vary 1:1 with V_{CC} . V_{EE} can vary + 0.925 V to -0.5 V.

7. All loading with 50 Ω to $V_{CC} - 2.0 \text{ V}$.

8. Single ended input operation is limited $V_{CC} \geq 3.0 \text{ V}$ in PECL mode.

9. V_{IHCMR} min varies 1:1 with V_{EE} ; V_{IHCMR} max varies 1:1 with V_{CC} . The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

Table 7. NECL DC CHARACTERISTICS $V_{CC} = 0 \text{ V}$, $V_{EE} = -2.375 \text{ V}$ to -3.8 V (Note 10)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current	60	90	120	60	90	120	60	90	120	mA
V_{OH}	Output HIGH Voltage (Note 11)	-1145	-1020	-895	-1145	-1020	-895	-1145	-1020	-895	mV
V_{OL}	Output LOW Voltage (Note 11)	-1995	-1770	-1600	-1995	-1770	-1600	-1995	-1770	-1600	mV

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Table 7. NECL DC CHARACTERISTICS $V_{CC} = 0\text{ V}$, $V_{EE} = -2.375\text{ V}$ to -3.8 V (Note 10)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{IH}	Input HIGH Voltage (Single-Ended)	-1165		-880	-1165		-880	-1165		-880	mV
V_{IL}	Input LOW Voltage (Single-Ended)	-1995		-1625	-1995		-1625	-1995		-1625	mV
V_{BB}	Output Reference Voltage (Note 12)	-1525	-1425	-1325	-1525	-1425	-1325	-1525	-1425	-1325	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 13)	$V_{EE} + 1.2$		0.0	$V_{EE} + 1.2$		0.0	$V_{EE} + 1.2$		0.0	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current CLK CLK	0.5 -150			0.5 -150			0.5 -150			μA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm.

10. Input and output parameters vary 1:1 with V_{CC} .

11. All loading with $50\ \Omega$ to $V_{CC} - 2.0\text{ V}$.

12. Single ended input operation is limited $V_{EE} \leq -3.0\text{V}$ in NECL mode.

13. V_{IHCMR} min varies 1:1 with V_{EE} , V_{IHCMR} max varies 1:1 with V_{CC} . The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

Table 8. HSTL DC CHARACTERISTICS $V_{CC} = 2.375$ to 3.8 V , $V_{EE} = 0\text{ V}$

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{IH}	Input HIGH Voltage	1200			1200			1200			mV
V_{IL}	Input LOW Voltage			400			400			400	mV
V_x	Input Crossover Voltage	680		900	680		900	680		900	mV
I_{CC}	Power Supply Current	70	100	120	70	100	120	70	100	120	mA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm.

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Table 9. AC CHARACTERISTICS $V_{CC} = 0\text{ V}$; $V_{EE} = -2.375\text{ to }-3.8\text{ V}$ or $V_{CC} = 2.375\text{ to }3.8\text{ V}$; $V_{EE} = 0\text{ V}$ (Note 14)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$f_{\text{maxPECL/HSTL}}$	Maximum Frequency (Figure 4)		3			3			3		GHz
t_{PLH} t_{PHL}	Propagation Delay (Differential Configuration)	325	400	475	350	430	500	375	510	590	ps
t_{skew}	Within-Device Skew (Note 15) Within-Device Skew @ 2.5 V (Note 15) Device-to-Device Skew (Note 16)		20 20 85	25 25 150		20 20 85	25 25 150		25 20 85	35 25 150	ps
t_{JITTER}	CLOCK Random Jitter (RMS) @ $\leq 0.5\text{ GHz}$ @ $\leq 1.0\text{ GHz}$ @ $\leq 1.5\text{ GHz}$ @ $\leq 2.0\text{ GHz}$ @ $\leq 2.5\text{ GHz}$ @ $\leq 3.0\text{ GHz}$		0.209 0.200 0.197 0.220 0.232 0.348	0.5 0.5 0.4 0.5 0.4 0.6		0.204 0.214 0.213 0.224 0.290 0.545	0.5 0.6 0.5 0.5 0.5 0.8		0.221 0.229 0.243 0.292 0.522 0.911	0.5 0.5 0.4 0.6 0.8 1.3	ps
$t_{\text{jit}(\phi)}$	Additive RMS Phase Jitter $f_c = 156.25\text{ MHz}$, Integration Range: 12 kHz to 20 MHz (See Figure 5)					60					fs
V_{PP}	Input Swing (Differential Interconnect Configuration) Measured Single-Ended	150	800	1200	150	800	1200	150	800	1200	mV
t_r/t_f	Output Rise/Fall Time (20%–80%)	105	200	255	125	200	275	150	230	320	ps

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm.

14. Measured with 750 mV source, 50% duty cycle clock source. All loading with $50\ \Omega$ to $V_{CC} - 2.0\text{ V}$.

15. Skew is measured between outputs under identical transitions and conditions on any one device.

16. Device-to-Device skew for identical transitions at identical V_{CC} levels.

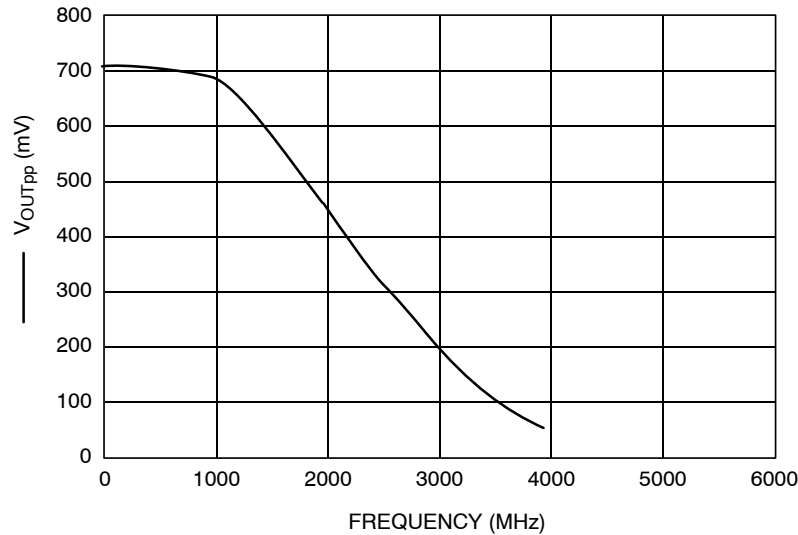


Figure 4. F_{max} Typical

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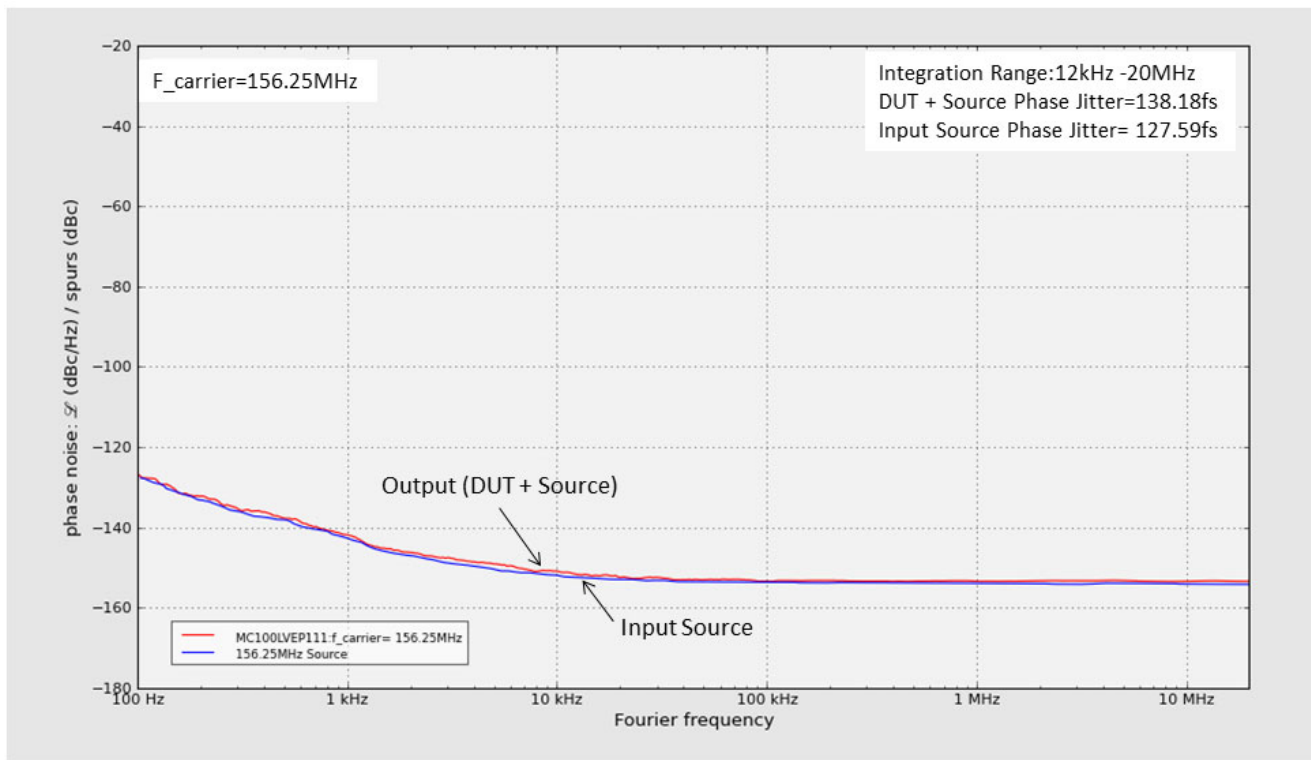


Figure 5. Typical MC100LVEP111 Phase Noise Plot at $f_{\text{Carrier}} = 156.25 \text{ MHz}$, $V_{\text{CC}} = 3.3 \text{ V}$, 25°C

The above phase noise data was captured using Agilent E5052A/B. The data displays the input phase noise and output phase noise used to calculate the additive phase jitter at a specified integration range. The additive RMS phase jitter contributed by the device (integrated between 12 kHz and 20 MHz) is 53 fs. The additive RMS phase jitter performance of the fanout buffer is highly dependent on the phase noise of the input source.

To obtain the most precise additive phase noise measurement, it is vital that the source phase noise be

notably lower than that of the DUT. If the phase noise of the source is greater than the noise floor of the device under test, the source noise will dominate the additive phase jitter calculation and lead to an incorrect negative result for the additive phase noise within the integration range. The Figure above is a good example of the MC100LVEP111 source generator phase noise having a significantly lower floor than the DUT and results in an additive phase jitter of 53 fs.

$$\text{Additive RMS phase jitter} = \sqrt{\text{RMS phase jitter of output}^2 - \text{RMS phase jitter of input}^2}$$

$$53 \text{ fs} = \sqrt{138.18 \text{ fs}^2 - 127.59 \text{ fs}^2}$$

Figure 5 was created with measured data from Agilent-E5052B Signal Source Analyzer using ON Semiconductor Phase Noise Explorer web tool. This free application enables an interactive environment for advanced

phase noise and jitter analysis of timing devices and clock tree designs. To see the performance of MC100LVEP111 beyond conditions outlined in this datasheet, please visit the ON Semiconductor [Green Point Design Tools](#) homepage.

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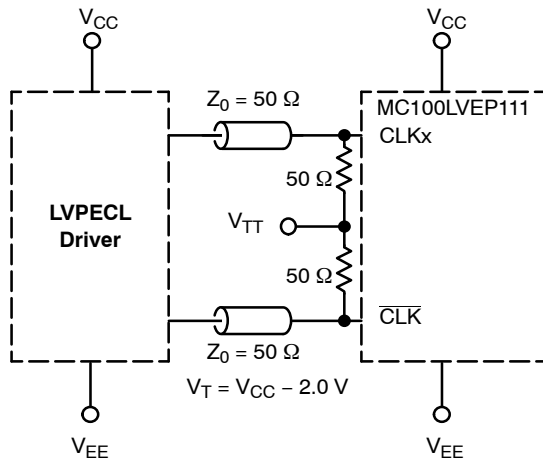


Figure 6. LVPECL in Interface

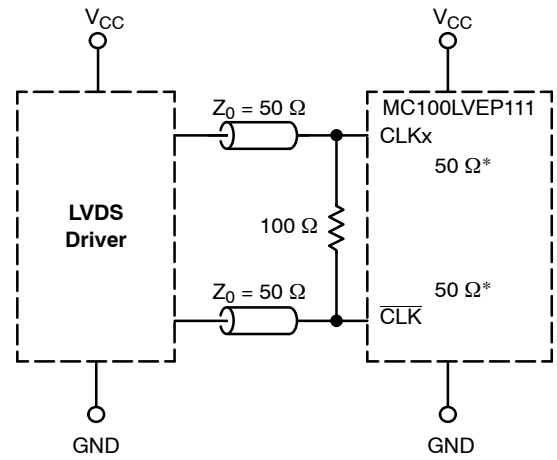


Figure 7. LVDS in Interface

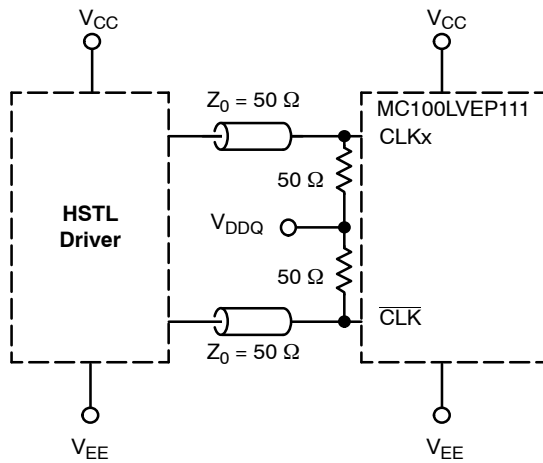


Figure 8. HSTL in Interface

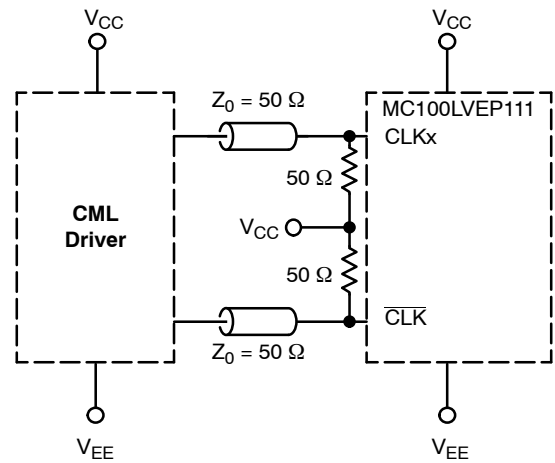


Figure 9. Standard 50 Ω Load CML in Interface

MC100LVEP111

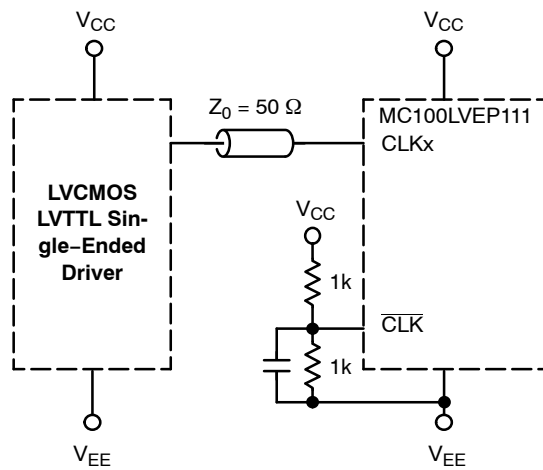


Figure 10. Single-Ended Interface LVC MOS/LVTTL in Interface Using an External Voltage Reference

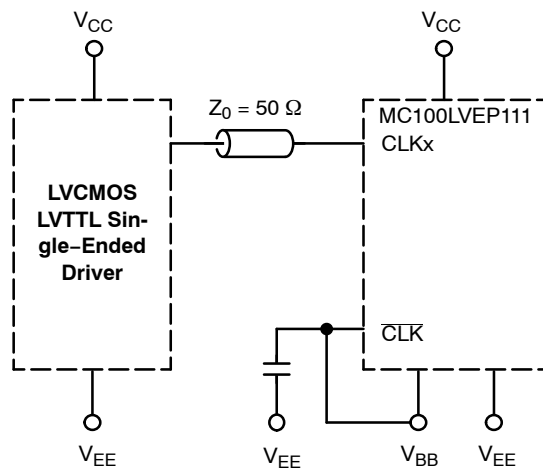


Figure 11. Single-Ended Interface LVC MOS/LVTTL in Interface Using V_{BB}

MC100LVEP111

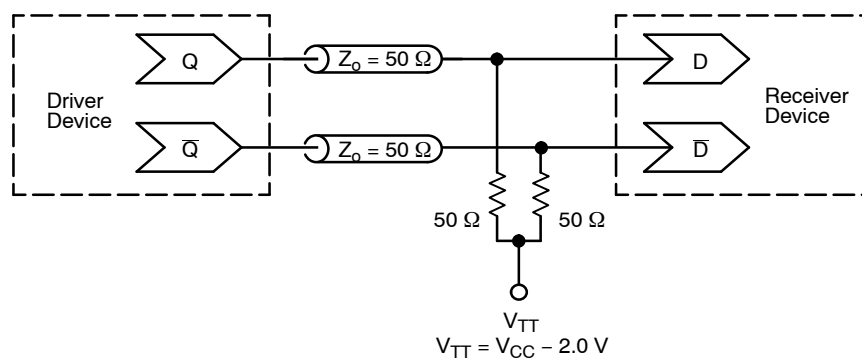


Figure 12. Typical Termination for Output Driver and Device Evaluation
(See Application Note AND8020/D – Termination of ECL Logic Devices.)

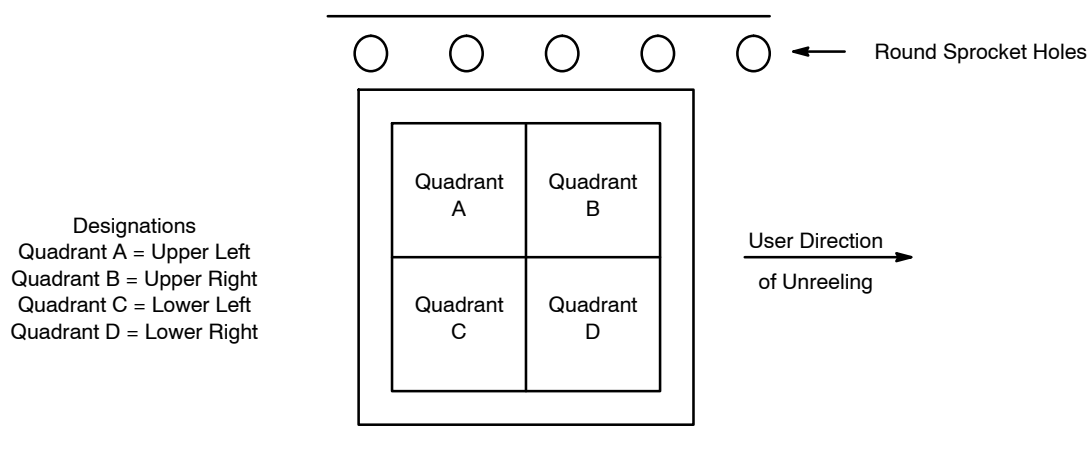


Figure 13. Tape and Reel Pin 1 Quadrant Orientation

ORDERING INFORMATION

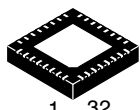
Device	Package	Shipping [†]
MC100LVEP111FAG	LQFP-32 (Pb-Free)	250 Units / Tray
MC100LVEP111FARG	LQFP-32 (Pb-Free)	2000 / Tape & Reel (Pin 1 Orientation in Quadrant B, Figure 13)
M100LVEP111FATWG	LQFP-32 (Pb-Free)	2000 / Tape & Reel (Pin 1 Orientation in Quadrant A, Figure 13)
MC100LVEP111MNG	QFN-32 (Pb-Free)	74 Units / Rail
MC100LVEP111MNRG	QFN-32 (Pb-Free)	1000 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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Resource Reference of Application Notes

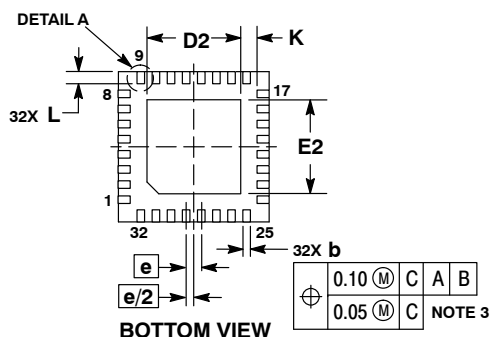
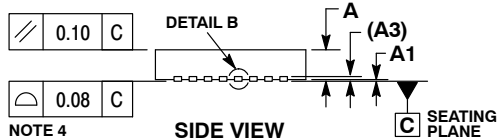
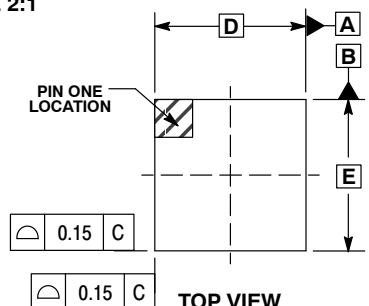
- AN1405/D** – ECL Clock Distribution Techniques
- AN1406/D** – Designing with PECL (ECL at +5.0 V)
- AN1503/D** – ECLinPS™ I/O SPICE Modeling Kit
- AN1504/D** – Metastability and the ECLinPS Family
- AN1568/D** – Interfacing Between LVDS and ECL
- AN1672/D** – The ECL Translator Guide
- AND8001/D** – Odd Number Counters Design
- AND8002/D** – Marking and Date Codes
- AND8020/D** – Termination of ECL Logic Devices
- AND8066/D** – Interfacing with ECLinPS
- AND8090/D** – AC Characteristics of ECL Devices



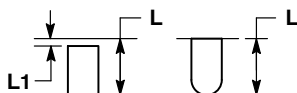
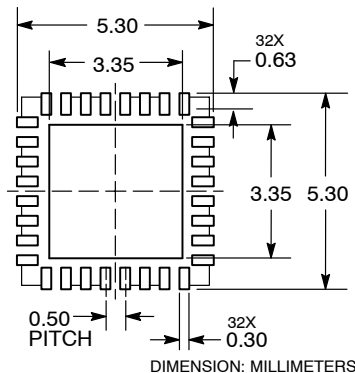
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SCALE 2:1

QFN32 5x5, 0.5P CASE 488AM ISSUE A

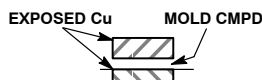
DATE 23 OCT 2013



RECOMMENDED SOLDERING FOOTPRINT*



DETAIL A
ALTERNATE TERMINAL
CONSTRUCTIONS



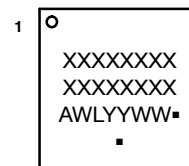
DETAIL B
ALTERNATE
CONSTRUCTION

NOTES:

1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

MILLIMETERS		
DIM	MIN	MAX
A	0.80	1.00
A1		0.05
A3	0.20 REF	
b	0.18	0.30
D	5.00 BSC	
D2	2.95	3.25
E	5.00 BSC	
E2	2.95	3.25
e	0.50 BSC	
K	0.20	
L	0.30	0.50
L1		0.15

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
▪ = Pb-Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking.
Pb-Free indicator, "G" or microdot "▪", may or may not be present.

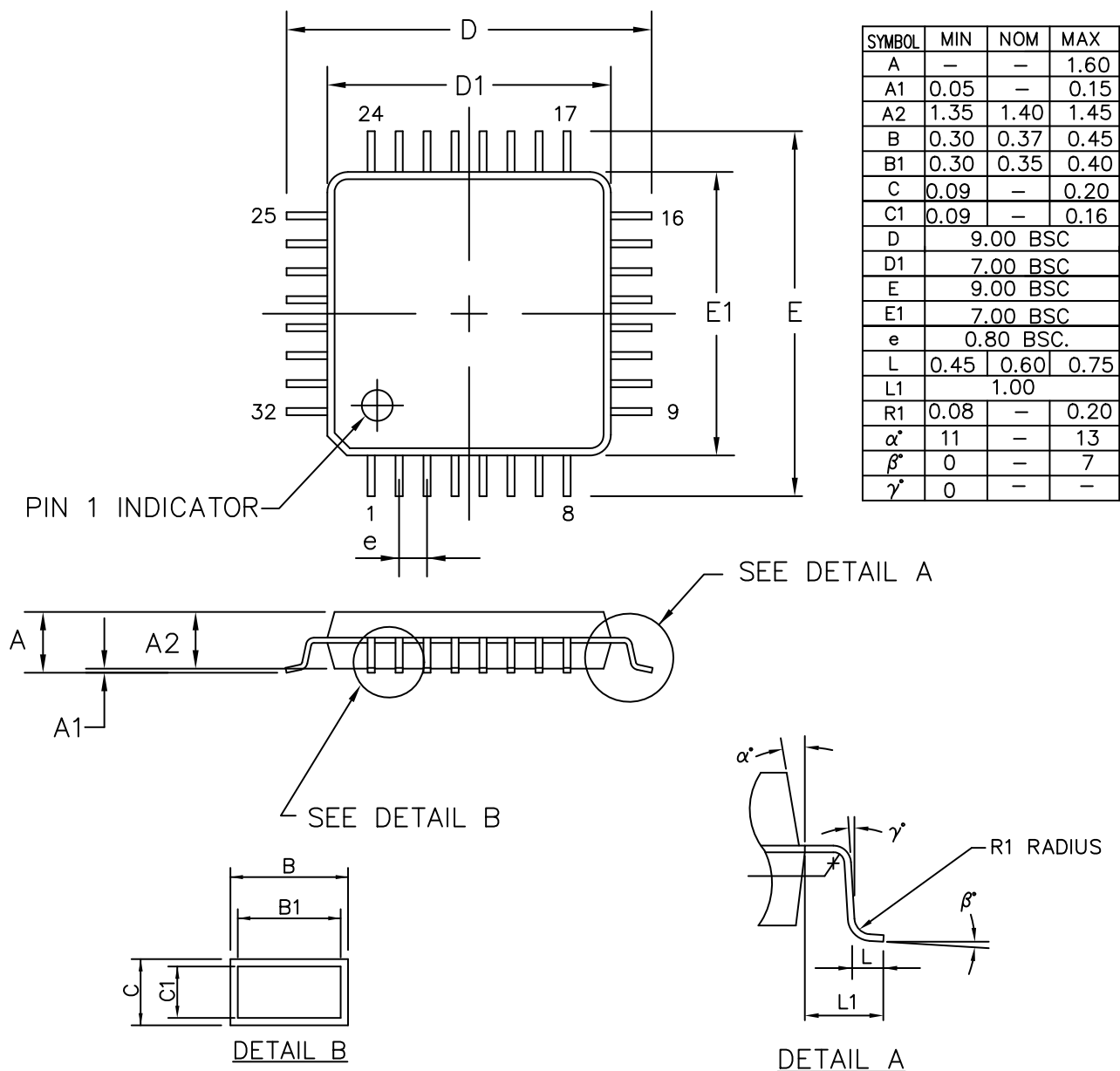
*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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CASE 561AB-01
ISSUE O

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