# CM1451

# LCD and Camera EMI Filter Array with ESD Protection

## Description

The CM1451 is an inductor−capacitor (L−C) based EMI filter array with integrated ESD protection in CSP. The CM1451−06 and CM1451−08 are configured in 6 and 8 channel formats respectively. Each channel is implemented as a 5−pole L−C filter with the component values 9.5 pF − 17 nH − 9.5 pF − 17 nF − 9.5 pF. The CM1451's roll−off frequency at −10 dB attenuation is 500 MHz. It can be used in applications where the data rates are as high as 200 Mbps while providing greater than 35 dB attenuation over the 800 MHz to 2.7 GHz frequency range. The device has ESD protection diodes on every pin that provide a very high level of protection for sensitive electronic components that may be subjected to electrostatic discharge (ESD). The ESD protection diodes connected to the filter ports safely dissipate ESD strikes of ±15 kV, exceeding the Level 4 requirement of the IEC61000−4−2 international standard. Using the MIL−STD−883 (Method 3015) specification for Human Body Model (HBM) ESD, the pins are protected for contact discharges at greater than ±30 kV.

This device is particularly well−suited for portable electronics (e.g. wireless handsets, PDAs) because of its small package format and easy−to−use pin assignments. In particular, the CM1451 is ideal for EMI filtering and protecting data and control lines for the LCD display and camera interface in wireless handsets while maintaining the integrity of signals that have rise/fall times as fast as 2 ns.

The CM1451 incorporates OptiGuard, a coating that results in improved reliability at assembly. The CM1451 is available in a space−saving, low−profile Chip Scale Package with RoHS compliant lead−free finishing.

## Features

- High Bandwidth, High RF Rejection Filter Array
- Six and Eight Channels of EMI Filtering
- Utilizes Inductor−Based Design Technology for True L−C Filter Implementation
- OptiGuard Coating for Improved Reliability
- Chip Scale Package (CSP) Features Extremely Low Lead Inductance for Optimum Filter and ESD Performance
- 15 kV ESD Protection on Each Channel (IEC 61000−4−2 Level 4, Contact Discharge)
- 30 kV ESD Protection on Each Channel (HBM)
- Better than 40 dB of Attenuation at 1 GHz
- Maintains Signal Integrity for Signals that Have a Risetime and Falltime as Fast as 2 ns

## Applications

- LCD and Camera Data Lines in Mobile Handsets
- I/O Port Protection for Mobile Handsets, Notebook Computers, PDAs, etc.
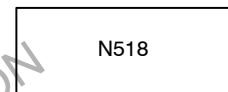- Wireless Handsets / Cell Phones

## ON Semiconductor®

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**WLCSP15**
CP SUFFIX
CASE 567BT

**WLCSP20**
CP SUFFIX
CASE 567CL

### MARKING DIAGRAM

| N516 | | N518 |
| --- | --- | --- |

CM1451−06
15−Bump CSP Package

CM1451−08
20−Bump CSP Package

N516 = CM1451−06CP
N518 = CM1451−08CP

### ORDERING INFORMATION

| Device | Package | Shipping[†] |
| --- | --- | --- |
| CM1451−06CP | CSP−15 (Pb−Free) | 3500/Tape & Reel |
| CM1451−08CP | CSP−20 (Pb−Free) | 3500/Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

- 15−Bump, 3.006 mm x 1.376 mm Footprint Chip Scale Package (CM1451−06CP)
- 20−Bump, 4.006 mm x 1.376 mm Footprint Chip Scale Package (CM1451−08CP)
- These Devices are Pb−Free and are RoHS Compliant

- EMI Filtering for Data Ports in Cell Phones, PDAs or Notebook Computers
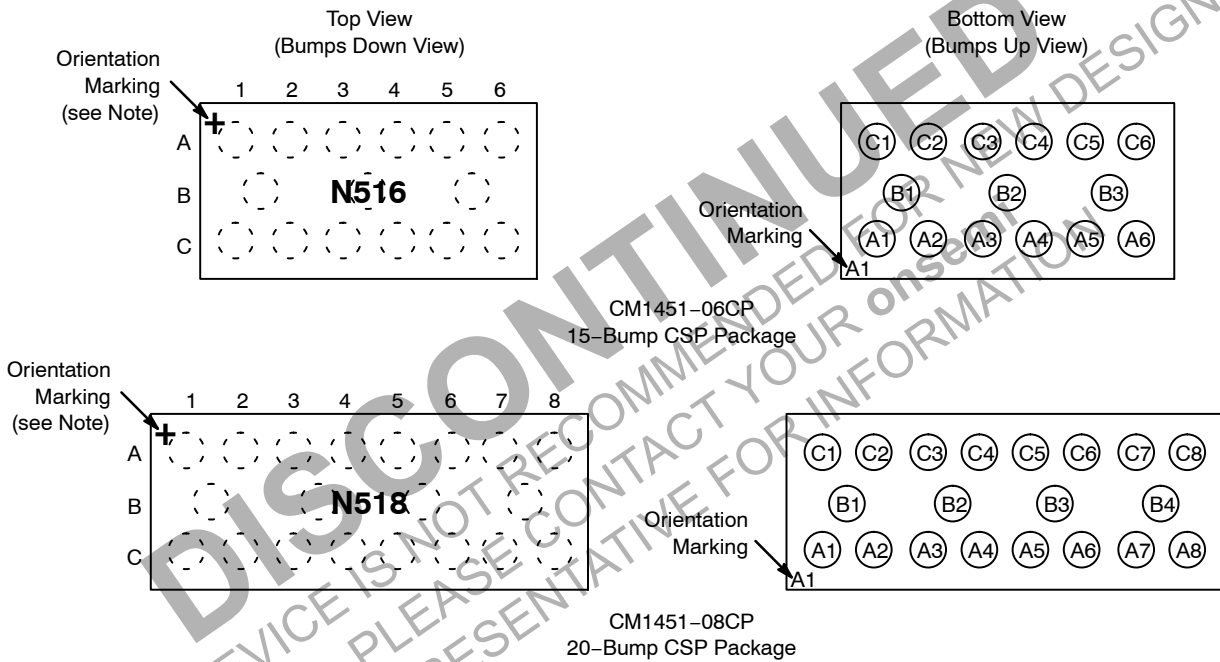- Handheld PCs / PDAs
- LCD and Camera Modules

# CM1451

## BLOCK DIAGRAM



1 of n EMI Filtering + ESD Channels
(n = 6 for CM1451−06, 8 for CM1451−08, m=n/2)
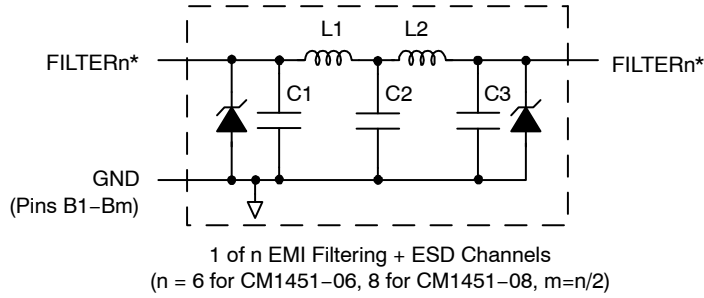
*See Package/Pinout Diagrams for expanded pin information.

## PACKAGE / PINOUT DIAGRAMS



Top View
(Bumps Down View)

Orientation Marking
(see Note)

N516

Bottom View
(Bumps Up View)

Orientation Marking

CM1451−06CP
15−Bump CSP Package

Orientation Marking
(see Note)

N518

Orientation Marking

CM1451−08CP
20−Bump CSP Package

Note: Lead−free devices are specified by using a "+" character for the top side orientation mark.

### Table 1. PIN DESCRIPTIONS

| CM1451−06 | CM1451−08 | | | CM1451−06 | CM1451−08 | | |
|---|---|---|---|---|---|---|---|
| Pin(s) | Pin(s) | Name | Description | Pin(s) | Pin(s) | Name | Description |
| A1 | A1 | FILTER1 | Filter Channel 1 | C1 | C1 | FILTER1 | Filter Channel 1 |
| A2 | A2 | FILTER2 | Filter Channel 2 | C2 | C2 | FILTER2 | Filter Channel 2 |
| A3 | A3 | FILTER3 | Filter Channel 3 | C3 | C3 | FILTER3 | Filter Channel 3 |
| A4 | A4 | FILTER4 | Filter Channel 4 | C4 | C4 | FILTER4 | Filter Channel 4 |
| A5 | A5 | FILTER5 | Filter Channel 5 | C5 | C5 | FILTER5 | Filter Channel 5 |
| A6 | A6 | FILTER6 | Filter Channel 6 | C6 | C6 | FILTER6 | Filter Channel 6 |
| − | A7 | FILTER7 | Filter Channel 7 | − | C7 | FILTER7 | Filter Channel 7 |
| − | A8 | FILTER8 | Filter Channel 8 | − | C8 | FILTER8 | Filter Channel 8 |
| B1−B3 | B1−B4 | GND | Device Ground | | | | |

# CM1451

## SPECIFICATIONS

### Table 2. ABSOLUTE MAXIMUM RATINGS

| Parameter | Rating | Units |
|---|---|---|
| Storage Temperature Range | −65 to +150 | °C |
| Current per Inductor | 30 | mA |
| DC Package Power Rating | 500 | mW |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

### Table 3. STANDARD OPERATING CONDITIONS

| Parameter | Rating | Units |
|---|---|---|
| Operating Temperature Range | −40 to +85 | °C |

### Table 4. ELECTRICAL OPERATING CHARACTERISTICS (Note 1)

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $L_{TOT}$ | Total Channel Inductance ($L_1 + L_2$) | | | 34 | | nH |
| $L_1, L_2$ | Inductance | | | 17 | | nH |
| $R_{DC\ IN-OUT}$ | DC Channel Resistance | | | 18 | | Ω |
| $C_{TOT}$ | Total Channel Capacitance ($C_1 + C_2 + C_3$) | At 2.5 V DC, 1 MHz, 30 mV AC | 22.8 | 28.5 | 34.2 | pF |
| $C_1, C_2, C_3$ | Capacitance | At 2.5 V DC, 1 MHz, 30 mV AC | 7.6 | 9.5 | 11.4 | pF |
| $f_C$ | Cut−off Frequency $Z_{SOURCE} = 50\ \Omega$, $Z_{LOAD} = 50\ \Omega$ | | | 260 | | MHz |
| $f_{RO}$ | Roll−off Frequency at −10 dB Attenuation $Z_{SOURCE} = 50\ \Omega$, $Z_{LOAD} = 50\ \Omega$ | | | 500 | | MHz |
| $V_{DIODE}$ | Diode Standoff Voltage | $I_{DIODE} = 10\ \mu A$ | | 6.0 | | V |
| $I_{LEAK}$ | Diode Leakage Current | $V_{DIODE} = +3.3\ V$ | | 0.1 | 1.0 | μA |
| $V_{SIG}$ | Signal Clamp Voltage     Positive Clamp     Negative Clamp | $I_{LOAD} = 10\ mA$ | 5.6 −1.5 | 6.8 −0.8 | 9.0 −0.4 | V |
| $V_{ESD}$ | In−system ESD Withstand Voltage   a) Human Body Model, MIL−STD−883, Method 3015   b) Contact Discharge per IEC 61000−4−2 Level 4 | (Note 2) | 30 15 | | | kV |
| $R_{DYN}$ | Dynamic Resistance     Positive     Negative | | | 2.30 0.90 | | Ω |

1.  $T_A = 25°C$ unless otherwise specified.
2.  ESD applied to input and output pins with respect to GND, one at a time.

# CM1451

## PERFORMANCE INFORMATION

**Typical Filter Performance ($T_A$ = 25°C, DC Bias = 0 V, 50 Ω Environment)**
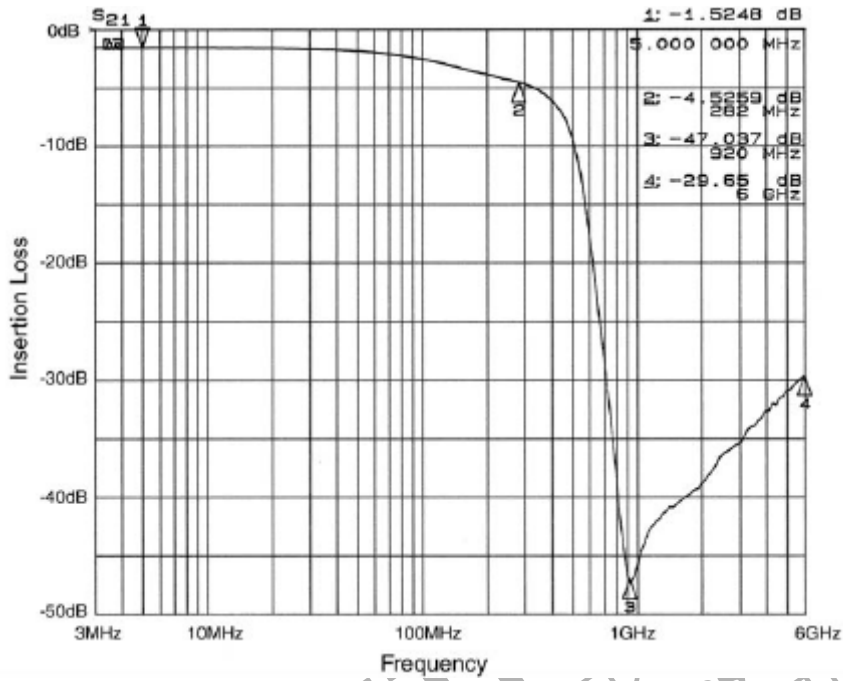

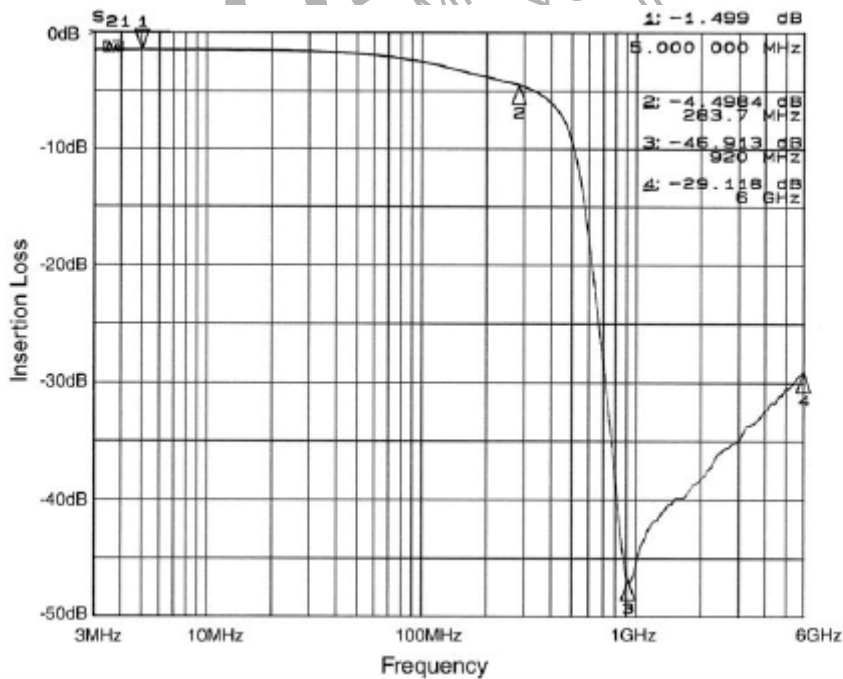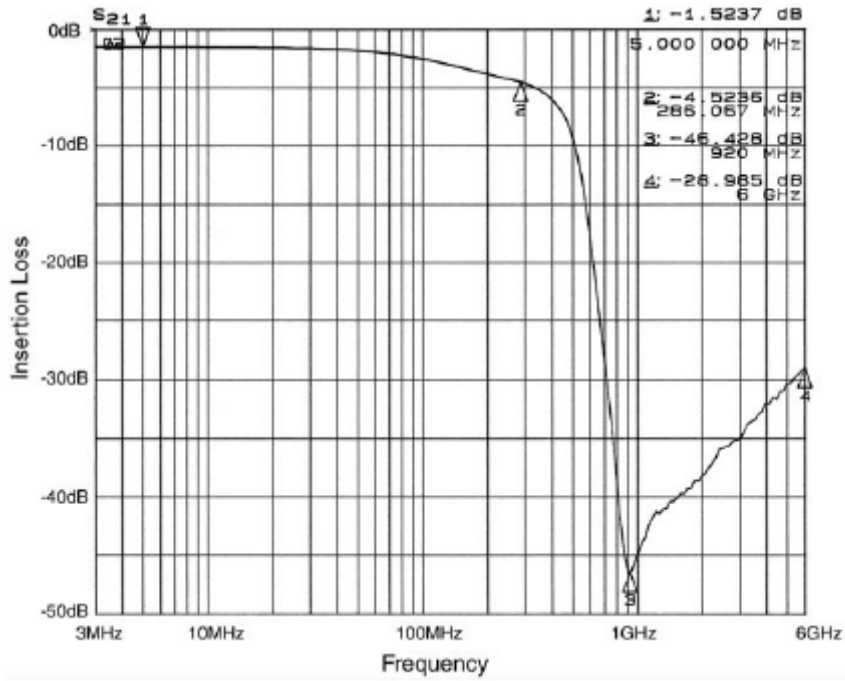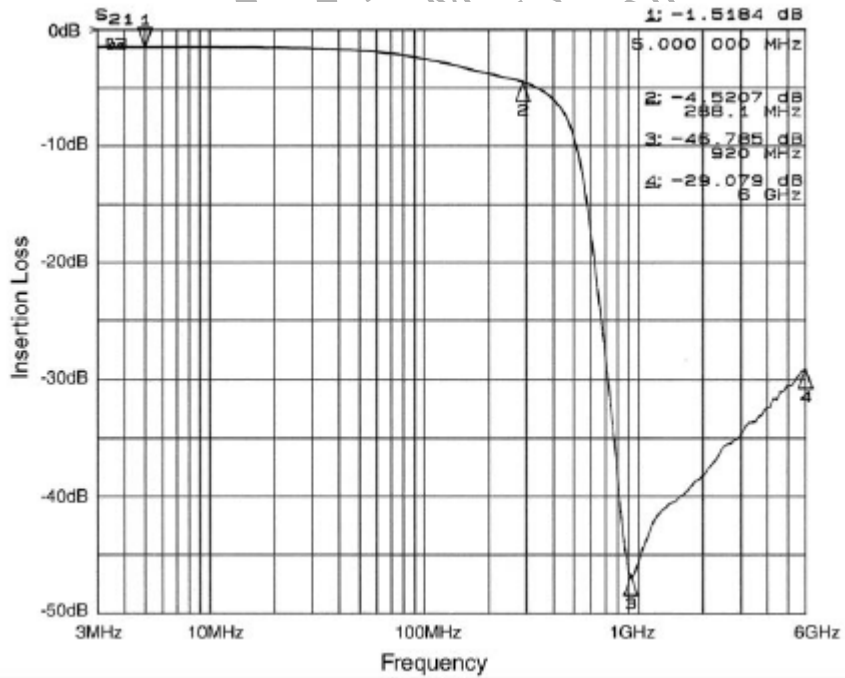
**Figure 1. Insertion Loss vs. Frequency (A1−C1 to GND B1)**
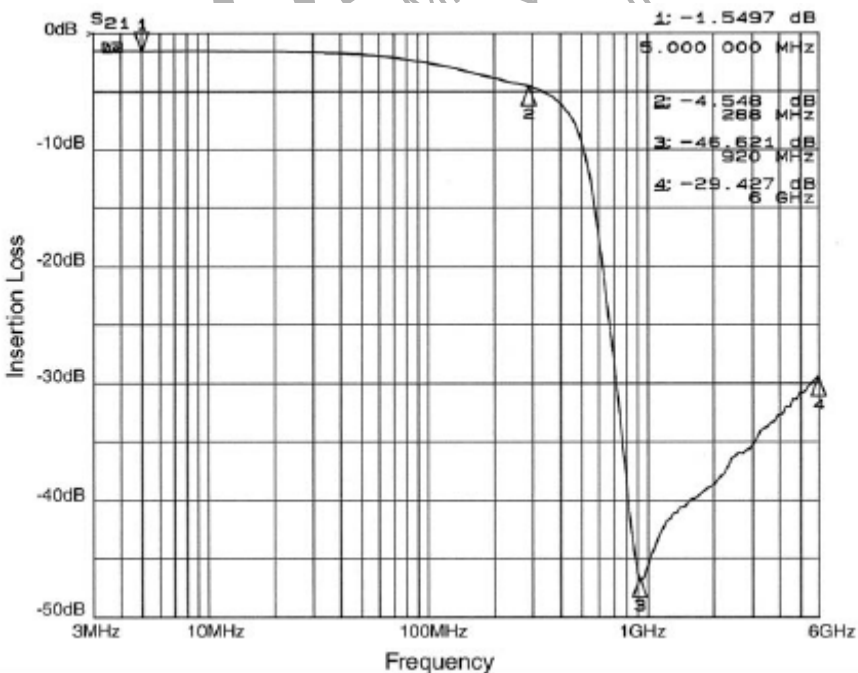


**Figure 2. Insertion Loss vs. Frequency (A2−C2 to GND B1)**

## PERFORMANCE INFORMATION (Cont'd)

**Typical Filter Performance ($T_A$ = 25°C, DC Bias = 0 V, 50 $\Omega$ Environment)**



**Figure 3. Insertion Loss vs. Frequency (A3−C3 to GND B2)**



**Figure 4. Insertion Loss vs. Frequency (A4−C4 to GND B2)**

## PERFORMANCE INFORMATION (Cont'd)

**Typical Filter Performance (T$_A$ = 25°C, DC Bias = 0 V, 50 Ω Environment)**



**Figure 5. Insertion Loss vs. Frequency (A5−C5 to GND B3)**



**Figure 6. Insertion Loss vs. Frequency (A6−C6 to GND B3)**

## PERFORMANCE INFORMATION (Cont'd)
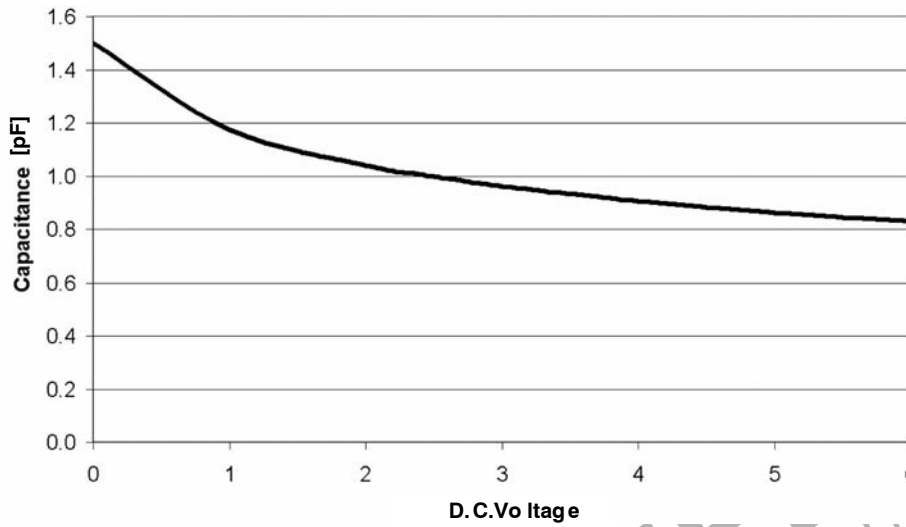


**Figure 7. Filter Capacitance vs. Input Voltage over Temperature
(normalized to capacitance at 2.5 VDC and 25°C)**

**Transient Response Characteristics**
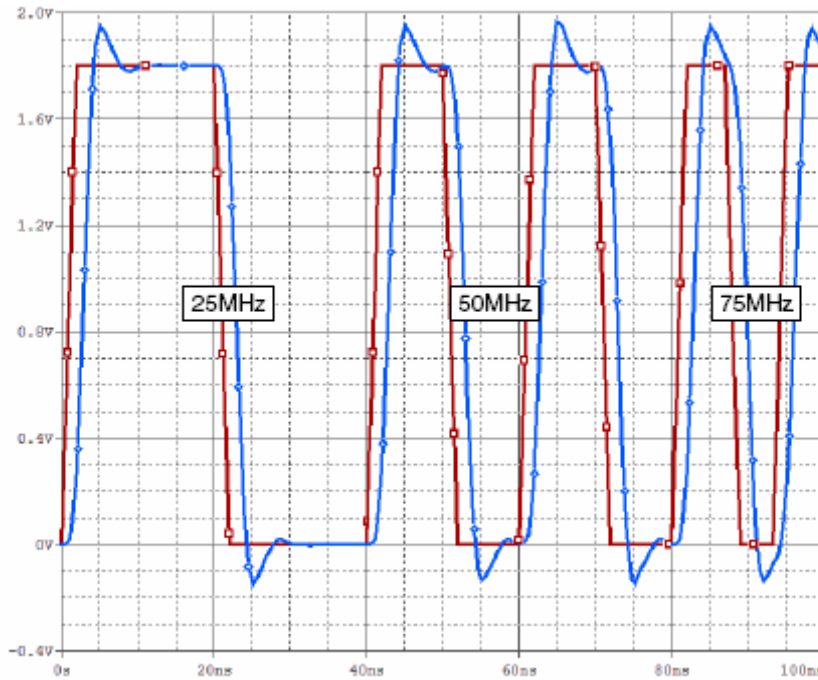


**Figure 8. Simulated Transient Response
(input signal risetime and falltime = 2 ns, clocked at 25, 50 and 75 MHz,
15 Ω Source Resistance, 5 pF Load)**

# CM1451

## APPLICATION INFORMATION

**Table 5. PRINTED CIRCUIT BOARD RECOMMENDATIONS**

| Parameter | Value |
|---|---|
| Pad Size on PCB | 0.240 mm |
| Pad Shape | Round |
| Pad Definition | Non−Solder Mask defined pads |
| Solder Mask Opening | 0.290 mm Round |
| Solder Stencil Thickness | 0.125 – 0.150 mm |
| Solder Stencil Aperture Opening (laser cut, 5% tapered walls) | 0.300 mm Round |
| Solder Flux Ratio | 50/50 by volume |
| Solder Paste Type | No Clean |
| Pad Protective Finish | OSP (Entek Cu Plus 106A) |
| Tolerance − Edge To Corner Ball | ±50 μm |
| Solder Ball Side Coplanarity | ±20 μm |
| Maximum Dwell Time Above Liquidous | 60 seconds |
| Maximum Soldering Temperature for Lead−free Devices using a Lead−free Solder Paste | 260°C |

Non−Solder Mask Defined Pad
0.240 mm DIA.

Solder Stencil Opening
0.300 mm DIA.

Solder Mask Opening
0.290 mm DIA.
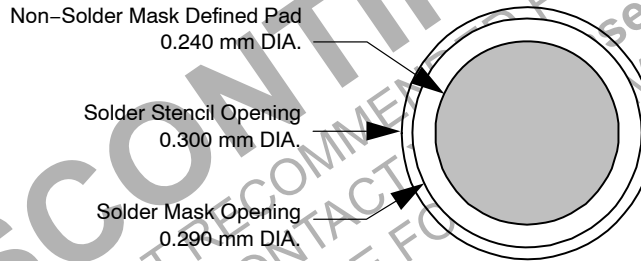
**Figure 9. Recommended Non−Solder Mask Defined Pad Illustration**
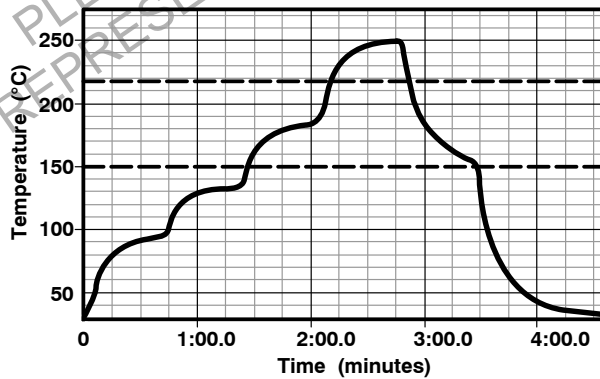
**Figure 10. Lead−free (SnAgCu) Solder Ball Reflow Profile**

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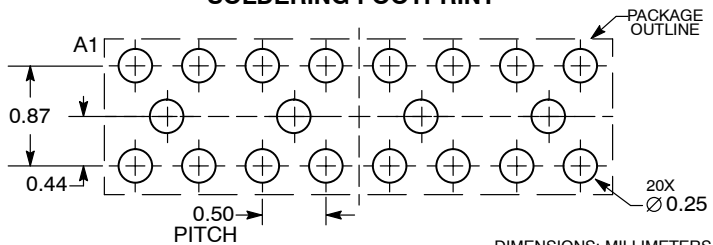
**SCALE 4:1**

**WLCSP15, 3.01x1.38**
CASE 567BT
ISSUE O

DATE 26 JUL 2010
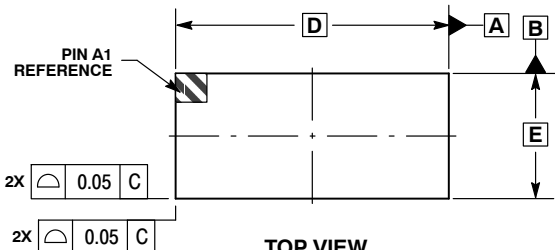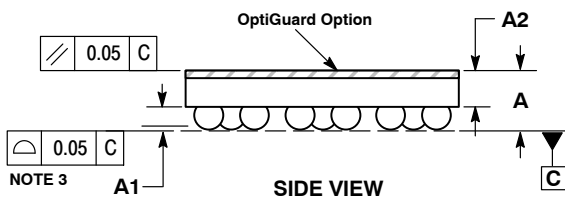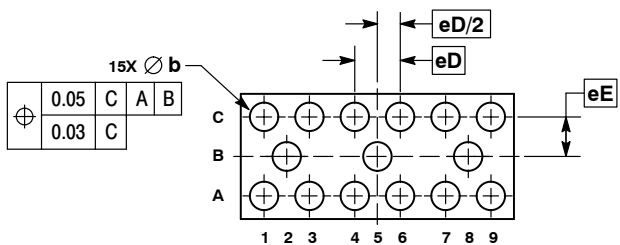
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. COPLANARITY APPLIES TO SPHERICAL CROWNS OF SOLDER BALLS.

| DIM | MILLIMETERS | |
|-----|-----|-----|
| | MIN | MAX |
| A | 0.56 | 0.72 |
| A1 | 0.21 | 0.27 |
| A2 | 0.42 REF | |
| b | 0.29 | 0.35 |
| D | 3.01 BSC | |
| E | 1.38 BSC | |
| eD | 0.50 BSC | |
| eE | 0.435 BSC | |
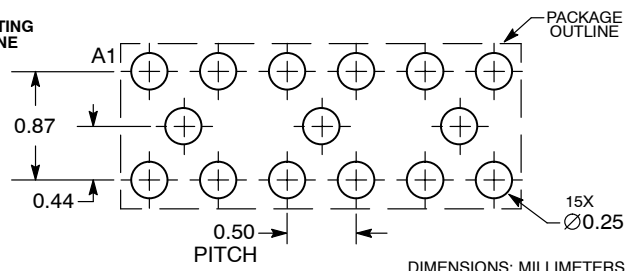
**TOP VIEW**

PIN A1 REFERENCE

2X ⌒ 0.05 C

2X ⌒ 0.05 C

**SIDE VIEW**

OptiGuard Option

∥ 0.05 C

⌒ 0.05 C

NOTE 3

A1

A2

A

C SEATING PLANE

**BOTTOM VIEW**

15X ⌀ b

| ⌖ | 0.05 | C | A | B |
| | 0.03 | C | | |

eD/2

eD

eE

C B A

1 2 3 4 5 6 7 8 9

**RECOMMENDED SOLDERING FOOTPRINT***

A1

0.87

0.44

0.50 PITCH

PACKAGE OUTLINE

15X ⌀0.25

DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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|---|---|---|---|
| DESCRIPTION: | WLCSP15, 3.01X1.38 | | PAGE 1 OF 1 |

**WLCSP20, 4.01x1.38**
CASE 567CL
ISSUE O

DATE 26 JUL 2010
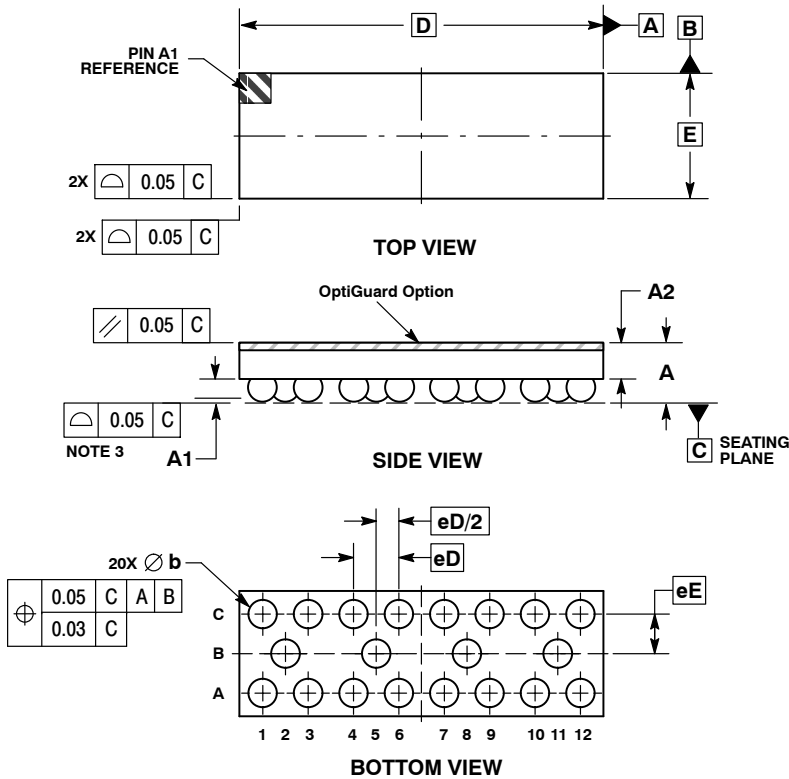
**SCALE 4:1**

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. COPLANARITY APPLIES TO SPHERICAL CROWNS OF SOLDER BALLS.

| DIM | MILLIMETERS | |
| | MIN | MAX |
|---|---|---|
| A | 0.56 | 0.72 |
| A1 | 0.21 | 0.27 |
| A2 | 0.42 REF | |
| b | 0.29 | 0.35 |
| D | 4.01 BSC | |
| E | 1.38 BSC | |
| eD | 0.50 BSC | |
| eE | 0.435 BSC | |

PIN A1 REFERENCE

$D$    $A$ $B$

$E$

2X  0.05  C

2X  0.05  C

**TOP VIEW**

OptiGuard Option

$A2$

0.05  C

$A$

0.05  C

NOTE 3    $A1$

**SIDE VIEW**

$C$  SEATING PLANE

$eD/2$
$eD$

20X  ⌀ $b$

$eE$

0.05  C  A  B
0.03  C

C
B
A

1 2 3  4 5 6  7 8 9  10 11 12

**BOTTOM VIEW**

**RECOMMENDED SOLDERING FOOTPRINT***

A1

PACKAGE OUTLINE

0.87

0.44

0.50 PITCH

20X ⌀ 0.25

DIMENSIONS: MILLIMETERS

*For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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| DESCRIPTION: | WLCSP20, 4.01X1.38 | PAGE 1 OF 1 |

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