P-Channel 20 V (D-S) MOSFET

PRODUCT SUMMARY		
V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A)
- 20	0.0108 at V_{GS} = - 4.5 V	- 15.3
	0.015 at V_{GS} = - 2.5 V	- 13.0
	0.020 at V_{GS} = - 1.8 V	- 11.2

FEATURES

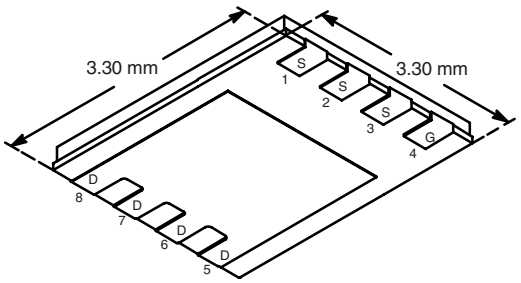
- **Halogen-free According to IEC 61249-2-21 Definition**
- TrenchFET® Power MOSFET: 1.8 V Rated
- Ultra Low On-Resistance for Increased Battery Life
- New PowerPAK® Package
  - Low Thermal Resistance, R_{thJC}
  - Low 1.07 mm Profile
- Compliant to RoHS Directive 2002/95/EC

RoHS COMPLIANT
HALOGEN FREE Available

APPLICATIONS

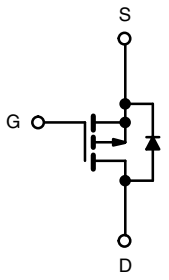
- Load/Power Switching in Portable Devices

PowerPAK 1212-8



Bottom View

Ordering Information: Si7107DN-T1-E3 (Lead (Pb)-free)
Si7107DN-T1-GE3 (Lead (Pb)-free and Halogen-free)



P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS T_A = 25 °C, unless otherwise noted					
Parameter		**Symbol**	**10 s**	**Steady State**	**Unit**
Drain-Source Voltage		V_{DS}	- 20		V
Gate-Source Voltage		V_{GS}	± 8		
Continuous Drain Current (T_J = 150 °C)[a]	T_A = 25 °C	I_D	- 15.3	- 9.8	A
	T_A = 70 °C		- 12.2	- 7.8	
Pulsed Drain Current		I_{DM}	- 40		
Continuous Source Current (Diode Conduction)[a]		I_S	- 3.2	- 1.3	
Maximum Power Dissipation[a]	T_A = 25 °C	P_D	3.8	1.5	W
	T_A = 70 °C		2.4	1.0	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	- 55 to 150		°C
Soldering Recommendations (Peak Temperature)[b, c]			260		

THERMAL RESISTANCE RATINGS					
Parameter		**Symbol**	**Typical**	**Maximum**	**Unit**
Maximum Junction-to-Ambient[a]	t ≤ 10 s	R_{thJA}	24	33	°C/W
	Steady State		65	81	
Maximum Junction-to-Case	Steady State	R_{thJC}	1.9	2.4	

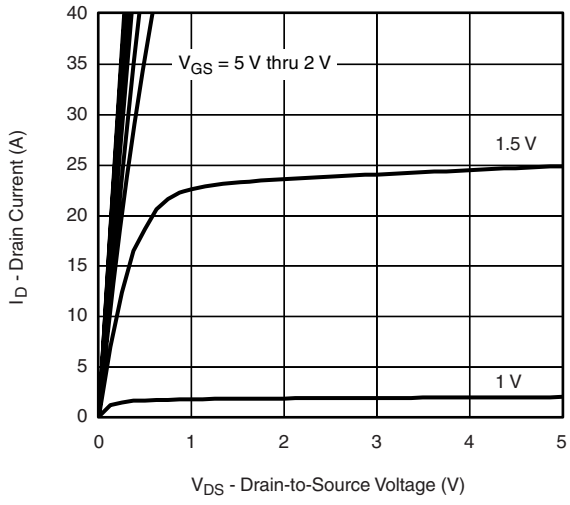
Notes:
a. Surface Mounted on 1" x 1" FR4 board.
b. See Solder Profile (www.vishay.com/ppg?73257). The PowerPAK 1212-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
c. Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.

SPECIFICATIONS T_J = 25 °C, unless otherwise noted						
Parameter	**Symbol**	**Test Conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
Static						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = - 450 µA	- 0.4		- 1.0	V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ± 8 V			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = - 20 V, V_{GS} = 0 V			- 1	µA
		V_{DS} = - 20 V, V_{GS} = 0 V, T_J = 55 °C			- 5	
On-State Drain Current[a]	$I_{D(on)}$	$V_{DS} \leq$ - 5 V, V_{GS} = - 4.5 V	- 40			A
Drain-Source On-State Resistance[a]	$R_{DS(on)}$	V_{GS} = - 4.5 V, I_D = - 15.3 A		0.0090	0.0108	Ω
		V_{GS} = - 2.5 V, I_D = - 13 A		0.0125	0.015	
		V_{GS} = - 1.8 V, I_D = - 5 A		0.0167	0.020	
Forward Transconductance[a]	g_{fs}	V_{DS} = - 15 V, I_D = - 15.3 A		58		S
Diode Forward Voltage[a]	V_{SD}	I_S = - 3.2 A, V_{GS} = 0 V		- 0.7	- 1.2	V
Dynamic[b]						
Total Gate Charge	Q_g	V_{DS} = - 10 V, V_{GS} = - 4.5 V, I_D = - 15.3 A		34	44	nC
Gate-Source Charge	Q_{gs}			4.6		
Gate-Drain Charge	Q_{gd}			9.2		
Gate Resistance	R_g	f = 1 MHz		8		Ω
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = - 10 V, R_L = 10 Ω $I_D \cong$ - 1 A, V_{GEN} = - 4.5 V, R_g = 6 Ω		27	40	ns
Rise Time	t_r			55	85	
Turn-Off Delay Time	$t_{d(off)}$			270	400	
Fall Time	t_f			160	240	
Source-Drain Reverse Recovery Time	t_{rr}	I_F = - 3.2 A, dI/dt = 100 A/µs		110	165	

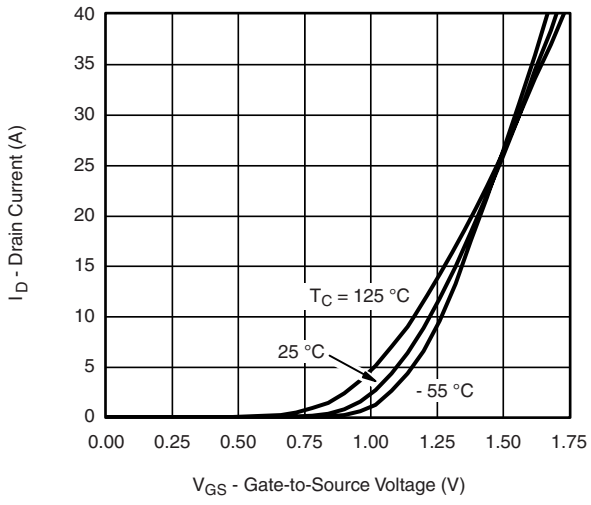
Notes:
a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %.
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

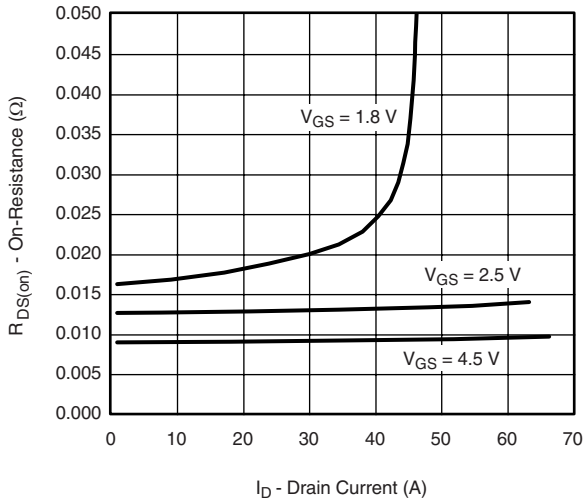


Output Characteristics

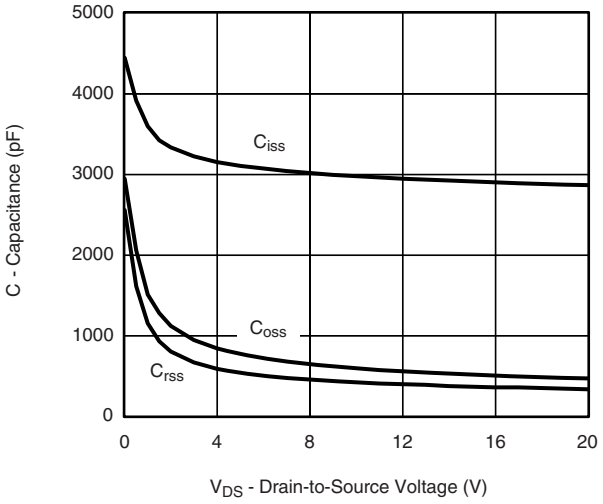


Transfer Characteristics

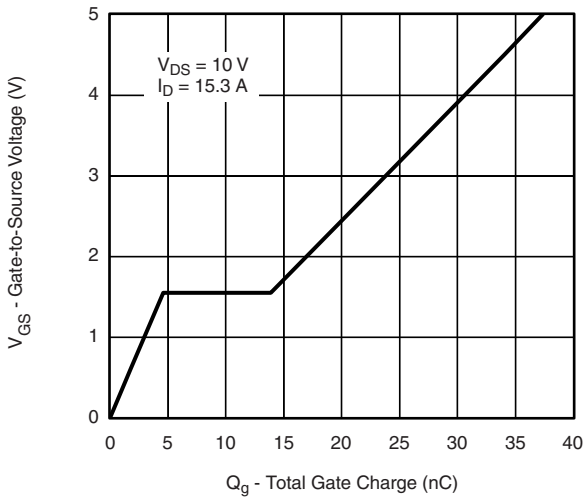
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



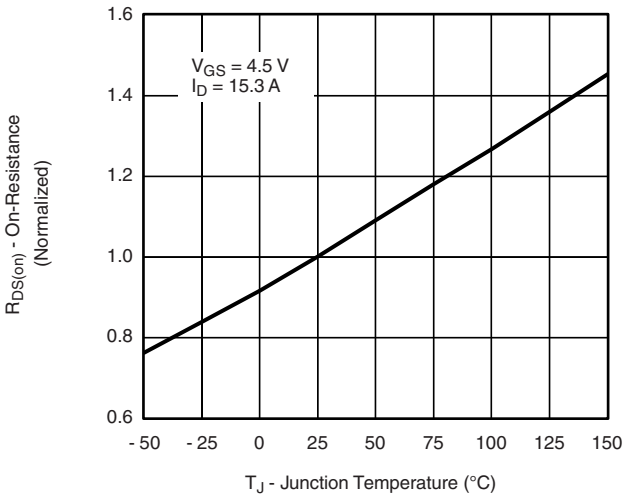
On-Resistance vs. Drain Current



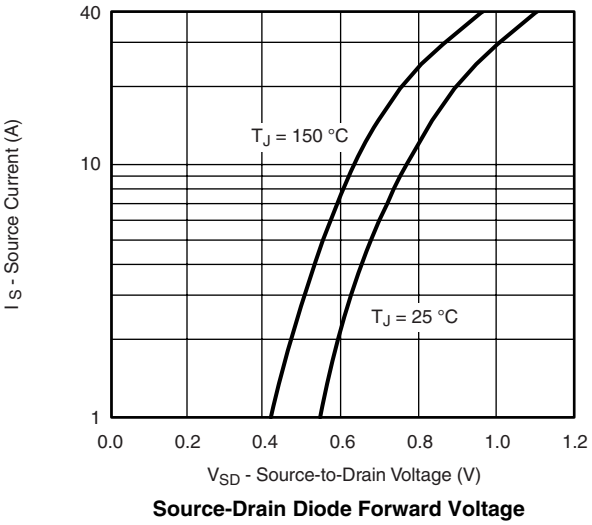
Capacitance



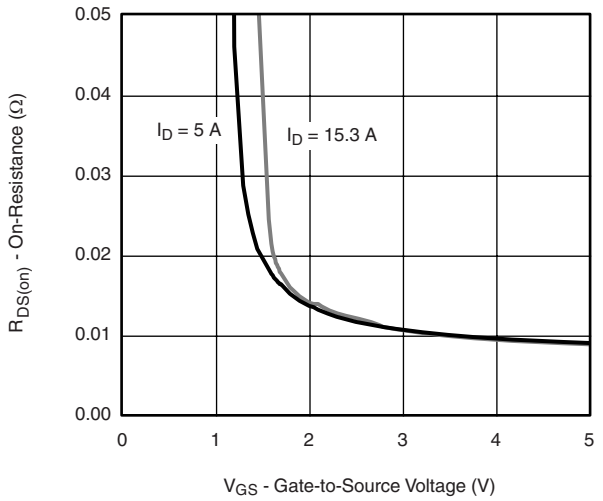
Gate Charge



On-Resistance vs. Junction Temperature

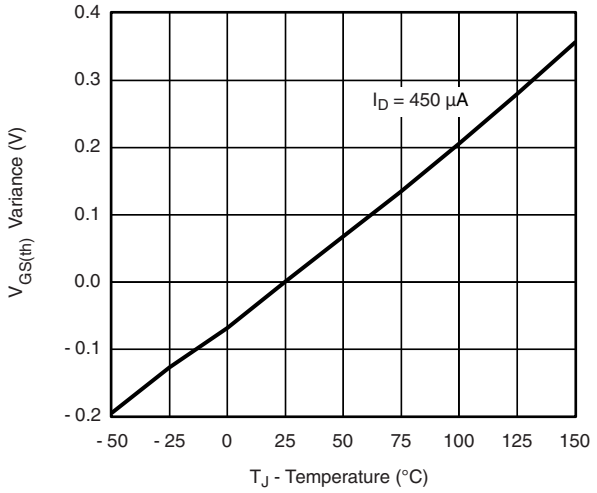


Source-Drain Diode Forward Voltage

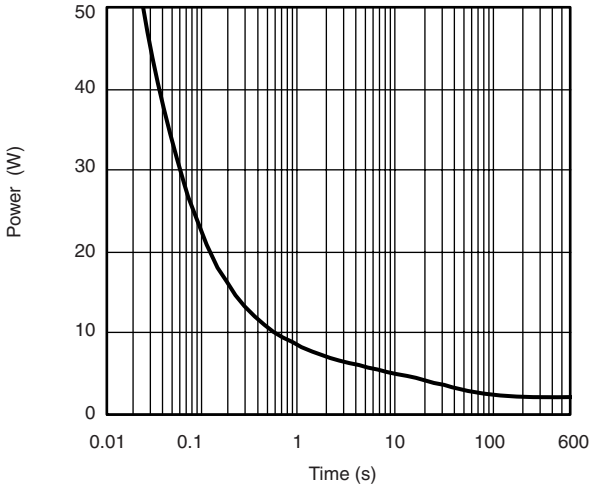


On-Resistance vs. Gate-to-Source Voltage

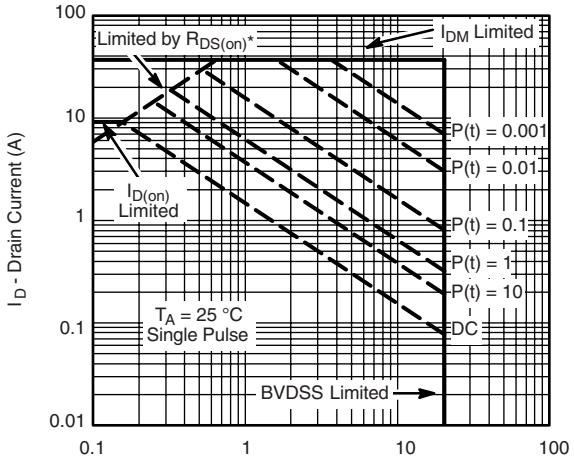
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



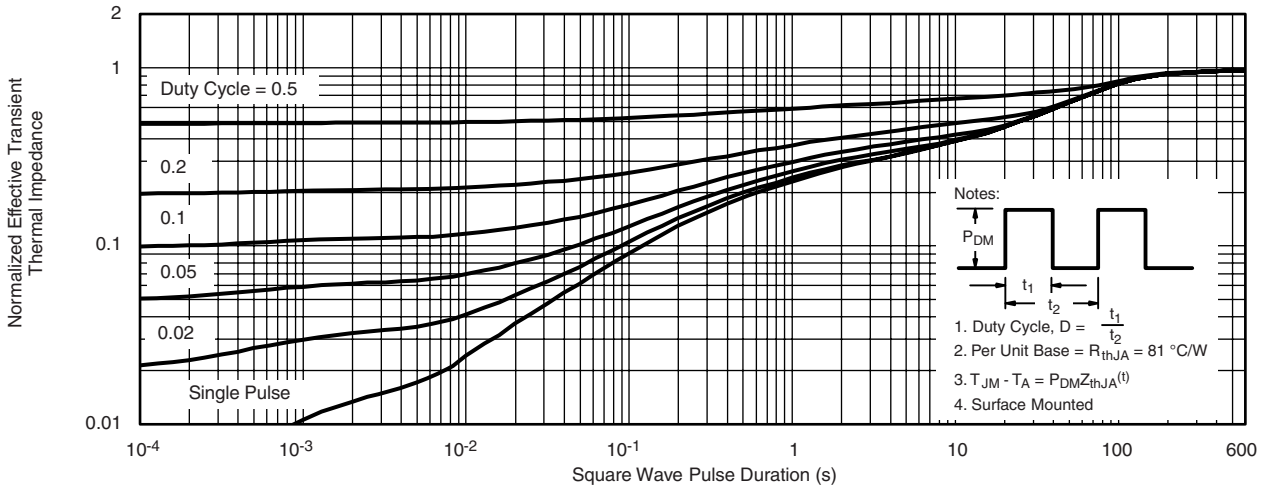
Threshold Voltage



Single Pulse Power, Junction-to-Ambient

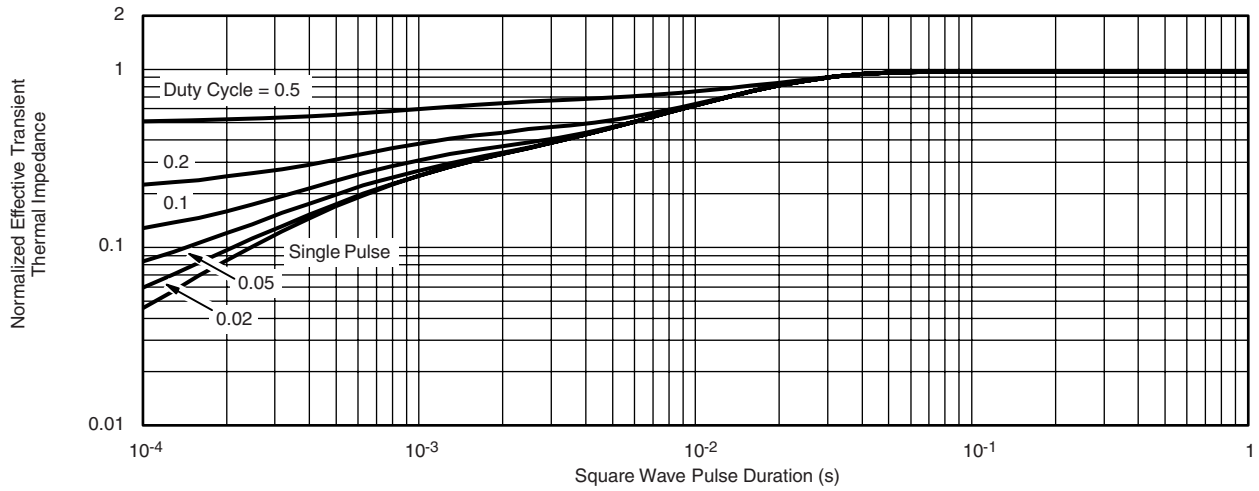


Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Ambient

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Normalized Thermal Transient Impedance, Junction-to-Case

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