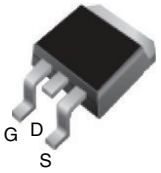
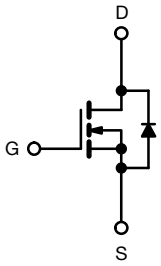
Power MOSFET

D²PAK (TO-263)





N-Channel MOSFET

FEATURES

- Dynamic dV/dt rating
- Repetitive avalanche rated
- Fast switching
- Ease of paralleling
- Simple drive requirements
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

RoHS* Available

HALOGEN FREE Available

Note

* This datasheet provides information about parts that are RoHS-compliant and / or parts that are non RoHS-compliant. For example, parts with lead (Pb) terminations are not RoHS-compliant. Please see the information / tables in this datasheet for details

PRODUCT SUMMARY		
V_{DS} (V)	900	
$R_{DS(on)}$ (Ω)	V_{GS} = 10 V	3.7
Q_g max. (nC)	78	
Q_{gs} (nC)	10	
Q_{gd} (nC)	42	
Configuration	Single	

DESCRIPTION

Third generation MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The D²PAK (TO-263) package is universally preferred for all commercial-industrial applications at power dissipation levels to approximately 50 W. The low thermal resistance and low package cost of the D²PAK (TO-263) contribute to its wide acceptance throughout the industry.

ORDERING INFORMATION		
Package	D²PAK (TO-263)	D²PAK (TO-263)
Lead (Pb)-free and Halogen-free	SiHFBF30S-GE3	-
Lead (Pb)-free	IRFBF30STRLPbF	IRFBF30STRRPbF

ABSOLUTE MAXIMUM RATINGS (T_C = 25 °C, unless otherwise noted)

PARAMETER			SYMBOL	LIMIT	UNIT
Drain-source voltage			V_{DS}	900	V
Gate-source voltage			V_{GS}	± 20	
Continuous drain current	V_{GS} at 10 V	T_C = 25 °C	I_D	3.6	A
		T_C = 100 °C		2.3	
Pulsed drain current [a]			I_{DM}	14	
Linear derating factor				1.0	W/°C
Single pulse avalanche energy [b]			E_{AS}	250	mJ
Repetitive avalanche current [a]			I_{AR}	3.6	A
Repetitive avalanche energy [a]			E_{AR}	13	mJ
Maximum power dissipation	T_C = 25 °C		P_D	125	W
Peak diode recovery dV/dt [c]			dV/dt	1.5	V/ns
Operating junction and storage temperature range			T_J, T_{stg}	-55 to +150	°C
Soldering recommendations (peak temperature) [d]	For 10 s			300	

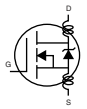
Notes

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
b. V_{DD} = 50 V, starting T_J = 25 °C, L = 36 mH, R_g = 25 Ω, I_{AS} = 3.6 A (see fig. 12)
c. $I_{SD} \leq 3.6$ A, dI/dt ≤ 70 A/μs, $V_{DD} \leq 600$, $T_J \leq 150$ °C
d. 1.6 mm from case

THERMAL RESISTANCE RATINGS				
PARAMETER	**SYMBOL**	**TYP.**	**MAX.**	**UNIT**
Maximum junction-to-ambient	R_{thJA}	-	62	°C/W
Maximum junction-to-ambient (PCB mount) [a]	R_{thJA}	-	40	
Maximum junction-to-case (drain)	R_{thJC}	-	1.0	

Note

a. When mounted on 1" square PCB (FR-4 or G-10 material)

SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)						
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**MIN.**	**TYP.**	**MAX.**	**UNIT**
Static						
Drain-source breakdown voltage	V_{DS}	V_{GS} = 0, I_D = 250 µA	900	-	-	V
V_{DS} temperature coefficient	$\Delta V_{DS}/T_J$	Reference to 25 °C, I_D = 1 mA	-	1.1	-	V/°C
Gate-source threshold voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA	2.0	-	4.0	V
Gate-source leakage	I_{GSS}	V_{GS} = ± 20 V	-	-	± 100	nA
Zero gate voltage drain current	I_{DSS}	V_{DS} = 900 V, V_{GS} = 0 V	-	-	100	µA
		V_{DS} = 720 V, V_{GS} = 0 V, T_J = 125 °C	-	-	500	
Drain-source on-state resistance	$R_{DS(on)}$	V_{GS} = 10 V; I_D = 2.2 A [b]	-	-	3.7	Ω
Forward transconductance	g_{fs}	V_{DS} = 100 V, I_D = 2.2 A [b]	2.3	-	-	S
Dynamic						
Input capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1.0 MHz, see fig. 5	-	1200	-	pF
Output capacitance	C_{oss}		-	320	-	
Reverse transfer capacitance	C_{rss}		-	200	-	
Total gate charge	Q_g	V_{GS} = 10 V; I_D = 3.6 A, V_{DS} = 360 V, see fig. 6 and 13 [b]	-	-	78	nC
Gate-source charge	Q_{gs}		-	-	10	
Gate-drain charge	Q_{gd}		-	-	42	
Turn-on delay time	$t_{d(on)}$	V_{DD} = 450 V, I_D = 3.6 A, R_g = 12 Ω, R_D = 120 Ω, see fig. 10 [b]	-	14	-	ns
Rise time	t_r		-	25	-	
Turn-off delay time	$t_{d(off)}$		-	90	-	
Fall time	t_f		-	30	-	
Gate input resistance	R_g	f = 1 MHz, open drain	0.4	-	2.0	Ω
Internal drain inductance	L_D	Between lead, 6 mm (0.25") from package and center of die contact 	-	4.5	-	nH
Internal source inductance	L_S		-	7.5	-	
Drain-Source Body Diode Characteristics						
Continuous source-drain diode current	I_S	MOSFET symbol showing the integral reverse p - n junction diode 	-	-	3.6	A
Pulsed diode forward current [a]	I_{SM}		-	-	14	
Body diode voltage	V_{SD}	T_J = 25 °C, I_S = 3.6 A, V_{GS} = 0 V [b]	-	-	1.8	V
Body diode reverse recovery time	t_{rr}	T_J = 25 °C, I_F = 3.6 A, dI/dt = 100 A/µs [b]	-	430	650	ns
Body diode reverse recovery charge	Q_{rr}		-	1.4	2.1	µC
Forward turn-on time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L_S and L_D)				

Notes

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)

b. Pulse width ≤ 300 µs; duty cycle ≤ 2 %

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

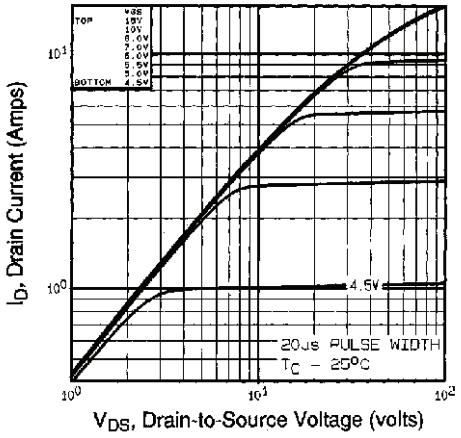


Fig. 1 - Typical Output Characteristics, T_C = 25 °C

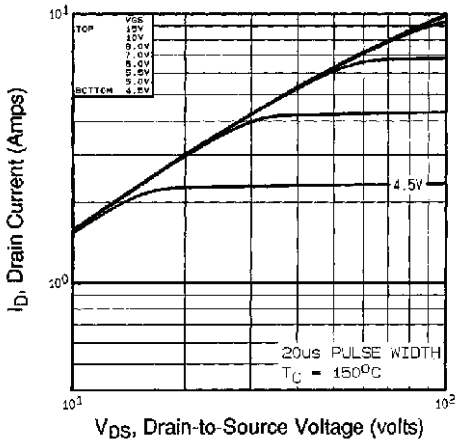


Fig. 2 - Typical Output Characteristics, T_C = 150 °C

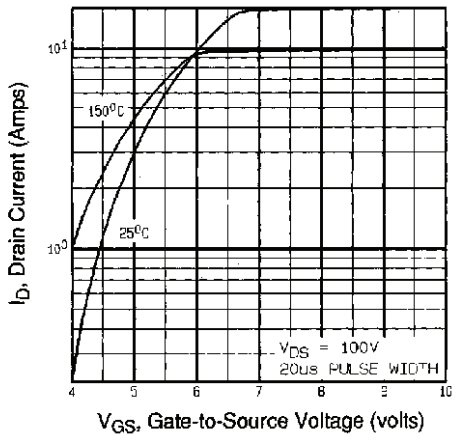


Fig. 3 - Typical Transfer Characteristics

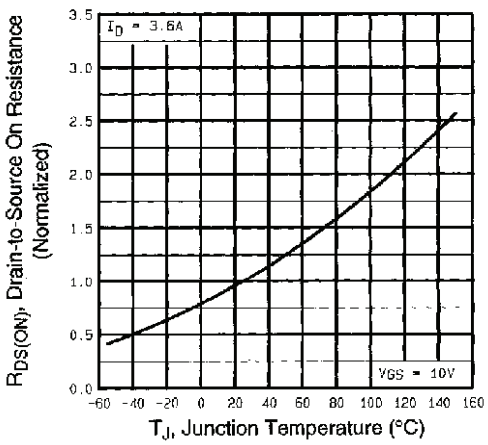


Fig. 4 - Normalized On-Resistance vs. Temperature

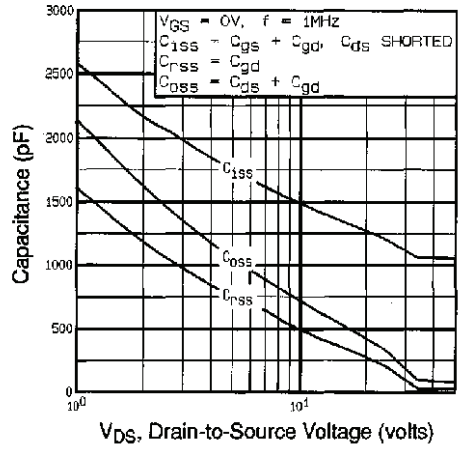


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

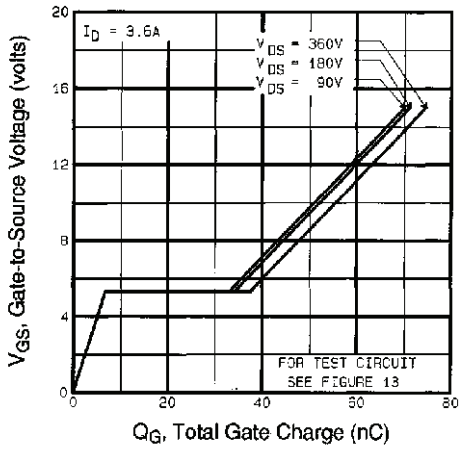


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

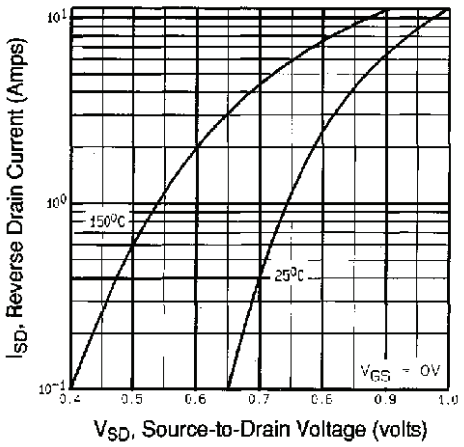


Fig. 7 - Typical Source-Drain Diode Forward Voltage

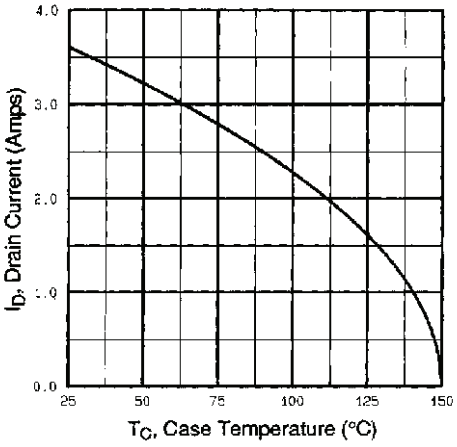


Fig. 9 - Maximum Drain Current vs. Case Temperature

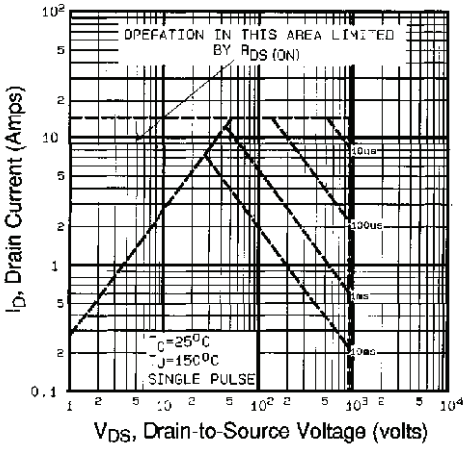


Fig. 8 - Maximum Safe Operating Area

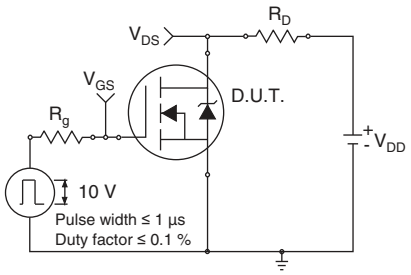


Fig. 10 - Switching Time Test Circuit

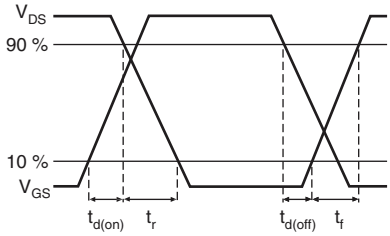


Fig. 11 - Switching Time Waveforms

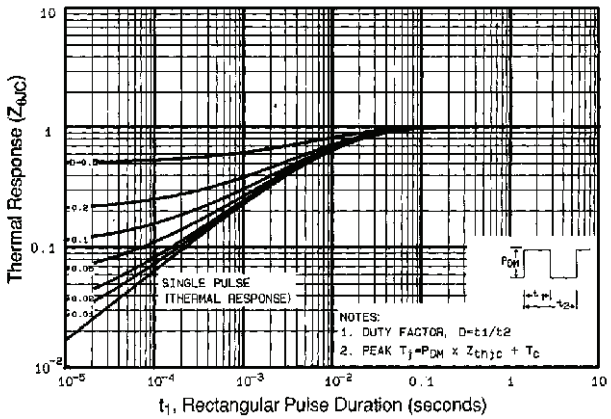


Fig. 12 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

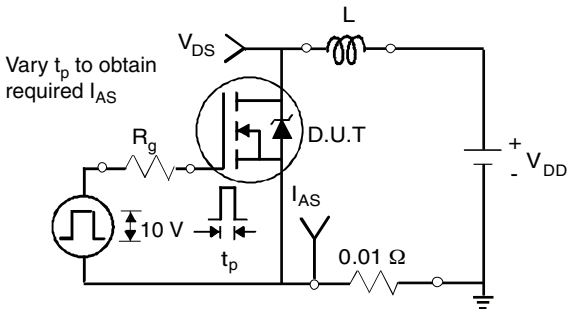


Fig. 13 - Unclamped Inductive Test Circuit

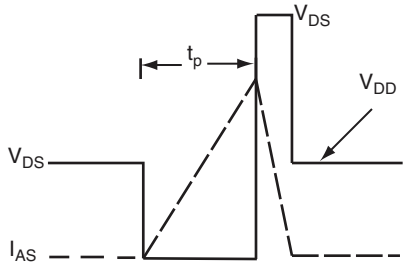


Fig. 14 - Unclamped Inductive Waveforms

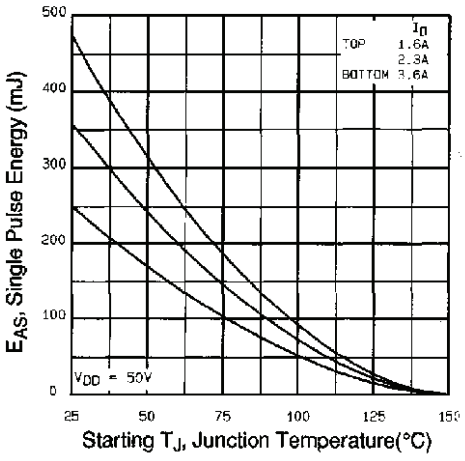


Fig. 15 - Maximum Avalanche Energy vs. Drain Current

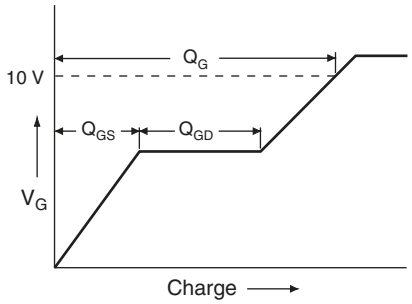


Fig. 16 - Basic Gate Charge Waveform

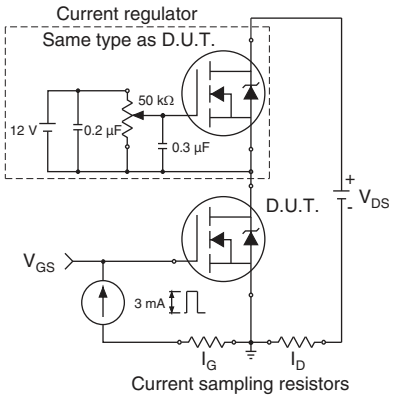
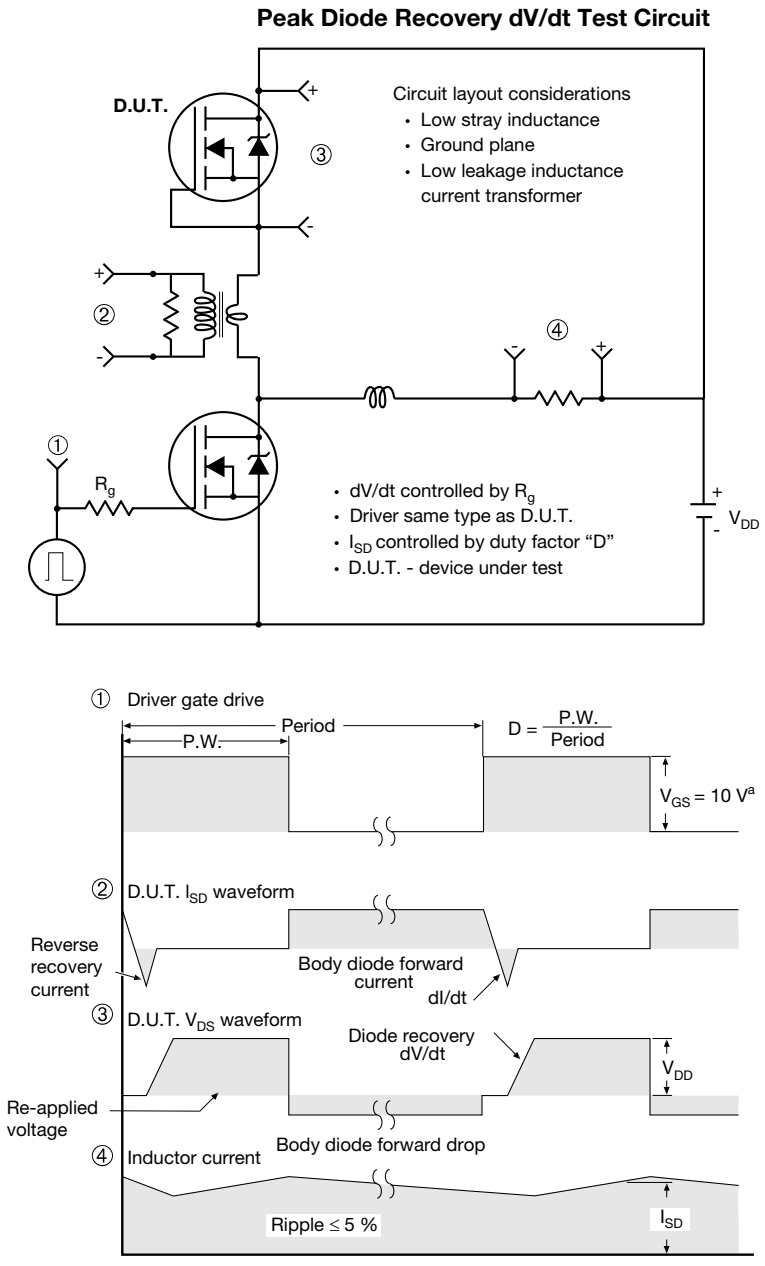


Fig. 17 - Gate Charge Test Circuit

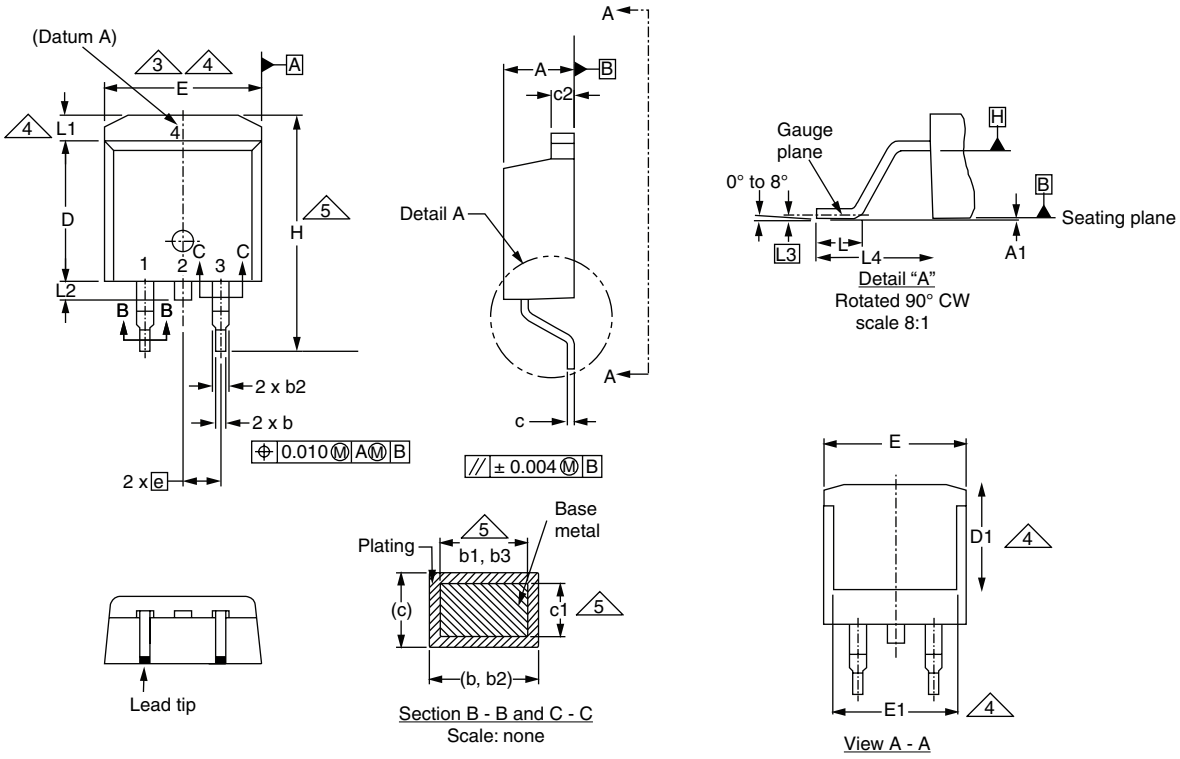


Note

a. V_{GS} = 5 V for logic level devices

Fig. 18 - For N-Channel

TO-263AB (HIGH VOLTAGE)



	MILLIMETERS		INCHES	
DIM.	MIN.	MAX.	MIN.	MAX.
A	4.06	4.83	0.160	0.190
A1	0.00	0.25	0.000	0.010
b	0.51	0.99	0.020	0.039
b1	0.51	0.89	0.020	0.035
b2	1.14	1.78	0.045	0.070
b3	1.14	1.73	0.045	0.068
c	0.38	0.74	0.015	0.029
c1	0.38	0.58	0.015	0.023
c2	1.14	1.65	0.045	0.065
D	8.38	9.65	0.330	0.380

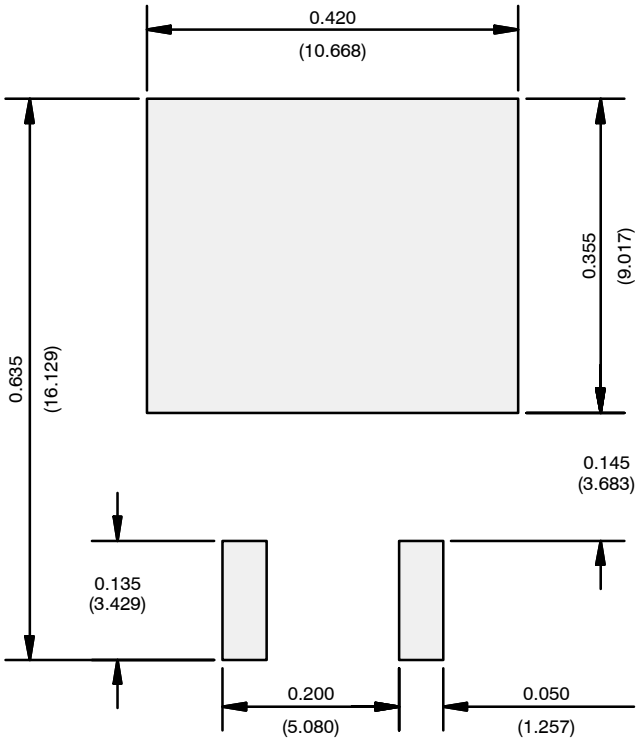
	MILLIMETERS		INCHES	
DIM.	MIN.	MAX.	MIN.	MAX.
D1	6.86	-	0.270	-
E	9.65	10.67	0.380	0.420
E1	6.22	-	0.245	-
e	2.54 BSC		0.100 BSC	
H	14.61	15.88	0.575	0.625
L	1.78	2.79	0.070	0.110
L1	-	1.65	-	0.066
L2	-	1.78	-	0.070
L3	0.25 BSC		0.010 BSC	
L4	4.78	5.28	0.188	0.208

ECN: S-82110-Rev. A, 15-Sep-08
DWG: 5970

Notes

1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Dimensions are shown in millimeters (inches).
3. Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outmost extremes of the plastic body at datum A.
4. Thermal PAD contour optional within dimension E, L1, D1 and E1.
5. Dimension b1 and c1 apply to base metal only.
6. Datum A and B to be determined at datum plane H.
7. Outline conforms to JEDEC outline to TO-263AB.

RECOMMENDED MINIMUM PADS FOR D²PAK: 3-Lead



Recommended Minimum Pads
Dimensions in Inches/(mm)

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