IRF840LCS, IRF840LCL, SiHF840LCS, SiHF840LCL

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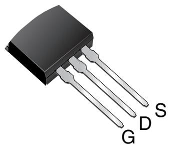
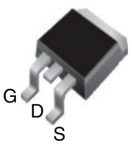
Vishay Siliconix

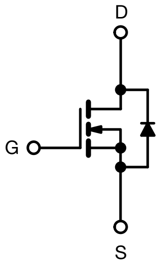
Power MOSFET

I^{2}PAK (TO-262)



D^{2}PAK (TO-263)





N-Channel MOSFET

PRODUCT SUMMARY		
V_{DS} (V)	500	
$R_{DS(on)}$ (Ω)	V_{GS} = 10 V	0.85
Q_g max. (nC)	39	
Q_{gs} (nC)	10	
Q_{gd} (nC)	19	
Configuration	Single	

FEATURES

- Ultra low gate charge
- Reduced gate drive requirement
- Enhanced 30 V V_{GS} rating
- Reduced C_{iss}, C_{oss}, C_{rss}
- Extremely high frequency operation
- Repetitive avalanche rated
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

RoHS*
Available

HALOGEN
FREE
Available

Note

* This datasheet provides information about parts that are RoHS-compliant and / or parts that are non RoHS-compliant. For example, parts with lead (Pb) terminations are not RoHS-compliant. Please see the information / tables in this datasheet for details

DESCRIPTION

This series of low charge power MOSFETs achieve significantly lower gate charge then conventional Power MOSFETs. Utilizing the new LCDMOS (low charge device Power MOSFETs) technology, the device improvements are achieved without added product cost, allowing for reduced gate drive requirements and total system savings. In addition, reduced switching losses and improved efficiency are achievable in a variety of high frequency applications. Frequencies of a few MHz at high current are possible using the new low charge Power MOSFETs.

These device improvements combined with the proven ruggedness and reliability that characterize Power MOSFETs offer the designer a new power transistor standard for switching applications.

ORDERING INFORMATION		
Package	D^{2}PAK (TO-263)	I^{2}PAK (TO-262)
Lead (Pb)-free and Halogen-free	SiHF840LCS-GE3	SiHF840LCL-GE3
Lead (Pb)-free	IRF840LCSPbF	IRF840LCLPbF
	IRF840LCSTRRPBF	-

Note

a. See device orientation.

ABSOLUTE MAXIMUM RATINGS (T_C = 25 °C, unless otherwise noted)					
PARAMETER			**SYMBOL**	**LIMIT**	**UNIT**
Drain-Source Voltage			V_{DS}	500	V
Gate-Source Voltage			V_{GS}	± 30	
Continuous Drain Current	V_{GS} at 10 V	T_C = 25 °C	I_D	8.0	A
		T_C = 100 °C		5.1	
Pulsed Drain Current [a, e]			I_{DM}	28	
Linear Derating Factor				1.0	W/°C
Single Pulse Avalanche Energy [b, e]			E_{AS}	510	mJ
Avalanche Current [a]			I_{AR}	8.0	A
Repetitive Avalanche Energy [a]			E_{AR}	13	mJ
Maximum Power Dissipation	T_C = 25 °C		P_D	125	W
	T_A = 25 °C			3.1	
Peak Diode Recovery dV/dt [c, e]			dV/dt	3.5	V/ns
Operating Junction and Storage Temperature Range			T_J, T_{stg}	-55 to +150	°C
Soldering Recommendations (Peak temperature) [d]	For 10 s			300	

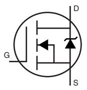
Notes

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
b. Starting T_J = 25 °C, L = 14 mH, R_g = 25 Ω, I_{AS} = 8.0 A (see fig. 12)
c. $I_{SD} \leq 8.0$ A, dI/dt ≤ 100 A/μs, $V_{DD} \leq V_{DS}$, $T_J \leq 150$ °C
d. 1.6 mm from case
e. Uses IRF840LC, SiHF840LC data and test conditions

THERMAL RESISTANCE RATINGS				
PARAMETER	**SYMBOL**	**TYP.**	**MAX.**	**UNIT**
Maximum Junction-to-Ambient (PCB mounted, steady-state) [a]	R_{thJA}	-	40	°C/W
Maximum Junction-to-Case (Drain)	R_{thJC}	-	1.0	

Note

a. When mounted on 1" square PCB (FR-4 or G-10 material)

SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)						
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**MIN.**	**TYP.**	**MAX.**	**UNIT**
Static						
Drain-Source Breakdown Voltage	V_{DS}	V_{GS} = 0, I_D = 250 μA	500	-	-	V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to 25 °C, I_D = 1 mA [c]	-	0.63	-	V/°C
Gate-Source Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 μA	2.0	-	4.0	V
Gate-Source Leakage	I_{GSS}	V_{GS} = ± 20 V	-	-	± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 500 V, V_{GS} = 0 V	-	-	25	μA
		V_{DS} = 400 V, V_{GS} = 0 V, T_J = 125 °C	-	-	250	
Drain-Source On-State Resistance	$R_{DS(on)}$	V_{GS} = 10 V I_D = 4.8 A [b]	-	-	0.85	Ω
Forward Transconductance	g_{fs}	V_{DS} = 50 V, I_D = 4.8 A [b]	4.0	-	-	S
Dynamic						
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1.0 MHz, see fig. 5 [c]	-	1100	-	pF
Output Capacitance	C_{oss}		-	170	-	
Reverse Transfer Capacitance	C_{rss}		-	18	-	
Total Gate Charge	Q_g	V_{GS} = 10 V I_D = 8.0 A, V_{DS} = 400 V, see fig. 6 and 13 [b, c]	-	-	39	nC
Gate-Source Charge	Q_{gs}		-	-	10	
Gate-Drain Charge	Q_{gd}		-	-	19	
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 250 V, I_D = 8.0 A, R_g = 9.1 Ω, R_D = 30 Ω, see fig. 10 [b, c]	-	12	-	ns
Rise Time	t_r		-	25	-	
Turn-Off Delay Time	$t_{d(off)}$		-	27	-	
Fall Time	t_f		-	19	-	
Gate Input Resistance	R_g	f = 1 MHz, open drain	0.7	-	3.7	Ω
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	MOSFET symbol showing the integral reverse p - n junction diode 	-	-	8.0	A
Pulsed Diode Forward Current [a]	I_{SM}		-	-	28	
Body Diode Voltage	V_{SD}	T_J = 25 °C, I_S = 8.0 A, V_{GS} = 0 V [b]	-	-	2.0	V
Body Diode Reverse Recovery Time	t_{rr}	T_J = 25 °C, I_F = 8.0 A, dI/dt = 100 A/μs [b, c]	-	490	740	ns
Body Diode Reverse Recovery Charge	Q_{rr}		-	3.0	4.5	μC
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L_S and L_D)				

Notes

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
b. Pulse width ≤ 300 μs; duty cycle ≤ 2 %
c. Uses SiHF840LC data and test conditions

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

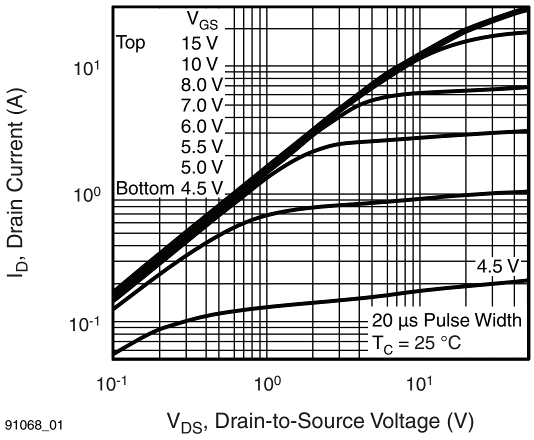


Fig. 1 - Typical Output Characteristics

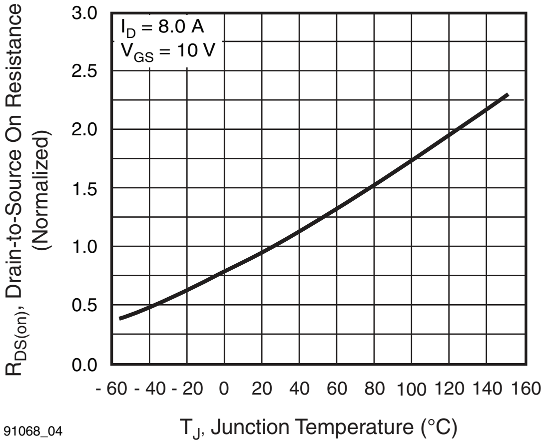


Fig. 4 - Normalized On-Resistance vs. Temperature

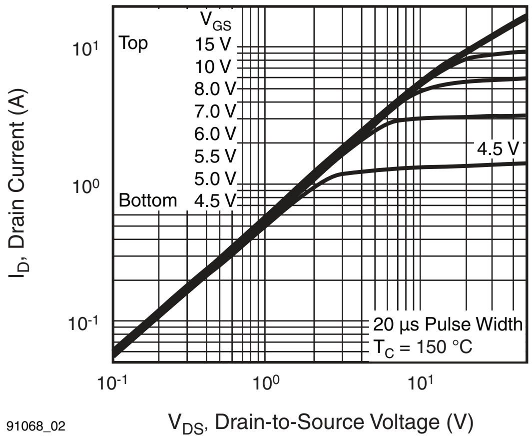


Fig. 2 - Typical Output Characteristics

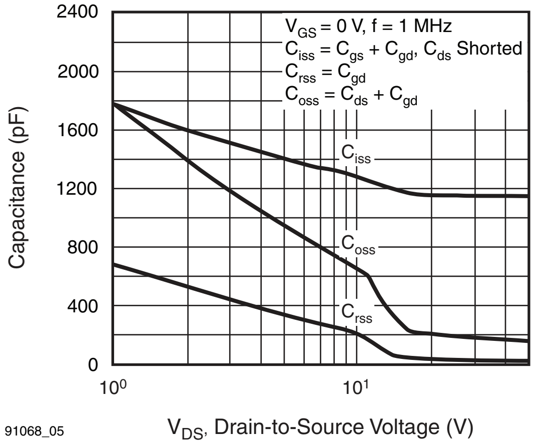


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

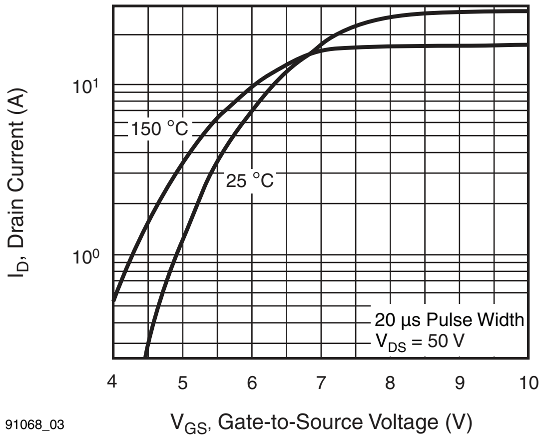


Fig. 3 - Typical Transfer Characteristics

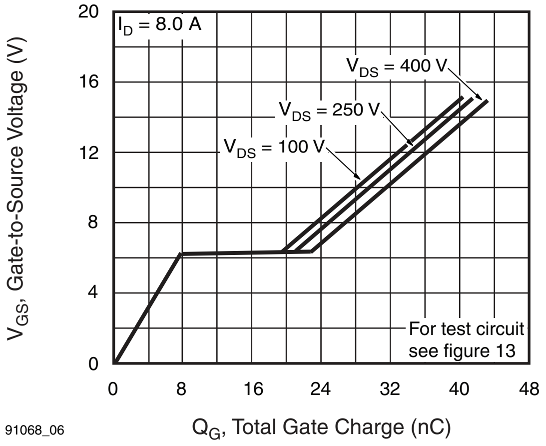


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

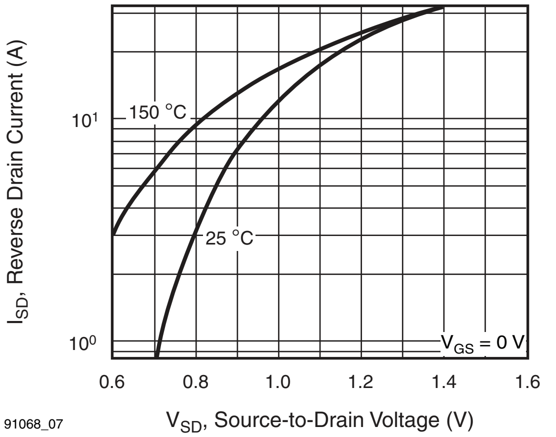


Fig. 7 - Typical Source-Drain Diode Forward Voltage

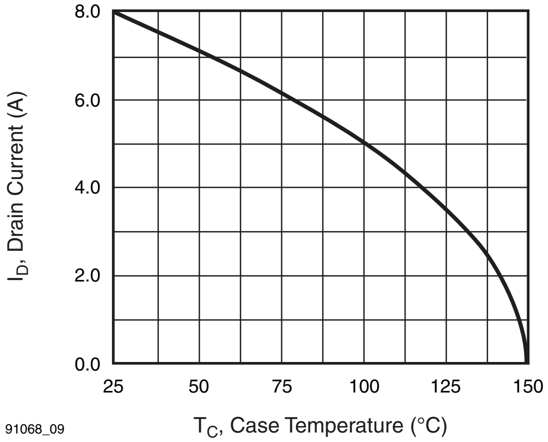


Fig. 9 - Maximum Drain Current vs. Case Temperature

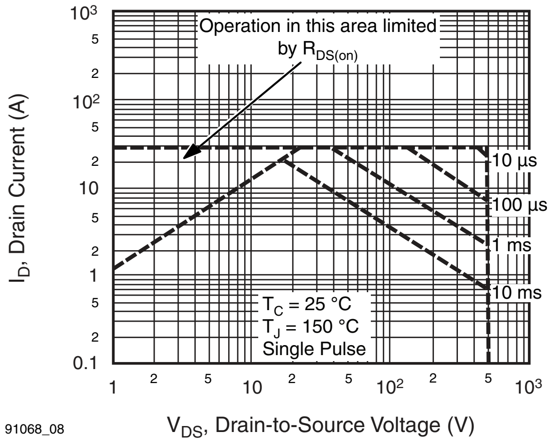


Fig. 8 - Maximum Safe Operating Area

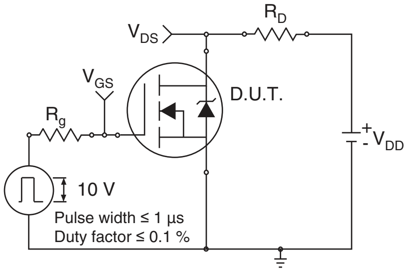


Fig. 10a - Switching Time Test Circuit

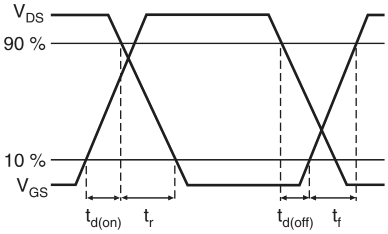


Fig. 10b - Switching Time Waveforms

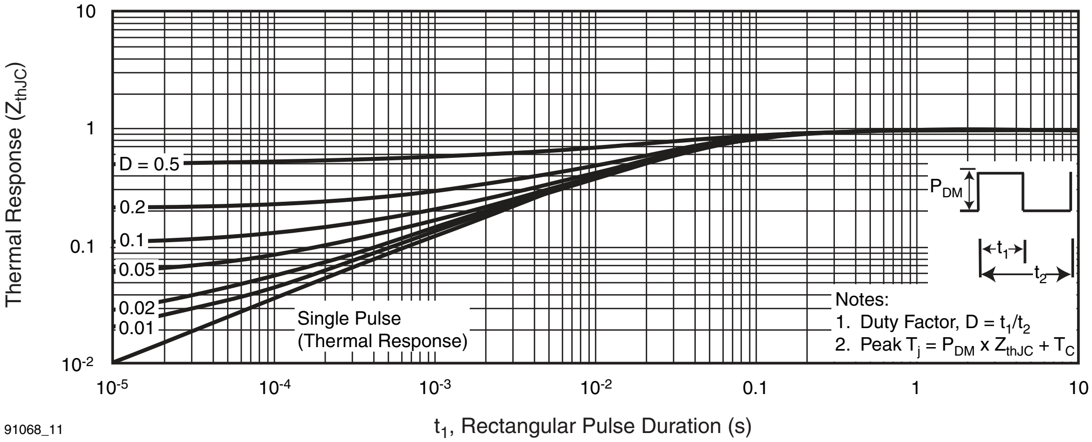


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

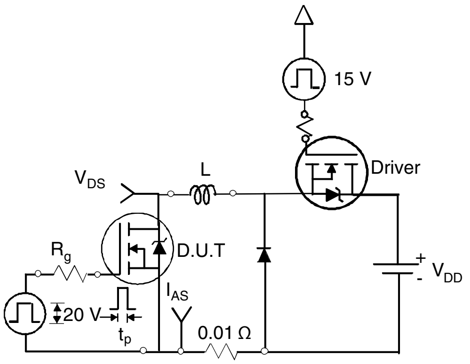


Fig. 12a - Unclamped Inductive Test Circuit

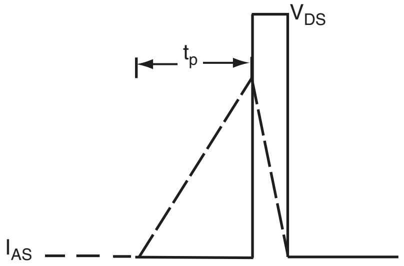


Fig. 12b - Unclamped Inductive Waveforms

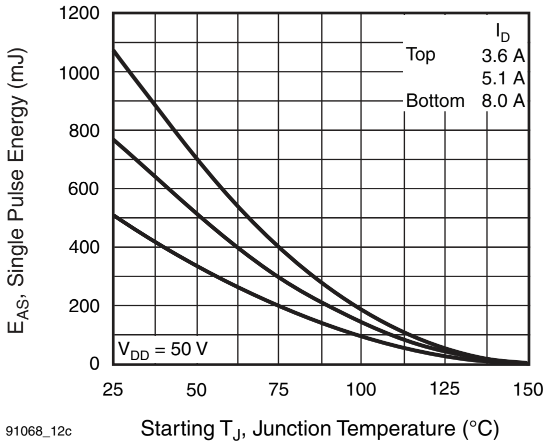


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

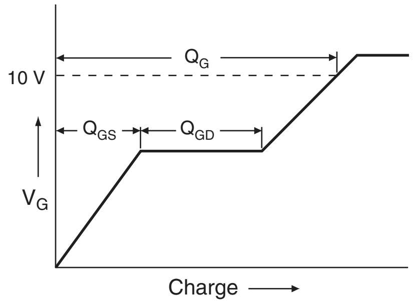


Fig. 13a - Basic Gate Charge Waveform

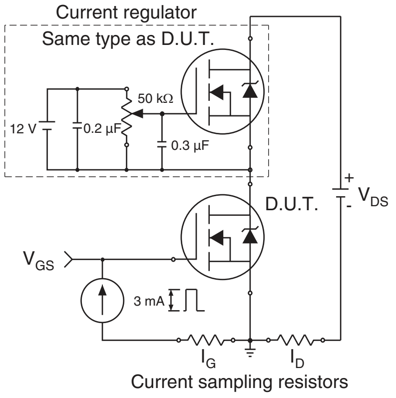
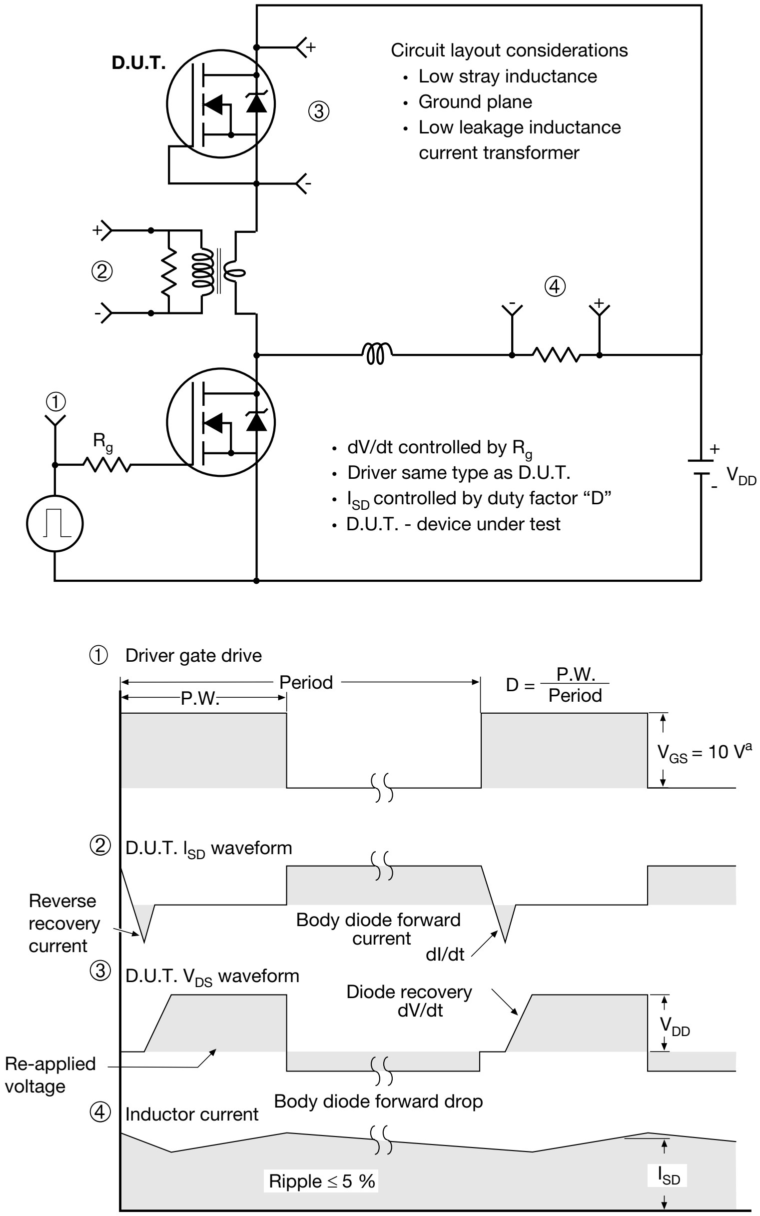


Fig. 13b - Gate Charge Test Circuit

Peak Diode Recovery dV/dt Test Circuit



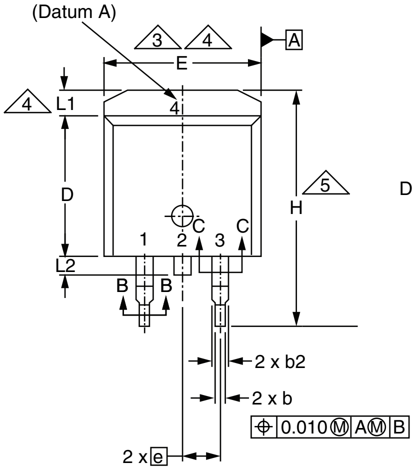
Note

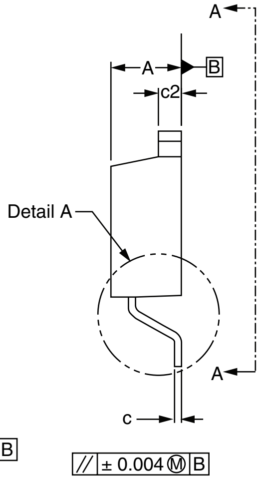
a. V_{GS} = 5 V for logic level devices

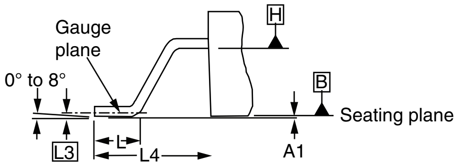
Fig. 14 - For N-Channel

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?91068.

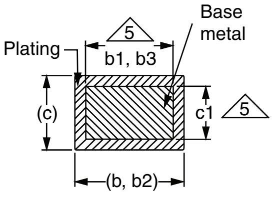
TO-263AB (HIGH VOLTAGE)







Detail "A"
Rotated 90° CW
scale 8:1



Section B - B and C - C
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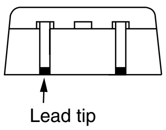
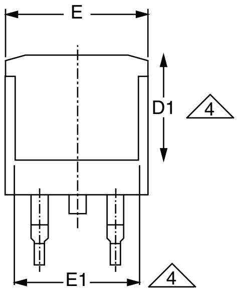




View A - A

	MILLIMETERS		INCHES	
DIM.	MIN.	MAX.	MIN.	MAX.
A	4.06	4.83	0.160	0.190
A1	0.00	0.25	0.000	0.010
b	0.51	0.99	0.020	0.039
b1	0.51	0.89	0.020	0.035
b2	1.14	1.78	0.045	0.070
b3	1.14	1.73	0.045	0.068
c	0.38	0.74	0.015	0.029
c1	0.38	0.58	0.015	0.023
c2	1.14	1.65	0.045	0.065
D	8.38	9.65	0.330	0.380

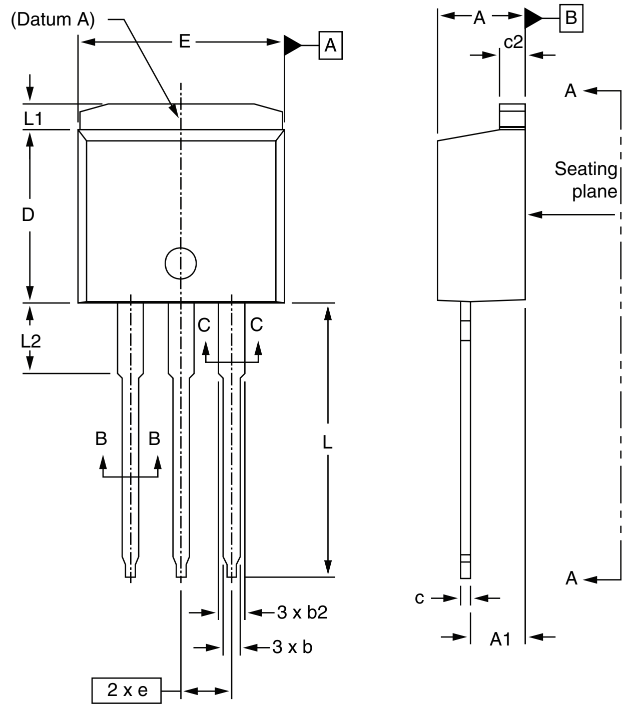
	MILLIMETERS		INCHES	
DIM.	MIN.	MAX.	MIN.	MAX.
D1	6.86	-	0.270	-
E	9.65	10.67	0.380	0.420
E1	6.22	-	0.245	-
e	2.54 BSC		0.100 BSC	
H	14.61	15.88	0.575	0.625
L	1.78	2.79	0.070	0.110
L1	-	1.65	-	0.066
L2	-	1.78	-	0.070
L3	0.25 BSC		0.010 BSC	
L4	4.78	5.28	0.188	0.208

ECN: S-82110-Rev. A, 15-Sep-08
DWG: 5970

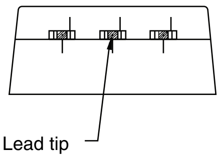
Notes

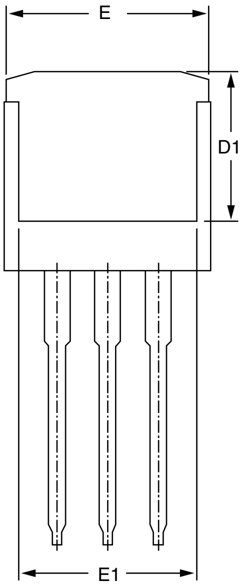
1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Dimensions are shown in millimeters (inches).
3. Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outmost extremes of the plastic body at datum A.
4. Thermal PAD contour optional within dimension E, L1, D1 and E1.
5. Dimension b1 and c1 apply to base metal only.
6. Datum A and B to be determined at datum plane H.
7. Outline conforms to JEDEC outline to TO-263AB.

I^2PAK (TO-262) (HIGH VOLTAGE)

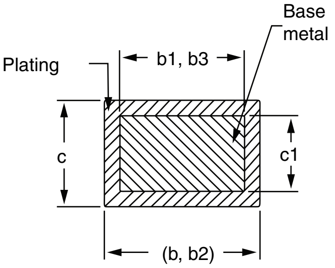


⌖ 0.010 Ⓜ A Ⓜ B





Section A - A



Section B - B and C - C
Scale: None

	MILLIMETERS		INCHES	
DIM.	MIN.	MAX.	MIN.	MAX.
A	4.06	4.83	0.160	0.190
A1	2.03	3.02	0.080	0.119
b	0.51	0.99	0.020	0.039
b1	0.51	0.89	0.020	0.035
b2	1.14	1.78	0.045	0.070
b3	1.14	1.73	0.045	0.068
c	0.38	0.74	0.015	0.029
c1	0.38	0.58	0.015	0.023
c2	1.14	1.65	0.045	0.065

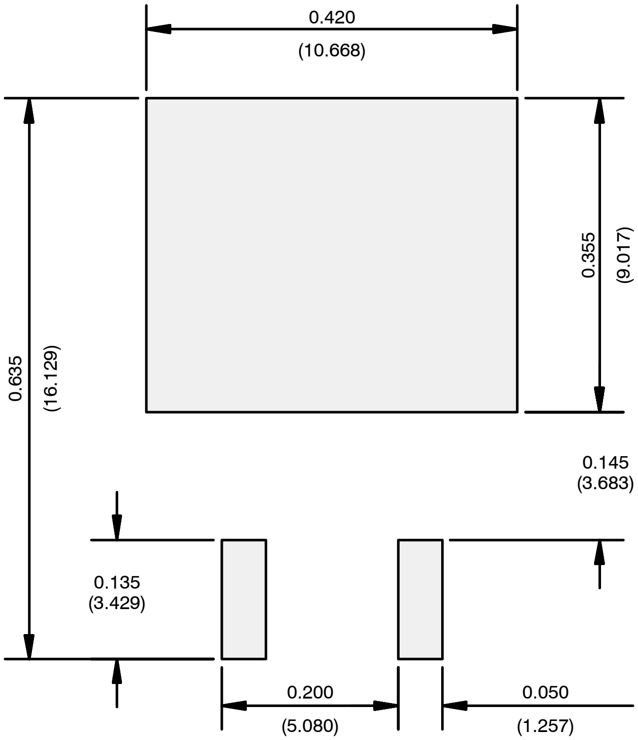
	MILLIMETERS		INCHES	
DIM.	MIN.	MAX.	MIN.	MAX.
D	8.38	9.65	0.330	0.380
D1	6.86	-	0.270	-
E	9.65	10.67	0.380	0.420
E1	6.22	-	0.245	-
e	2.54 BSC		0.100 BSC	
L	13.46	14.10	0.530	0.555
L1	-	1.65	-	0.065
L2	3.56	3.71	0.140	0.146

ECN: S-82442-Rev. A, 27-Oct-08
DWG: 5977

Notes

1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm per side. These dimensions are measured at the outmost extremes of the plastic body.
3. Thermal pad contour optional within dimension E, L1, D1, and E1.
4. Dimension b1 and c1 apply to base metal only.

RECOMMENDED MINIMUM PADS FOR D^{2}PAK: 3-Lead



Recommended Minimum Pads
Dimensions in Inches/(mm)

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