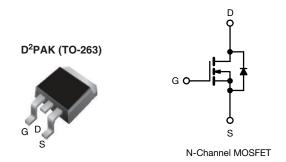
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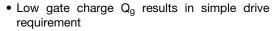
Vishay Siliconix

Power MOSFET



PRODUCT SUMMARY						
V _{DS} (V)	600	600				
R _{DS(on)} (Ω)	V _{GS} = 10 V	V _{GS} = 10 V 0.75				
Q _g max. (nC)	49	49				
Q _{gs} (nC)	13	13				
Q _{gd} (nC)	20					
Configuration	Single					

FEATURES





FREE

- Improved gate, avalanche and dynamic dV/dt ruggedness
- Fully characterized capacitance and avalanche voltage and current
- Material categorization: for definitions of compliance please see <u>www.vishay.com/doc?99912</u>

Note

* This datasheet provides information about parts that are RoHS-compliant and / or parts that are non RoHS-compliant. For example, parts with lead (Pb) terminations are not RoHS-compliant. Please see the information / tables in this datasheet for details

APPLICATIONS

- Switch mode power supply (SMPS)
- Uninterruptible power supply
- High speed power switching

APPLICABLE OFF LINE SMPS TOPOLOGIES

- · Active clamped forward
- · Main switch

ORDERING INFORMATION					
Package	D ² PAK (TO-263)	D ² PAK (TO-263)	D ² PAK (TO-263)		
Lead (Pb)-free and Halogen-free	SiHFS9N60A-GE3	SiHFS9N60ATRR-GE3 a	SiHFS9N60ATRL-GE3 a		
Lead (Pb)-free	IRFS9N60APbF	IRFS9N60ATRRPbF a	IRFS9N60ATRLPbF a		

Note

a. See device orientation

ABSOLUTE MAXIMUM RATINGS (TC	= 25 °C, unl	ess otherwis	se noted)			
PARAMETER			SYMBOL	LIMIT	UNIT	
Drain-Source Voltage			V _{DS}	600	.,	
Gate-Source Voltage			V _{GS}	± 30	V	
$T_{\rm C} = 25 ^{\circ}{\rm C}$,	9.2		
Continuous Drain Current	V _{GS} at 10 V	$T_C = 25 ^{\circ}C$ $T_C = 100 ^{\circ}C$	- I _D	5.8	Α	
Pulsed Drain Current ^a	I _{DM}	37				
Linear Derating Factor				1.3	W/°C	
Single Pulse Avalanche Energy ^b			E _{AS}	290	mJ	
Repetitive Avalanche Current ^a			I _{AR}	9.2	А	
Repetitive Avalanche Energy ^a			E _{AR}	17	mJ	
Maximum Power Dissipation T _C = 25 °C			P _D	170	W	
Peak Diode Recovery dV/dt ^c			dV/dt	5.0	V/ns	
Operating Junction and Storage Temperature Range			T _J , T _{stg}	-55 to +150	- °C	
Soldering Recommendations (Peak temperature) d for 10 s				300		

Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
- b. Starting T_J = 25 °C, L = 6.8 mH, R_g = 25 $\Omega,\,I_{AS}$ = 9.2 A (see fig. 12)
- c. $I_{SD} \le 9.2$ A, $dI/dt \le 50$ A/ μ s, $V_{DD} \le V_{DS}$, $T_{J} \le 150$ °C
- d. 1.6 mm from case



Vishay Siliconix

THERMAL RESISTANCE RATINGS					
PARAMETER SYMBOL TYP. MAX. UNIT					
Maximum Junction-to-Ambient	R _{thJA}	-	40	°C/W	
Maximum Junction-to-Case (Drain)	R _{thJC}	-	0.75	G/ VV	

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	V _{DS}	$V_{GS} = 0, I_D = 250 \mu A$		600	-	-	V
V _{DS} Temperature Coefficient	$\Delta V_{DS}/T_{J}$	Reference	ce to 25 °C, I _D = 1 mA	-	0.66	-	V/°C
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} :	= V _{GS} , I _D = 250 μA	2.0	-	4.0	V
Gate-Source Leakage	I _{GSS}		$V_{GS} = \pm 30 \text{ V}$	-	-	± 100	nA
Zero Gate Voltage Drain Current	1	V _{DS} :	= 600 V, V _{GS} = 0 V	-	-	25	μА
Zero Gate Voltage Drain Current	I _{DSS}	$V_{DS} = 480 \text{ V}$	$V_{\rm S} = 0 \ V_{\rm S} = 125 \ ^{\circ}{\rm C}$	1	-	250	
Drain-Source On-State Resistance	R _{DS(on)}	V _{GS} = 10 V	I _D = 5.5 A ^b	-	-	0.75	Ω
Forward Transconductance	9 _{fs}	V _{DS}	= 25 V, I _D = 3.1 A	5.5	-	-	S
Dynamic							
Input Capacitance	C_{iss}		$V_{GS} = 0 V$	1	1400	-	
Output Capacitance	C _{oss}]	$V_{DS} = 25 \text{ V},$	-	180	-	
Reverse Transfer Capacitance	C_{rss}	f = 1	f = 1.0 MHz, see fig. 5		7.1	-	1
Output Capacitance	C _{oss}	V _{GS} = 0 V	$V_{DS} = 1.0 \text{ V}, f = 1.0 \text{ MHz}$	-	1957	-	- pF -
			V _{DS} = 480 V, f = 1.0 MHz	-	49	-	
Effective Output Capacitance	Coss eff.		$V_{DS} = 0 \text{ V to } 480 \text{ V}^{\text{ c}}$	1	96	-	
Total Gate Charge	Q_g			ı	-	49	
Gate-Source Charge	Q_{gs}	V _{GS} = 10 V	$V_{GS} = 10 \text{ V}$ $I_D = 9.2 \text{ A}, V_{DS} = 400 \text{ V}$ see fig. 6 and 13 b		-	13	nC
Gate-Drain Charge	Q_{gd}				-	20	
Turn-On Delay Time	t _{d(on)}	$V_{DD} = 300 \text{ V, } I_{D} = 9.2 \text{ A}$ $R_{g} = 9.1 \Omega, R_{D} = 35.5 \Omega,$ see fig. 10 ^b		1	13	-	ns
Rise Time	t _r			ı	25	-	
Turn-Off Delay Time	t _{d(off)}			1	30	-	
Fall Time	t _f			1	22	-	
Gate Input Resistance	R_{g}	f = 1 MHz, open drain		0.5	-	3.2	Ω
Drain-Source Body Diode Characteristic	s						
Continuous Source-Drain Diode Current	I _S	MOSFET symbol showing the integral reverse p - n junction diode		ı	-	9.2	A
Pulsed Diode Forward Current ^a	I _{SM}			-	-	37	
Body Diode Voltage	V _{SD}	$T_J = 25 ^{\circ}\text{C}, I_S = 9.2 \text{A}, V_{GS} = 0 \text{V}^{ \text{b}}$		-	-	1.5	V
Body Diode Reverse Recovery Time	t _{rr}	$T_J = 25 \text{ °C}, I_F = 9.2 \text{ A, dl/dt} = 100 \text{ A/µs}^{\text{b}}$		-	530	800	ns
Body Diode Reverse Recovery Charge	Q_{rr}			-	3.0	4.4	μC
Forward Turn-On Time	t _{on}	Intrinsic tu	ırn-on time is negligible (turn	on is dor	ninated b	v Le and	L _D)

Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
- b. Pulse width \leq 300 μ s; duty cycle \leq 2 %
- c. C_{oss} eff. is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80 % V_{DS}



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

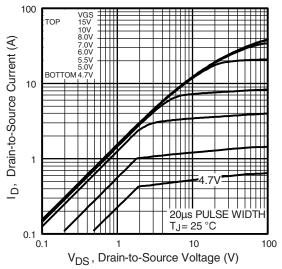
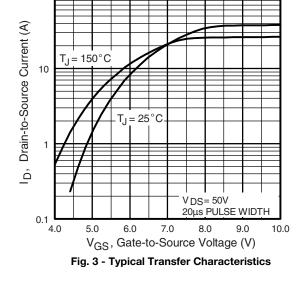


Fig. 1 - Typical Output Characteristics



100

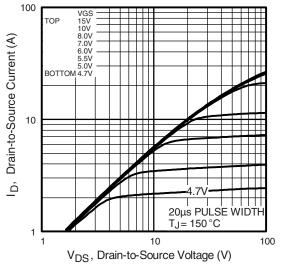


Fig. 2 - Typical Output Characteristics

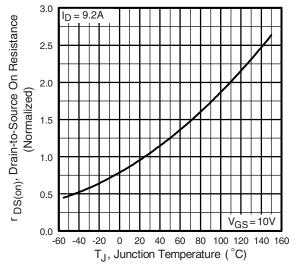


Fig. 4 - Normalized On-Resistance vs. Temperature



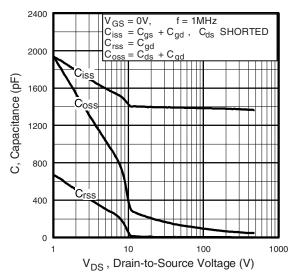


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

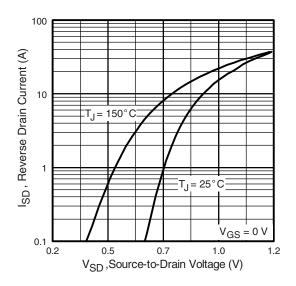


Fig. 7 - Typical Source-Drain Diode Forward Voltage

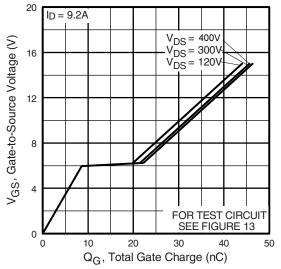


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

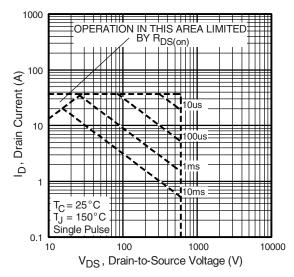


Fig. 1 - Maximum Safe Operating Area



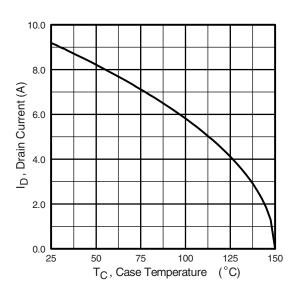


Fig. 8 - Maximum Drain Current vs. Case Temperature

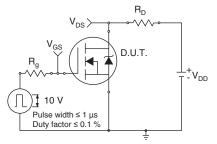


Fig. 10a - Switching Time Test Circuit

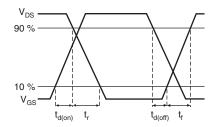


Fig. 10b - Switching Time Waveforms

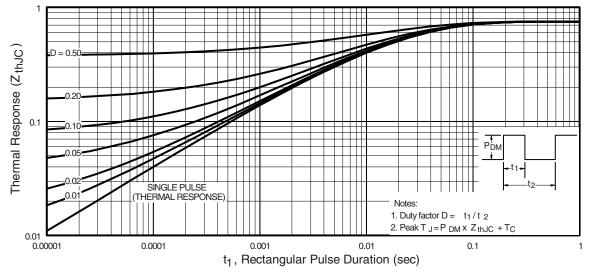


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

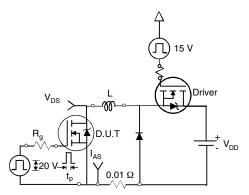


Fig. 12a - Unclamped Inductive Test Circuit

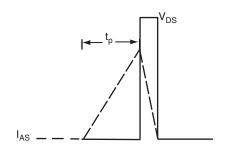


Fig. 12b - Unclamped Inductive Waveforms

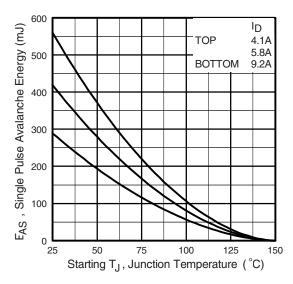


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

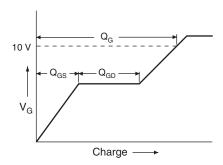


Fig. 13a - Basic Gate Charge Waveform

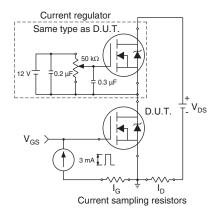
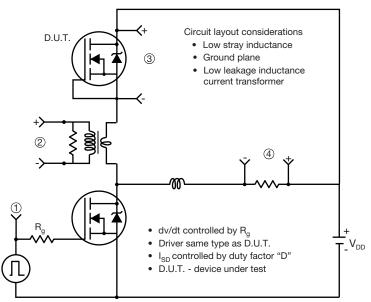


Fig. 13b - Gate Charge Test Circuit



Peak Diode Recovery dv/dt Test Circuit



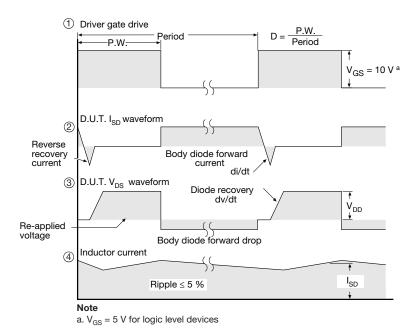


Fig. 14 - For N-Channel

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TO-263AB (HIGH VOLTAGE)







	MILLIN	METERS	INC	HES
DIM.	MIN.	MAX.	MIN.	MAX.
Α	4.06	4.83	0.160	0.190
A1	0.00	0.25	0.000	0.010
b	0.51	0.99	0.020	0.039
b1	0.51	0.89	0.020	0.035
b2	1.14	1.78	0.045	0.070
b3	1.14	1.73	0.045	0.068
С	0.38	0.74	0.015	0.029
c1	0.38	0.58	0.015	0.023
c2	1.14	1.65	0.045	0.065
D	8.38	9.65	0.330	0.380

	MILLIMETERS		INC	HES
DIM.	MIN.	MAX.	MIN.	MAX.
D1	6.86	-	0.270	-
Е	9.65	10.67	0.380	0.420
E1	6.22	-	0.245	ı
е	2.54 BSC		0.100 BSC	
Н	14.61	15.88	0.575	0.625
L	1.78	2.79	0.070	0.110
L1	-	1.65	ı	0.066
L2	-	1.78	-	0.070
L3	0.25 BSC		0.010	BSC
L4	4.78	5.28	0.188	0.208

ECN: S-82110-Rev. A, 15-Sep-08

DWG: 5970

Notes

- 1. Dimensioning and tolerancing per ASME Y14.5M-1994.
- 2. Dimensions are shown in millimeters (inches).
- 3. Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outmost extremes of the plastic body at datum A.
- 4. Thermal PAD contour optional within dimension E, L1, D1 and E1.
- 5. Dimension b1 and c1 apply to base metal only.
- 6. Datum A and B to be determined at datum plane H.
- 7. Outline conforms to JEDEC outline to TO-263AB.

Document Number: 91364 www.vishay.com Revision: 15-Sep-08





RECOMMENDED MINIMUM PADS FOR D²PAK: 3-Lead



Recommended Minimum Pads Dimensions in Inches/(mm)

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