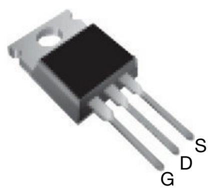
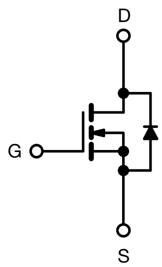
D Series Power MOSFET

TO-220AB





N-Channel MOSFET

PRODUCT SUMMARY		
V_{DS} (V) at T_J max.	450	
$R_{DS(on)}$ max. (Ω) at 25 °C	V_{GS} = 10 V	1.0
Q_g max. (nC)	18	
Q_{gs} (nC)	3	
Q_{gd} (nC)	4	
Configuration	Single	

FEATURES

- Optimal design
  - Low area specific on-resistance
  - Low input capacitance (C_{iss})
  - Reduced capacitive switching losses
  - High body diode ruggedness
  - Avalanche energy rated (UIS)
- Optimal efficiency and operation
  - Low cost
  - Simple gate drive circuitry
  - Low figure-of-merit (FOM): R_{on} x Q_g
  - Fast switching
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

RoHS* Available

HALOGEN FREE Available

Note

* This datasheet provides information about parts that are RoHS-compliant and / or parts that are non RoHS-compliant. For example, parts with lead (Pb) terminations are not RoHS-compliant. Please see the information / tables in this datasheet for details

APPLICATIONS

- Consumer electronics
  - Displays (LCD or plasma TV)
- Server and telecom power supplies
  - SMPS
- Industrial
  - Welding
  - Induction heating
- Motor drives
- Battery chargers

ORDERING INFORMATION	
Package	TO-220AB
Lead (Pb)-free	SiHP6N40D-E3
Lead (Pb)-free and halogen-free	SiHP6N40D-BE3 [a]
	SiHP6N40D-GE3

Note

a. "-BE3" denotes alternate manufacturing location

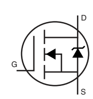
ABSOLUTE MAXIMUM RATINGS (T_C = 25 °C, unless otherwise noted)

PARAMETER			SYMBOL	LIMIT	UNIT
Drain-source voltage			V_{DS}	400	V
Gate-source voltage			V_{GS}	± 30	
Gate-source voltage AC (f > 1 Hz)				30	
Continuous drain current (T_J = 150 °C)	V_{GS} at 10 V	T_C = 25 °C	I_D	6	A
		T_C = 100 °C		4	
Pulsed drain current [a]			I_{DM}	13	
Linear derating factor				0.8	W/°C
Single pulse avalanche energy [b]			E_{AS}	104	mJ
Maximum power dissipation			P_D	104	W
Operating junction and storage temperature range			T_J, T_{stg}	-55 to +150	°C
Drain-source voltage slope	T_J = 125 °C		dV/dt	24	V/ns
Reverse diode dV/dt [d]				0.48	
Soldering recommendations (peak temperature) [c]	For 10 s			300	°C

Notes

a. Repetitive rating; pulse width limited by maximum junction temperature
b. V_{DD} = 50 V, starting T_J = 25 °C, L = 2.3 mH, R_g = 25 Ω, I_{AS} = 9.5 A
c. 1.6 mm from case
d. $I_{SD} \leq I_D$, starting T_J = 25 °C

THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum junction-to-ambient	R_{thJA}	-	62	°C/W
Maximum junction-to-case (drain)	R_{thJC}	-	1.2	

SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-source breakdown voltage	V_{DS}	V_{GS} = 0 V, I_D = 250 μA		400	-	-	V
V_{DS} temperature coefficient	$\Delta V_{DS}/T_J$	Reference to 25 °C, I_D = 250 μA		-	0.53	-	V/°C
Gate-source threshold Voltage (N)	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 μA		3	-	5	V
Gate-source leakage	I_{GSS}	V_{GS} = ± 30 V		-	-	± 100	nA
Zero gate voltage drain current	I_{DSS}	V_{DS} = 400 V, V_{GS} = 0 V		-	-	1	μA
		V_{DS} = 320 V, V_{GS} = 0 V, T_J = 125 °C		-	-	10	
Drain-source on-state resistance	$R_{DS(on)}$	V_{GS} = 10 V	I_D = 3 A	-	0.85	1.0	Ω
Forward transconductance	g_{fs}	V_{DS} = 50 V, I_D = 3 A		-	1.7	-	S
Dynamic							
Input capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 100 V, f = 1 MHz		-	311	-	pF
Output capacitance	C_{oss}			-	38	-	
Reverse transfer capacitance	C_{rss}			-	7	-	
Effective output capacitance, energy related [a]	$C_{o(er)}$	V_{GS} = 0 V, V_{DS} = 0 V to 320 V		-	44	-	
Effective output capacitance, time related [b]	$C_{o(tr)}$			-	54	-	
Total gate charge	Q_g	V_{GS} = 10 V	I_D = 3 A, V_{DS} = 320 V	-	9	18	nC
Gate-source charge	Q_{gs}			-	3	-	
Gate-drain charge	Q_{gd}			-	4	-	
Turn-on delay time	$t_{d(on)}$	V_{DD} = 400 V, I_D = 3 A, V_{GS} = 10 V, R_g = 9.1 Ω		-	12	24	ns
Rise time	t_r			-	11	22	
Turn-off delay time	$t_{d(off)}$			-	14	28	
Fall time	t_f			-	8	16	
Gate input resistance	R_g	f = 1 MHz, open drain		1.0	1.9	3.8	Ω
Drain-Source Body Diode Characteristics							
Continuous source-drain diode current	I_S	MOSFET symbol showing the integral reverse p - n junction diode		-	-	6	A
Pulsed diode forward current	I_{SM}			-	-	24	
Diode forward voltage	V_{SD}	T_J = 25 °C, I_S = 3 A, V_{GS} = 0 V		-	-	1.2	V
Reverse recovery time	t_{rr}	T_J = 25 °C, I_F = I_S = 3 A, dI/dt = 100 A/μs, V_R = 20 V		-	236	-	ns
Reverse recovery charge	Q_{rr}			-	1.1	-	μC
Reverse recovery current	I_{RRM}			-	9	-	A

Notes

a. $C_{oss(er)}$ is a fixed capacitance that gives the same energy as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DS}

b. $C_{oss(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DS}

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

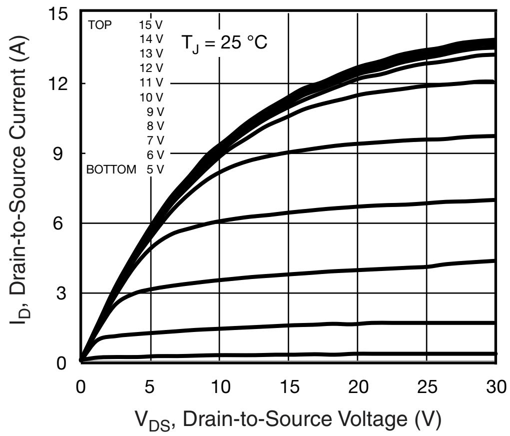


Fig. 1 - Typical Output Characteristics

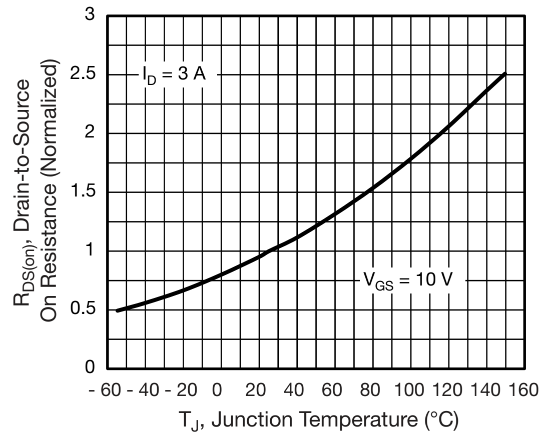


Fig. 4 - Normalized On-Resistance vs. Temperature

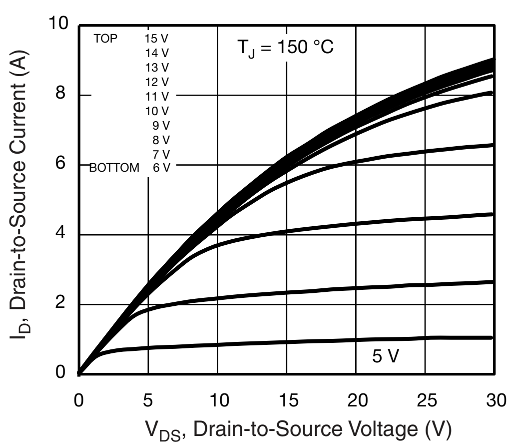


Fig. 2 - Typical Output Characteristics

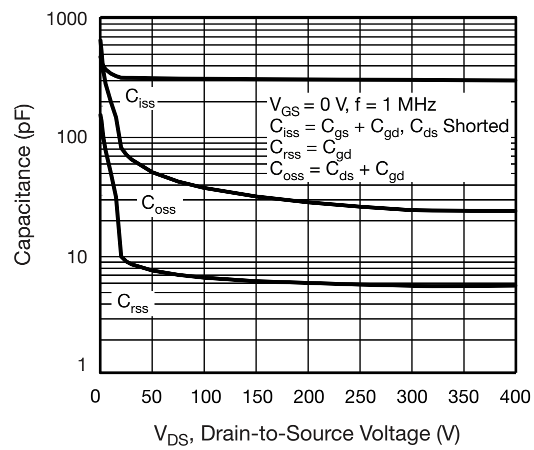


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

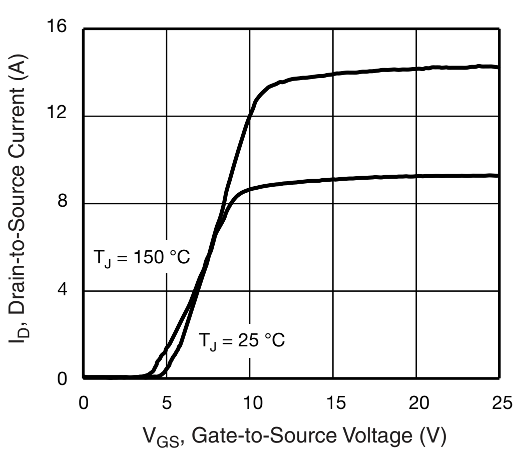


Fig. 3 - Typical Transfer Characteristics

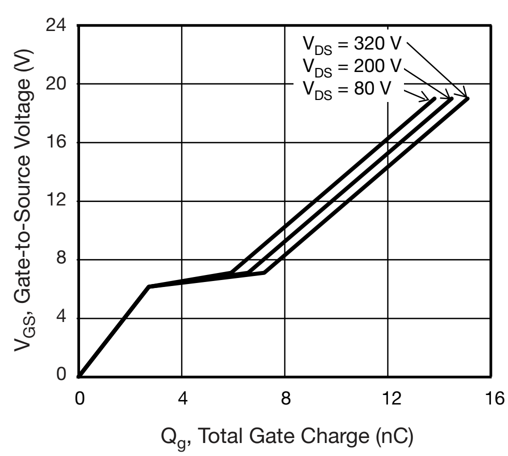


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

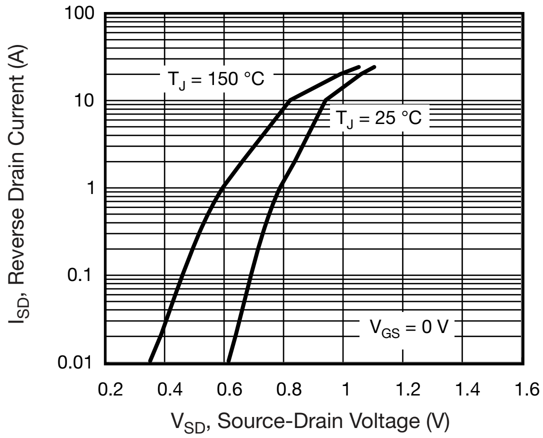


Fig. 7 - Typical Source-Drain Diode Forward Voltage

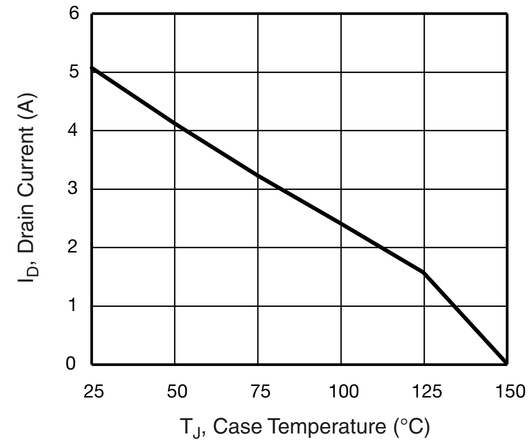


Fig. 9 - Maximum Drain Current vs. Case Temperature

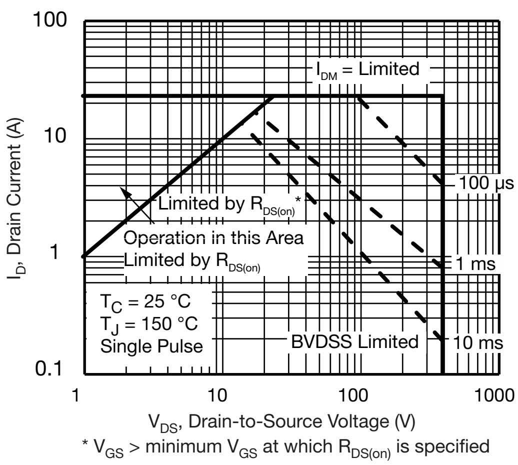


Fig. 8 - Maximum Safe Operating Area

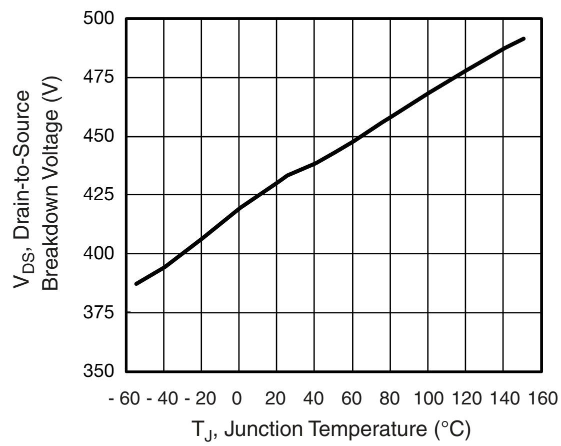


Fig. 10 - Temperature vs. Drain-to-Source Voltage

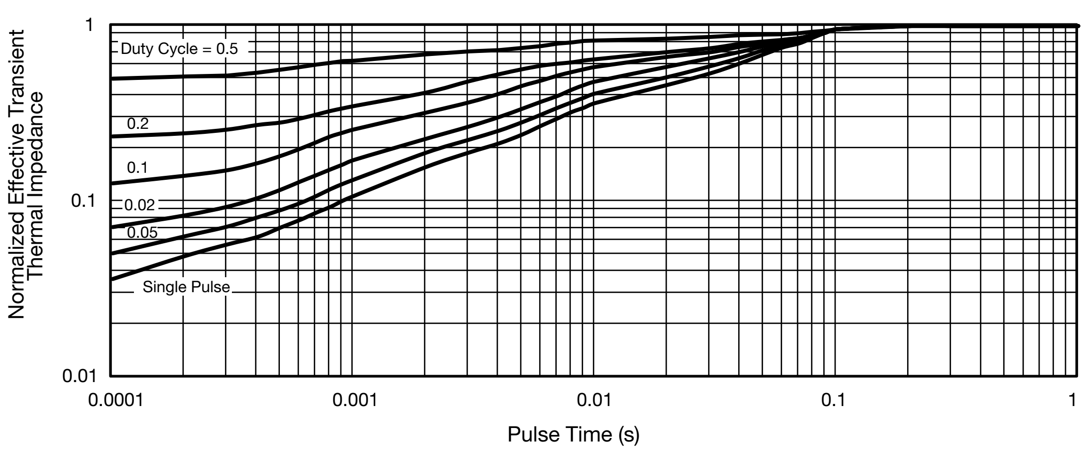


Fig. 11 - Normalized Thermal Transient Impedance, Junction-to-Case

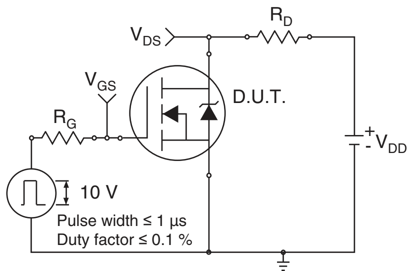


Fig. 12 - Switching Time Test Circuit

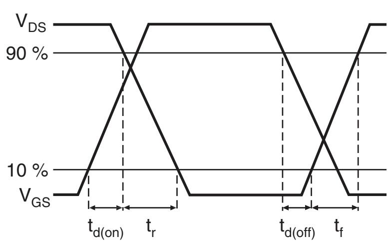


Fig. 13 - Switching Time Waveforms

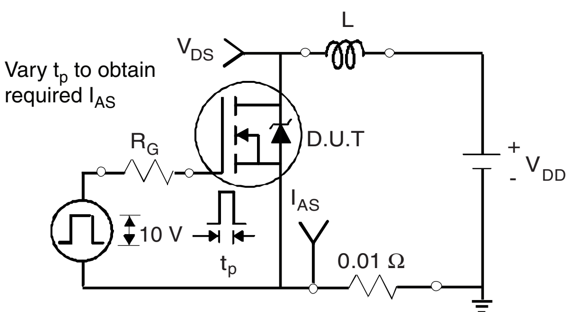


Fig. 14 - Unclamped Inductive Test Circuit

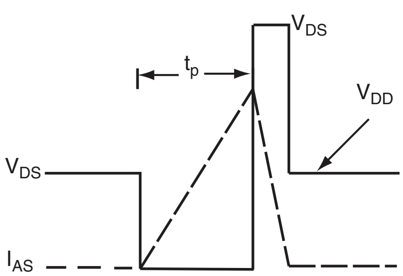


Fig. 15 - Unclamped Inductive Waveforms

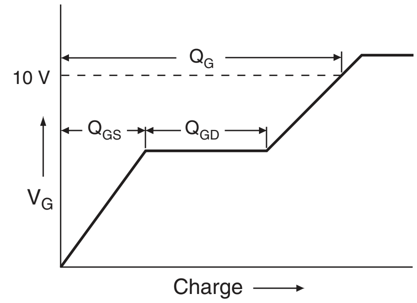


Fig. 16 - Basic Gate Charge Waveform

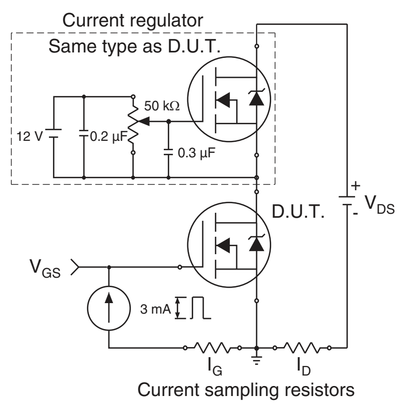
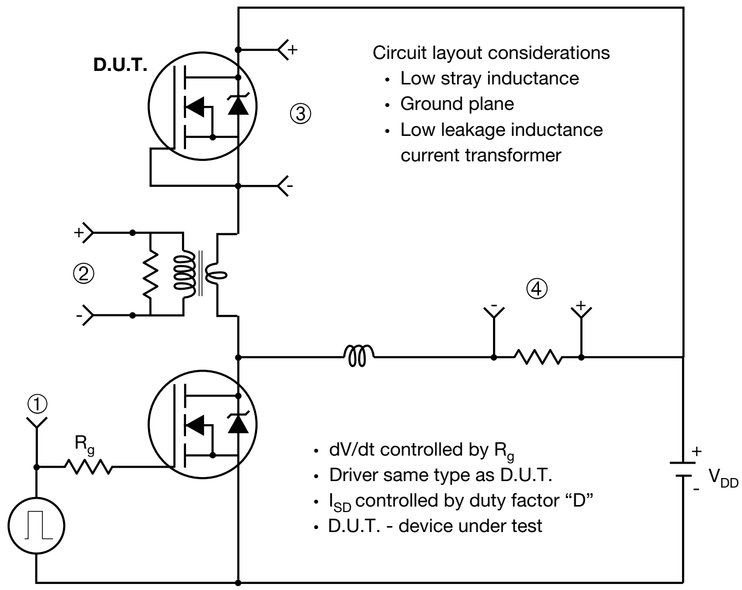
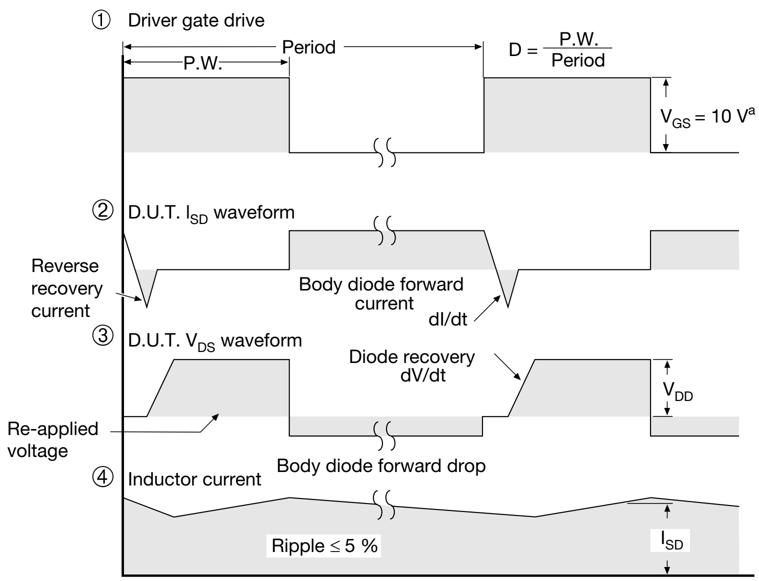


Fig. 17 - Gate Charge Test Circuit

For technical questions, contact: hvm@vishay.com

Peak Diode Recovery dV/dt Test Circuit





Note

a. V_{GS} = 5 V for logic level devices

Fig. 18 - For N-Channel

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