



N-Channel 30 V (D-S) MOSFET

PRODUCT SUMMARY					
V _{DS} (V)	$R_{DS(on)}(\Omega)$	I _D (A)	Q _g (Typ.)		
30	0.099 at V _{GS} = 4.5 V	1.2 ^a	3.5		
	0.140 at V _{GS} = 2.5 V	1.0	3.5		

FEATURES

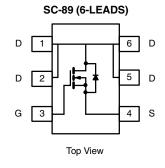
- Halogen-free According to IEC 61249-2-21 Definition
- TrenchFET® Power MOSFET
- 100 % R_q and UIS Tested
- Compliant to RoHS Directive 2002/95/EC

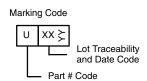


ROHS COMPLIANT HALOGEN FREE

APPLICATIONS

· Load Switch for Portable Devices





Ordering Information: Si1070X-T1-GE3 (Lead (Pb)-free and Halogen-free)

ABSOLUTE MAXIMUM RATINGS (T _A = 25 °C, unless otherwise noted)						
Parameter		Symbol	Limit	Unit		
Drain-Source Voltage		V_{DS}	30	V		
Gate-Source Voltage		V_{GS}	± 12			
Continuous Drain Current (T _{.I} = 150 °C) ^a	T _A = 25 °C	I_	1.2 ^{b, c}			
	T _A = 70 °C	l _D	1 ^{b, c}	A		
Pulsed Drain Current		I _{DM}	6	1		
Avalanche Current	L = 0.1 mH	I _{AS}	9			
Repetitive Avalanche Energy	L = 0.1 11111	E _{AS}	4.01	mJ		
Continuous Source-Drain Diode Current	T _A = 25 °C	I _S	0.2 ^{b, c}	Α		
Marrian Danier Dissipation	T _A = 25 °C	P _D	0.236 ^{b, c}	- w		
Maximum Power Dissipation ^a	T _A = 70 °C] 'D]	0.151 ^{b, c}			
Operating Junction and Storage Temperature Range		T _J , T _{stg}	- 55 to 150	°C		

THERMAL RESISTANCE RATINGS						
Parameter		Symbol	Typical	Maximum	Unit	
Adamiana kanadian ta Anakian ta d	t ≤ 5 s	R _{thJA}	440	530	°C/W	
Maximum Junction-to-Ambient ^{b, d}	Steady State		540	650	C/VV	

Notes:

- a. Based on $T_C = 25$ °C.
- b. Surface mounted on 1" x 1" FR4 board.
- c. t = 5 s.
- d. Maximum under steady state conditions is 650 $^{\circ}\text{C/W}.$

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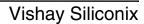


Parameter	Symbol	Test Conditions Min.		Тур.	Max.	Unit	
Static			•			•	
Drain-Source Breakdown Voltage	V _{DS}	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$	30			V	
V _{DS} Temperature Coefficient	$\Delta V_{DS}/T_{J}$	I _D = 250 μA		24.5		mV/°C	
V _{GS(th)} Temperature Coefficient	$\Delta V_{GS(th)}/T_J$	η _D = 250 μΑ		- 3.81		mv/°C	
Gate-Source Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$	0.7		1.55	V	
Gate-Source Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 12 V			± 100	nA	
Zovo Coto Voltogo Dvoin Current	I _{DSS}	V _{DS} = 30 V, V _{GS} = 0 V			1	nA	
Zero Gate Voltage Drain Current		V _{DS} = 30 V, V _{GS} = 0 V, T _J = 85 °C			10	μΑ	
On-State Drain Current ^a	I _{D(on)}	$V_{DS} = \ge 5 \text{ V}, V_{GS} = 4.5 \text{ V}$	6			Α	
Durin Course On Other During	D	V _{GS} = 4.5 V, I _D = 1.2 A		0.082	0.099	Ω	
Drain-Source On-State Resistance ^a	$R_{DS(on)}$	V _{GS} = 2.5 V, I _D = 1.0 A		0.116	0.140		
Forward Transconductance	9 _{fs}	V _{DS} = 15 V, I _D = 1.2 A		5		S	
Dynamic ^b			•			•	
Input Capacitance	C _{iss}			385		pF	
Output Capacitance	C _{oss}	$V_{DS} = 15 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$		55			
Reverse Transfer Capacitance	C _{rss}			30			
Total Cata Charge		$V_{DS} = 15 \text{ V}, V_{GS} = 5 \text{ V}, I_D = 1.2 \text{ A}$		3.8	8.3	nC	
Total Gate Charge	Q_g			3.5	4.1		
Gate-Source Charge	Q _{gs}	$V_{DS} = 15 \text{ V}, V_{GS} = 4.5 \text{ V}, I_{D} = 4.6 \text{ A}$		1.1			
Gate-Drain Charge	Q _{gd}			0.98		1	
Gate Resistance	R _g	f = 1 MHz	MHz 4.7		6.2	Ω	
Turn-On Delay Time	t _{d(on)}			10	15		
Rise Time	t _r	$V_{DD} = 15 \text{ V}, R_{L} = 15 \Omega$		22	33	- ns	
Turn-Off DelayTime	t _{d(off)}	$I_D \cong 1.0 \text{ A}, V_{GEN} = 4.5 \text{ V}, R_g = 1 \Omega$		14	21		
Fall Time	t _f			6	9		
Drain-Source Body Diode Characterist	ics					•	
Pulse Diode Forward Current ^a	I _{SM}				6	Α	
Body Diode Voltage	V_{SD}	I _S = 1.2 A		0.8	1.2	V	
Body Diode Reverse Recovery Time	t _{rr}			19.4	29.5	nC	
Body Diode Reverse Recovery Charge	Q_{rr}	1 _ 2 0 A dl/d+ 100 A/vc		18.43	27.5		
Reverse Recovery Fall Time	ta	$I_F = 3.8 \text{ A}, \text{ dI/dt} = 100 \text{ A/}\mu\text{s}$		16.4		ns	
Reverse Recovery Rise Time	t _b			3			

Notes:

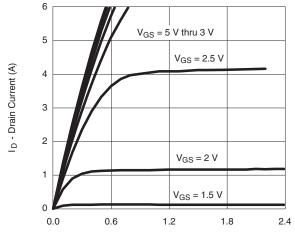
- a. Pulse test; pulse width $\leq 300~\mu s,$ duty cycle $\leq 2~\%.$
- b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



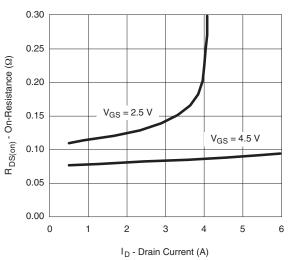


TYPICAL CHARACTERISTICS ($T_A = 25$ °C, unless otherwise noted)

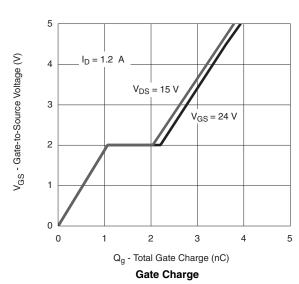


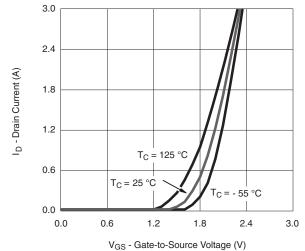
 V_{DS} - Drain-to-Source Voltage (V)

Output Characteristics

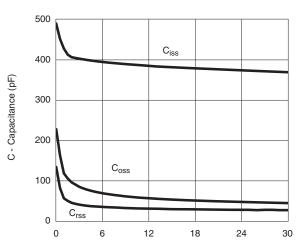


On-Resistance vs. Drain Current



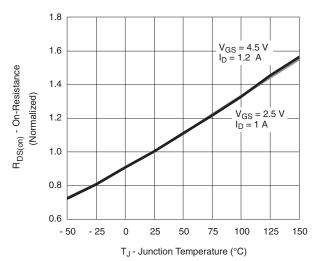


Transfer Characteristics Curves vs. Temp.



V_{DS} - Drain-to-Source Voltage (V)

Capacitance

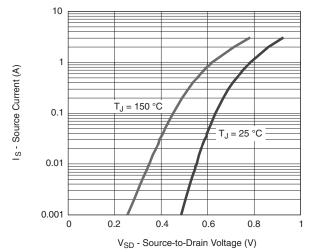


On-Resistance vs. Junction Temperature

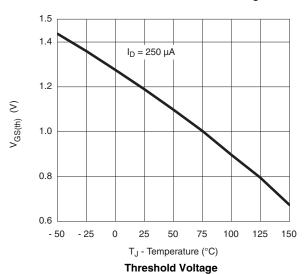
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TYPICAL CHARACTERISTICS ($T_A = 25$ °C, unless otherwise noted)

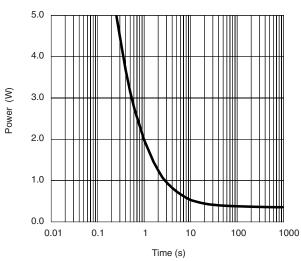


Source-Drain Diode Forward Voltage

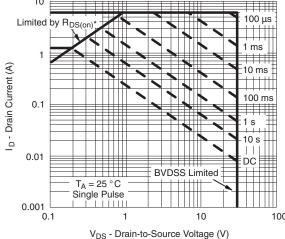


 C_{SO} 0.18 C_{D} 0.18 C_{D} 0.12 C_{D} 0.12 C_{D} 0.00 C_{D} 0

R_{DS(on)} vs. V_{GS} vs. Temperature



Single Pulse Power



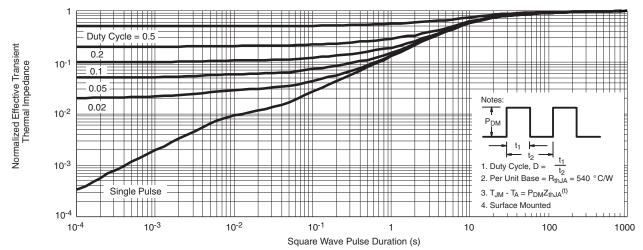
* V_{GS} > minimum V_{GS} at which $R_{DS(on)}$ is specified

Safe Operating Area, Junction-to-Ambient





TYPICAL CHARACTERISTICS ($T_A = 25$ °C, unless otherwise noted)

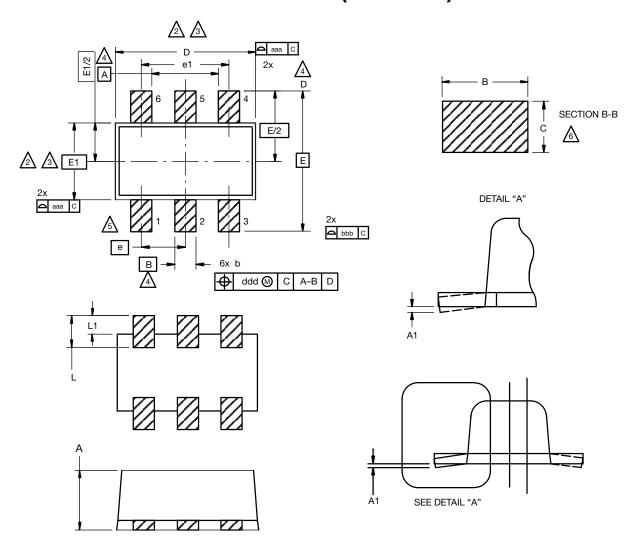


Normalized Thermal Transient Impedance, Junction-to-Ambient

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?73893.



SC-89 6-Leads (SOT-563F)



Notes

1. Dimensions in millimeters.

Dimension D does not include mold flash, protrusions or gate burrs. Mold flush, protrusions or gate burrs shall not exceed 0.15 mm per dimension E1 does not include interlead flash or protrusion, interlead flash or protrusion shall not exceed 0.15 mm per side.

Dimensions D and E1 are determined at the outmost extremes of the plastic body exclusive of mold flash, the bar burrs, gate burrs and interlead flash, but including any mismatch between the top and the bottom of the plastic body.

ADatums A, B and D to be determined 0.10 mm from the lead tip.

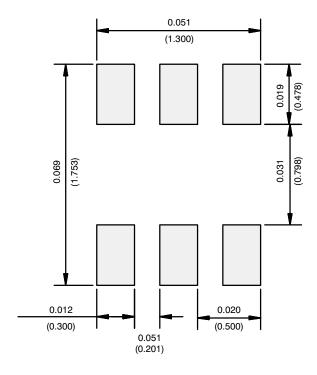
A Terminal numbers are shown for reference only.

These dimensions apply to the flat section of the lead between 0.08 mm and 0.15 mm from the lead tip.

DIM.	MILLIMETERS					
DIW.	MIN.	NOM.	MAX.			
Α	0.56	0.58	0.60			
A1	0	0.02	0.10			
b	0.15	0.22	0.30			
С	0.10	0.14	0.18			
D	1.50	1.60	1.70			
E	1.50	1.60	1.70			
E1	1.15	1.20	1.25			
е	0.45	0.50	0.55			
e1	0.95	1.00	1.05			
L	0.25	0.35	0.50			
L1	0.10	0.20	0.30			
C14-0439-Rev. C, 11-Aug-14 DWG: 5880						



RECOMMENDED MINIMUM PADS FOR SC-89: 6-Lead



Recommended Minimum Pads Dimensions in Inches/(mm)

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APPLICATION NOTE



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