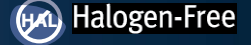


## EPC2036 – Enhancement Mode Power Transistor

 $V_{DS}, 100\text{ V}$  $R_{DS(on)}, 73\text{ m}\Omega$  $I_D, 1.7\text{ A}$ 

Gallium Nitride's exceptionally high electron mobility and low temperature coefficient allows very low  $R_{DS(on)}$ , while its lateral device structure and majority carrier diode provide exceptionally low  $Q_G$  and zero  $Q_{RR}$ . The end result is a device that can handle tasks where very high switching frequency, and low on-time are beneficial as well as those where on-state losses dominate.

## Maximum Ratings

PARAMETER		VALUE	UNIT
$V_{DS}$	Drain-to-Source Voltage (Continuous)	100	V
	Drain-to-Source Voltage (up to 10,000 5 ms pulses at 150°C)	120	
$I_D$	Continuous ( $T_A = 25^\circ\text{C}$ , $R_{\theta JA} = 340^\circ\text{C/W}$ )	1.7	A
	Pulsed ( $25^\circ\text{C}$ , $T_{PULSE} = 300\ \mu\text{s}$ )	18	
$V_{GS}$	Gate-to-Source Voltage	6	V
	Gate-to-Source Voltage	-4	
$T_J$	Operating Temperature	-40 to 150	$^\circ\text{C}$
$T_{STG}$	Storage Temperature	-40 to 150	

## Thermal Characteristics

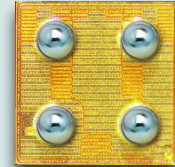
PARAMETER		TYP	UNIT
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	6	$^\circ\text{C/W}$
$R_{\theta JB}$	Thermal Resistance, Junction-to-Board	49	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1)	100	

Note 1:  $R_{\theta JA}$  is determined with the device mounted on one square inch of copper pad, single layer 2 oz copper on FR4 board. See [https://epc-co.com/epc/documents/product-training/Appnote\\_Thermal\\_Performance\\_of\\_eGaN\\_FETs.pdf](https://epc-co.com/epc/documents/product-training/Appnote_Thermal_Performance_of_eGaN_FETs.pdf) for details

Static Characteristics ( $T_J = 25^\circ\text{C}$  unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$BV_{DSS}$	Drain-to-Source Voltage	$V_{GS} = 0\text{ V}$ , $I_D = 300\ \mu\text{A}$	100			V
$I_{DSS}$	Drain-Source Leakage	$V_{DS} = 80\text{ V}$ , $V_{GS} = 0\text{ V}$		20	250	$\mu\text{A}$
$I_{GSS}$	Gate-to-Source Forward Leakage	$V_{GS} = 5\text{ V}$		0.1	0.9	mA
	Gate-to-Source Reverse Leakage	$V_{GS} = -4\text{ V}$		20	250	$\mu\text{A}$
$V_{GS(TH)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$ , $I_D = 0.6\text{ mA}$	0.8	1.4	2.5	V
$R_{DS(on)}$	Drain-Source On Resistance	$V_{GS} = 5\text{ V}$ , $I_D = 1\text{ A}$		62	73	$\text{m}\Omega$
$V_{SD}$	Source-Drain Forward Voltage	$I_S = 0.5\text{ A}$ , $V_{GS} = 0\text{ V}$		1.9		V

All measurements were done with substrate shorted to source.



EPC2036 eGaN® FETs are supplied only in passivated die form with solder bumps  
Die Size: 0.9 mm x 0.9 mm

## Applications

- High Speed DC-DC conversion
- Wireless Power Transfer
- High Frequency Hard-Switching and Soft-Switching Circuits
- Lidar/Pulsed Power Applications
- Class-D Audio

## Benefits

- Ultra High Efficiency
- Ultra Low  $R_{DS(on)}$
- Ultra Low  $Q_G$
- Ultra Small Footprint



Dynamic Characteristics ( $T_j = 25^\circ\text{C}$  unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$C_{ISS}$	Input Capacitance	$V_{DS} = 50\text{ V}, V_{GS} = 0\text{ V}$		75	90	pF
$C_{RSS}$	Reverse Transfer Capacitance			0.7	1.1	
$C_{OSS}$	Output Capacitance			50	75	
$R_G$	Gate Resistance			0.6		$\Omega$
$Q_G$	Total Gate Charge	$V_{DS} = 50\text{ V}, V_{GS} = 5\text{ V}, I_D = 1\text{ A}$		700	910	pC
$Q_{GS}$	Gate-to-Source Charge	$V_{DS} = 50\text{ V}, I_D = 1\text{ A}$		170		
$Q_{GD}$	Gate-to-Drain Charge			140	240	
$Q_{G(TH)}$	Gate Charge at Threshold			120		
$Q_{OSS}$	Output Charge	$V_{DS} = 50\text{ V}, V_{GS} = 0\text{ V}$		3900	5900	
$Q_{RR}$	Source-Drain Recovery Charge			0		

All measurements were done with substrate shorted to source.

Figure 1: Typical Output Characteristics at 25°C

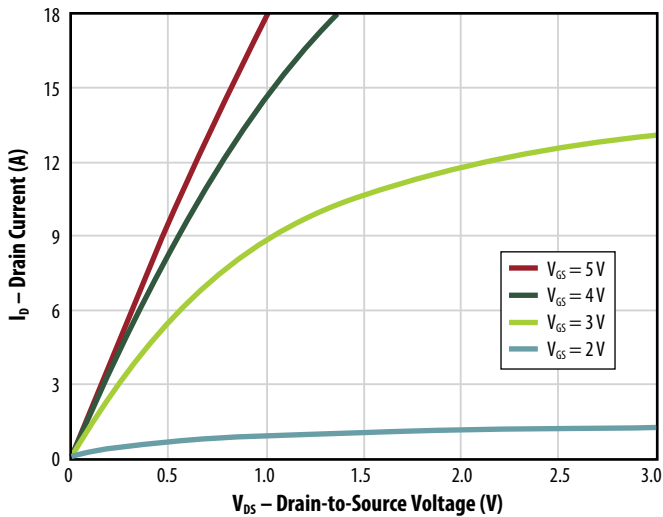


Figure 2: Transfer Characteristics

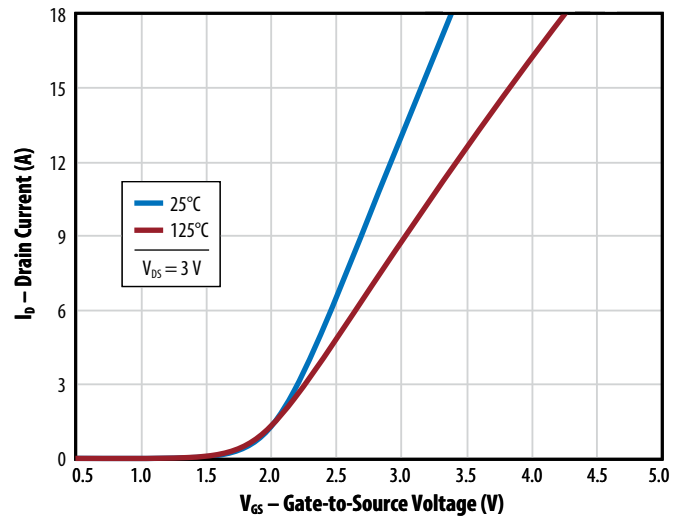


Figure 3:  $R_{DS(on)}$  vs.  $V_{GS}$  for Various Drain Currents

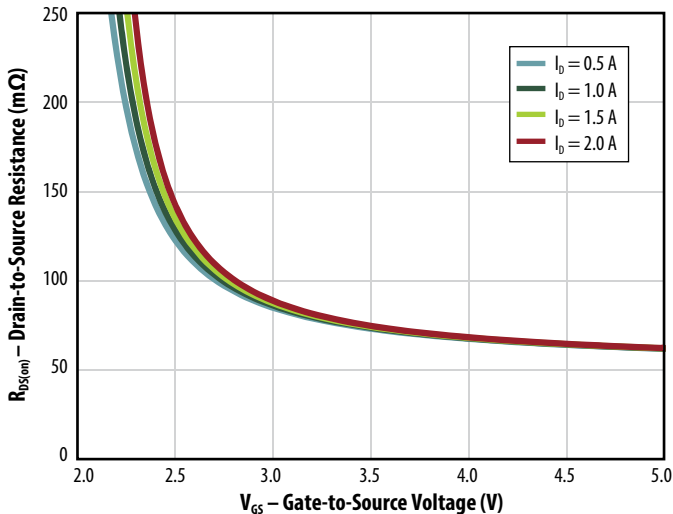


Figure 4:  $R_{DS(on)}$  vs.  $V_{GS}$  for Various Temperatures

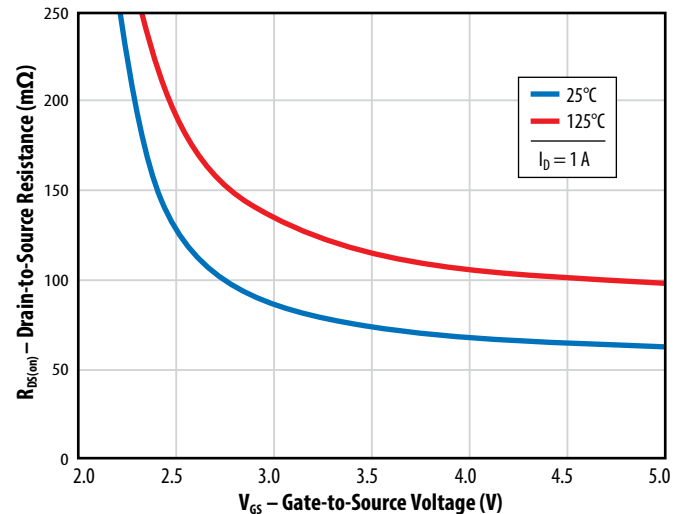


Figure 5a: Capacitance (Linear Scale)

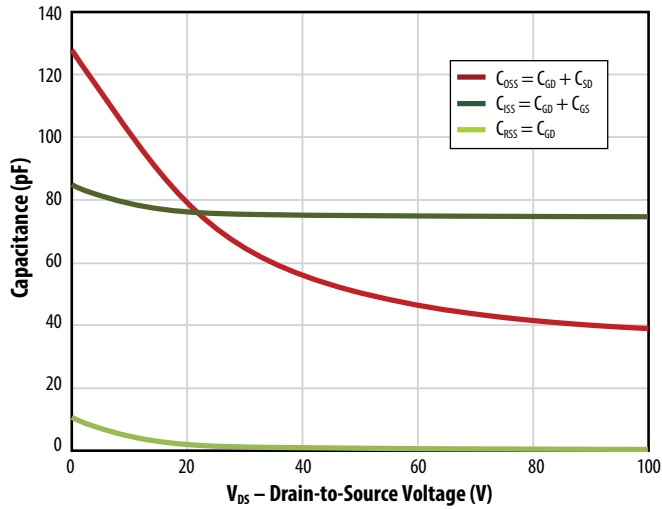


Figure 5b: Capacitance (Log Scale)

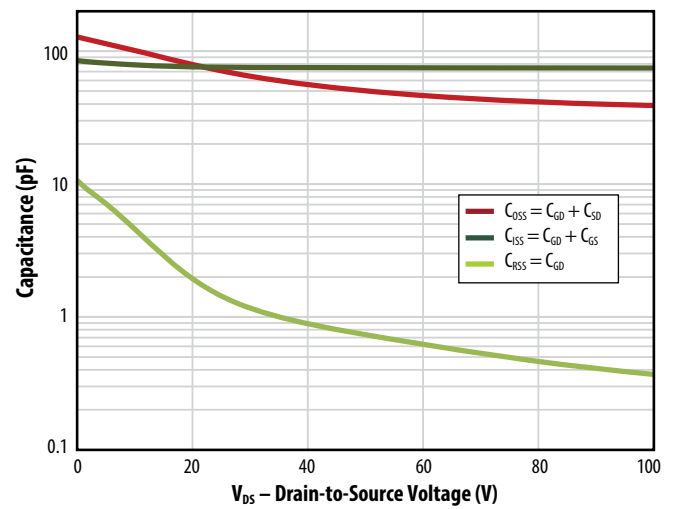


Figure 6: Gate Charge

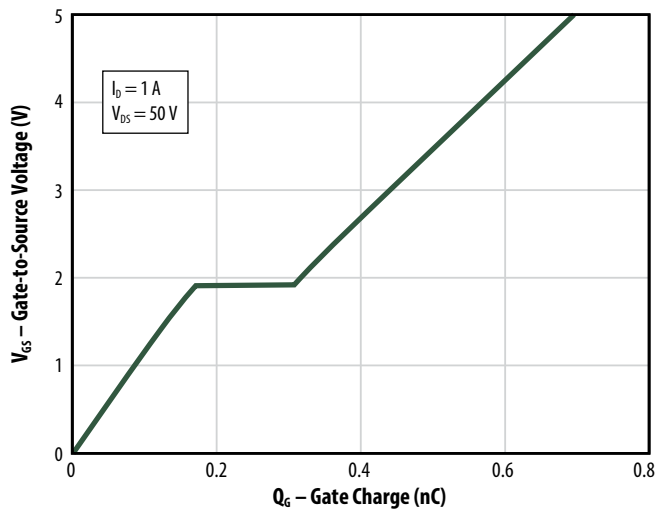


Figure 7: Reverse Drain-Source Characteristics

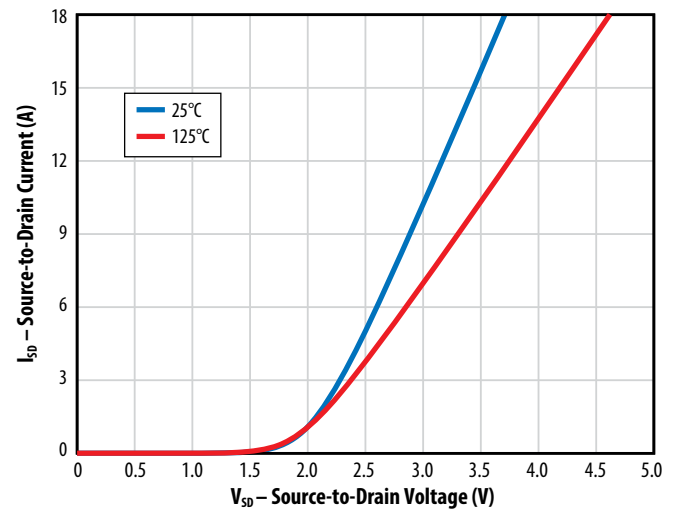


Figure 8: Normalized On Resistance vs. Temperature

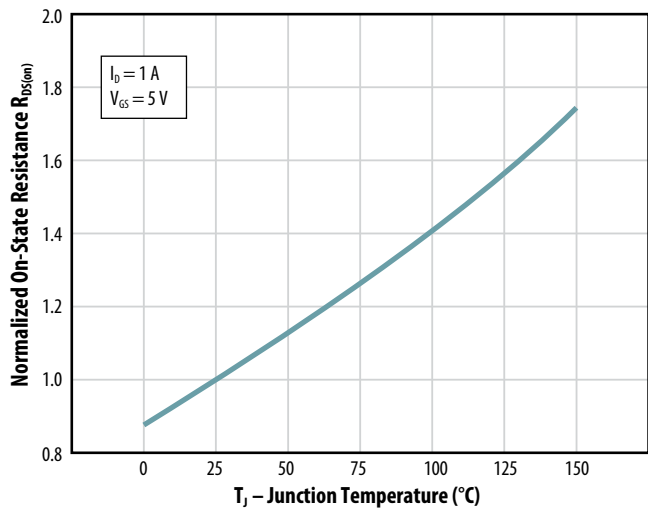
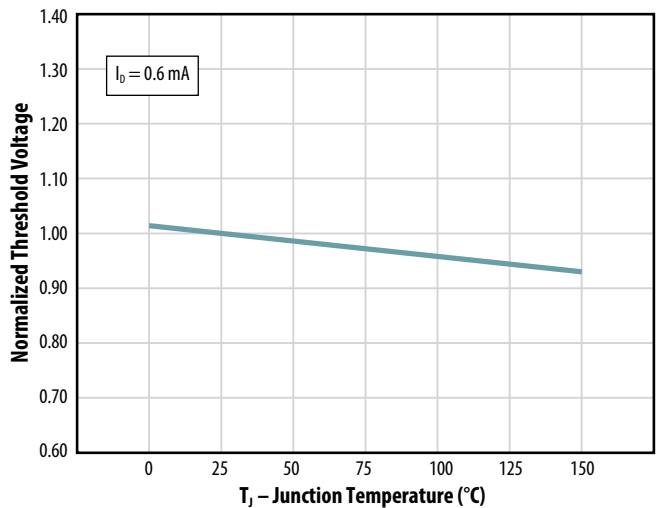


Figure 9: Normalized Threshold Voltage vs. Temperature



All measurements were done with substrate shorted to source.

Figure 10: Gate Leakage Current

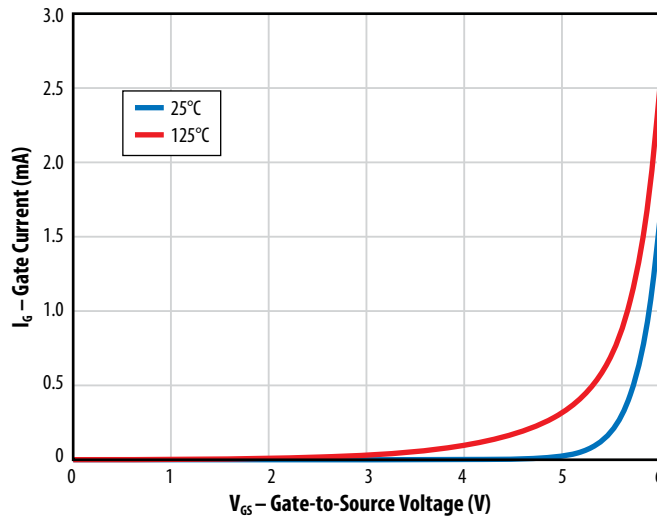


Figure 11: Transient Thermal Response Curves

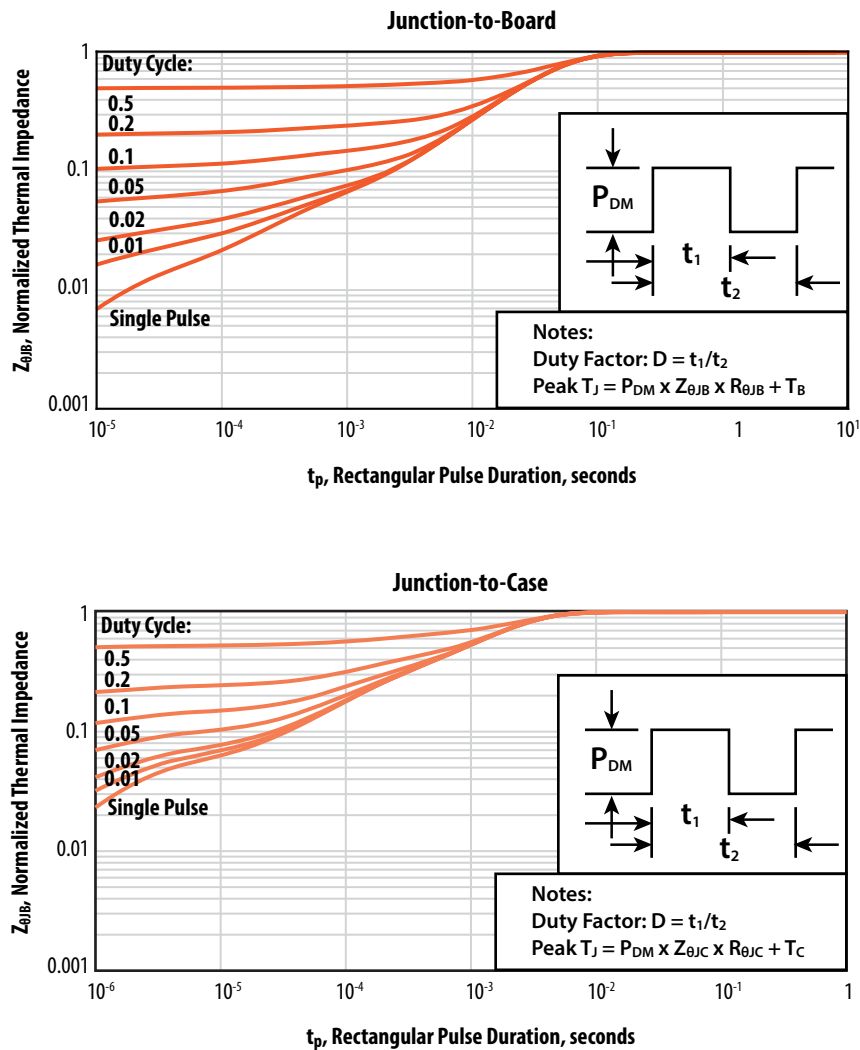
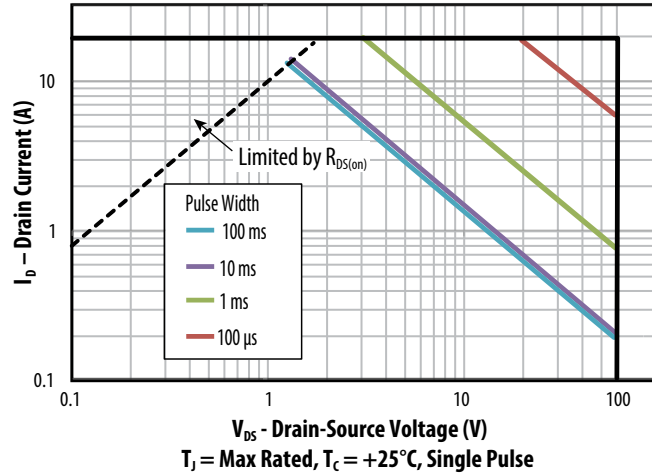
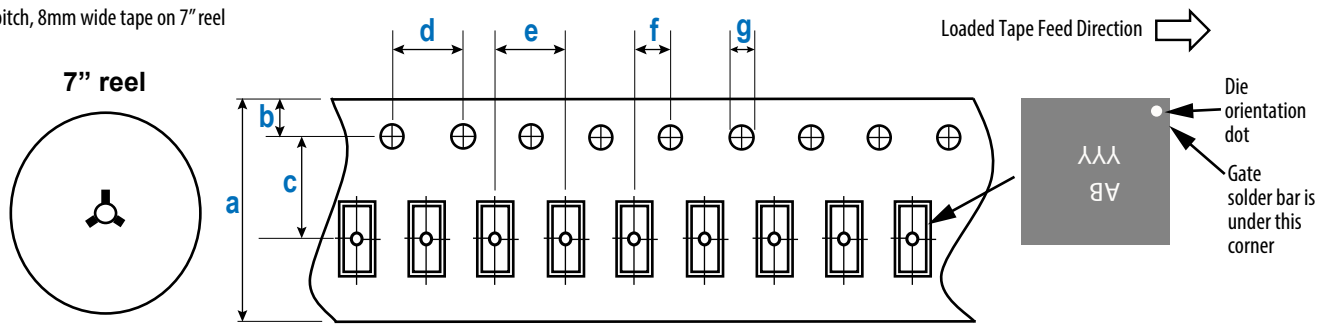


Figure 12: Safe Operating Area



**TAPE AND REEL CONFIGURATION**

4mm pitch, 8mm wide tape on 7" reel



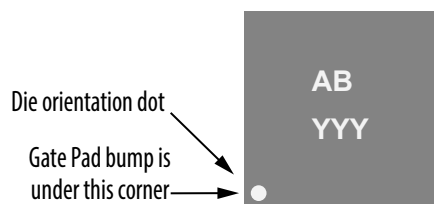
Die is placed into pocket solder bar side down (face side down)

EPC2036 (Note 1)	Dimension (mm)		
	Target	MIN	MAX
a	8.00	7.90	8.30
b	1.75	1.65	1.85
c (Note 2)	3.50	3.45	3.55
d	4.00	3.90	4.10
e	4.00	3.90	4.10
f (Note 2)	2.00	1.95	2.05
g	1.50	1.50	1.60

Note 1: MSL 1 (moisture sensitivity level 1) classified according to IPC/ JEDEC industry standard.

Note 2: Pocket position is relative to the sprocket hole measured as true position of the pocket, not the pocket hole.

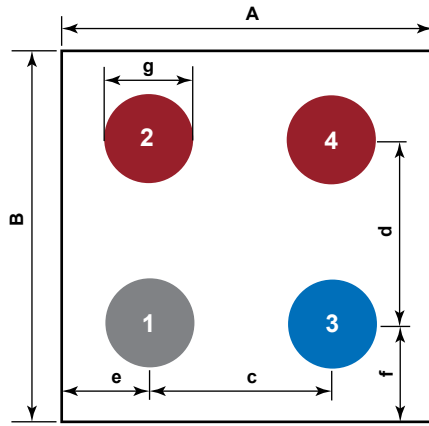
**DIE MARKINGS**



Part Number	Laser Markings	
	Part # Marking Line 1	Lot_Date Code Marking Line 2
EPC2036	AB	YYY

**DIE OUTLINE**

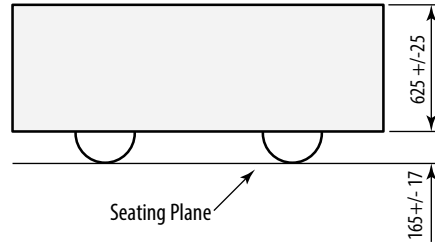
Solder Bump View



Pads 1 is Gate;  
Pad 3 is Drain;  
Pads 2, 4 are Source

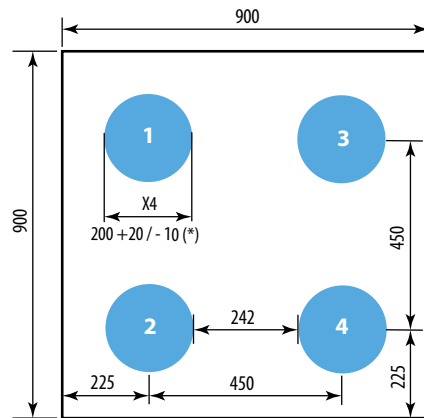
DIM	MIN	Nominal	MAX
A	870	900	930
B	870	900	930
c	450	450	450
d	450	450	450
e	210	225	240
f	210	225	240
g	187	208	229

Side View



**RECOMMENDED LAND PATTERN**

(measurements in  $\mu\text{m}$ )



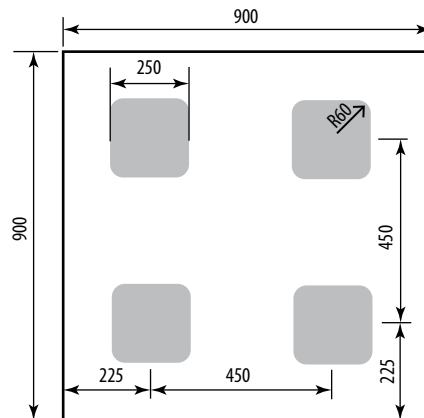
\* minimum 190

The land pattern is solder mask defined  
Solder mask is 10  $\mu\text{m}$  smaller per side than bump

Pads 1 is Gate;  
Pad 3 is Drain;  
Pads 2, 4 are Source

**RECOMMENDED STENCIL DRAWING**

(measurements in  $\mu\text{m}$ )



Recommended stencil should be 4mil (100  $\mu\text{m}$ ) thick, must be laser cut, openings per drawing.

Intended for use with SAC305 Type 4 solder, reference 88.5% metals content.

Additional assembly resources available at  
<https://epc-co.com/epc/DesignSupport/AssemblyBasics.aspx>

Efficient Power Conversion Corporation (EPC) reserves the right to make changes without further notice to any products herein to improve reliability, function or design. EPC does not assume any liability arising out of the application or use of any product or circuit described herein; neither does it convey any license under its patent rights, nor the rights of others.

eGaN® is a registered trademark of Efficient Power Conversion Corporation.  
EPC Patent Listing: [epc-co.com/epc/AboutEPC/Patents.aspx](https://epc-co.com/epc/AboutEPC/Patents.aspx)

Information subject to change without notice.

Revised February, 2022