

**Vishay Siliconix** 

# Complementary N- and P-Channel 20 V (D-S) MOSFET

PRODUC	RODUCT SUMMARY					
	V <sub>DS</sub> (V)	<b>R<sub>DS(on)</sub> (</b> Ω <b>)</b>	I <sub>D</sub> (mA)			
		0.70 at V <sub>GS</sub> = 4.5 V	600			
N-Channel	20	0.85 at V <sub>GS</sub> = 2.5 V	500			
		1.25 at V <sub>GS</sub> = 1.8 V	350			
	- 20	1.2 at $V_{GS}$ = - 4.5 V	- 400			
P-Channel		1.6 at $V_{GS}$ = - 2.5 V	- 300			
		2.7 at V <sub>GS</sub> = - 1.8 V	- 150			

#### FEATURES

- Halogen-free According to IEC 61249-2-21
  Definition
- TrenchFET<sup>®</sup> Power MOSFETs
- 2000 V ESD Protection
- Very Small Footprint
- High-Side Switching
- Low On-Resistance: N-Channel, 0.7 Ω P-Channel, 1.2 Ω
- Low Threshold: ± 0.8 V (Typ.)
- Fast Switching Speed: 14 ns
- 1.8 V Operation
- Compliant to RoHS Directive 2002/95/EC

#### BENEFITS

- Ease in Driving Switches
- Low Offset (Error) Voltage
- Low-Voltage Operation
- High-Speed Circuits
- Low Battery Voltage Operation

#### **APPLICATIONS**

- Replace Digital Transistor, Level-Shifter
- Battery Operated Systems
- · Power Supply Converter Circuits

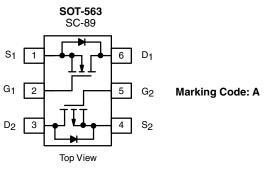
Ordering Information: Si1016X-T1-GE3 (Lead (Pb)-free and Halogen-free)

ABSOLUTE MAXIMUM RATIN	<b>IGS</b> (T <sub>A</sub> = 2	25 °C, unle	ss otherv	vise noted)				
			N-Channel P-Cha		Channel			
Parameter		Symbol	5 s	Steady State	5 s	Steady State	Unit	
Drain-Source Voltage	e Voltage V <sub>DS</sub> 20 - 20		- 20	V				
Gate-Source Voltage		V <sub>GS</sub>	as ±6		v			
Continuous Drain Current /T 150 °C)	T <sub>A</sub> = 25 °C		515	485	- 390	- 370		
Continuous Drain Current (T <sub>J</sub> = 150 °C) <sup>a</sup>	T <sub>A</sub> = 85 °C	I <sub>D</sub>	370	350	- 280	- 265		
Pulsed Drain Current <sup>b</sup>		I <sub>DM</sub>	650		- 650		mA	
Continuous Source Current (Diode Conduct	ion) <sup>a</sup>	۱ <sub>S</sub>	450	380	- 450	- 380	-	
	T <sub>A</sub> = 25 °C	Б	280	250	280	250	mW	
Maximum Power Dissipation <sup>a</sup>	T <sub>A</sub> = 85 °C	P <sub>D</sub>	145	130	145	130		
Operating Junction and Storage Temperatur	ction and Storage Temperature Range T <sub>J</sub> , T <sub>stg</sub> - 55 to 150		°C					
Gate-Source ESD Rating (HBM, Method 30	Source ESD Rating (HBM, Method 3015) ESD 2000		V					

Notes:

a. Surface mounted on FR4 board.

b. Pulse width limited by maximum junction temperature.





COMPLIANT

HALOGEN

FREE

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Parameter	Symbol	Test Conditions		Min.	Тур.	Max.	Unit	
Static				•	•			
Cata Threshold Valtage	V	$V_{DS} = V_{GS,} I_D = 250 \ \mu A$	N-Ch	0.45		1	V	
Gate Threshold Voltage	V <sub>GS(th)</sub>	$V_{DS} = V_{GS}, I_{D} = -250 \ \mu A$	P-Ch	- 0.45		- 1	V	
Gate Body Leakage	I <sub>GSS</sub>	$V_{DS} = 0 V, V_{GS} = \pm 4.5 V$	N-Ch		± 0.5	± 1.0	μΑ	
Gate Body Leakage			P-Ch		± 1.0	± 2.0		
	-	$V_{DS} = 16 V, V_{GS} = 0 V$	N-Ch		0.3	100	nA	
Zero Gate Voltage Drain		$V_{DS} = -16 V, V_{GS} = 0 V$	P-Ch		- 0.3	- 100		
Current	I <sub>DSS</sub>	$V_{DS}$ = 16 V, $V_{GS}$ = 0 V, $T_{J}$ = 85 °C	N-Ch			5	μΑ	
		$V_{DS} = -16 \text{ V}, V_{GS} = 0 \text{ V}, T_{J} = 85 ^{\circ}\text{C}$	P-Ch			- 5		
		$V_{DS} = 5 V, V_{GS} = 4.5 V$	N-Ch	700				
On State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	V <sub>DS</sub> = - 5 V, V <sub>GS</sub> = - 4.5 V	P-Ch	- 700			mA	
		V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 600 mA	N-Ch		0.41	0.70	Ω	
Drain-Source On-State Resistance <sup>a</sup>	R <sub>DS(on)</sub>	V <sub>GS</sub> = - 4.5 V, I <sub>D</sub> = - 350 mA	P-Ch		0.80	1.2		
		V <sub>GS</sub> = 2.5 V, I <sub>D</sub> = 500 mA	N-Ch		0.53	0.85		
		V <sub>GS</sub> = - 2.5 V, I <sub>D</sub> = - 300 mA	P-Ch		1.20	1.6		
		V <sub>GS</sub> = 1.8 V, I <sub>D</sub> = 350 mA	N-Ch		0.70	1.25		
		V <sub>GS</sub> = - 1.8 V, I <sub>D</sub> = - 150 mA	P-Ch		1.80	2.7		
	9 <sub>fs</sub>	$V_{DS} = 10 \text{ V}, \text{ I}_{D} = 400 \text{ mA}$	N-Ch		1.0			
Forward Transconductance <sup>a</sup>		V <sub>DS</sub> = - 10 V, I <sub>D</sub> = - 250 mA	P-Ch		0.4		S	
		I <sub>S</sub> = 150 mA, V <sub>GS</sub> = 0 V	N-Ch		0.8	1.2	V	
Diode Forward Voltage <sup>a</sup>	$V_{SD}$	I <sub>S</sub> = - 150 mA, V <sub>GS</sub> = 0 V	P-Ch		- 0.8	- 1.2		
Dynamic <sup>b</sup>								
	0		N-Ch		750			
Total Gate Charge	Qg	N-Channel	P-Ch		1500			
Gate-Source Charge	Q <sub>qs</sub>	$V_{DS}$ = 10 V, $V_{GS}$ = 4.5 V, $I_{D}$ = 250 mA	N-Ch		75		pC	
date obtilee onarge	∝gs	P-Channel	P-Ch		150		pc	
Gate-Drain Charge	Q <sub>qd</sub>	$V_{DS} = -10 \text{ V}, V_{GS} = -4.5 \text{ V}, I_D = -250 \text{ mA}$	N-Ch		225			
g-	gu		P-Ch		450			
Turn-On Time	t <sub>ON</sub>	N-Channel V <sub>DD</sub> = 10 V, R <sub>L</sub> = 47 Ω	N-Ch		5			
		$V_{DD} = 10 \text{ V}, \text{ H}_{L} = 47.02$ $I_{D} \cong 200 \text{ mA}, \text{ V}_{\text{GEN}} = 4.5 \text{ V}, \text{ H}_{a} = 10 \Omega$	P-Ch		5			
	t <sub>OFF</sub>	P-Channel	N-Ch		25		ns	
Turn-Off Time		$V_{DD} = -10 \text{ V}, \text{ R}_{L} = 47 \Omega$	P-Ch		35			
		$I_D \cong$ - 200 mA, $V_{GEN}$ = - 4.5 V, $R_q$ = 10 $\Omega$						

Notes:

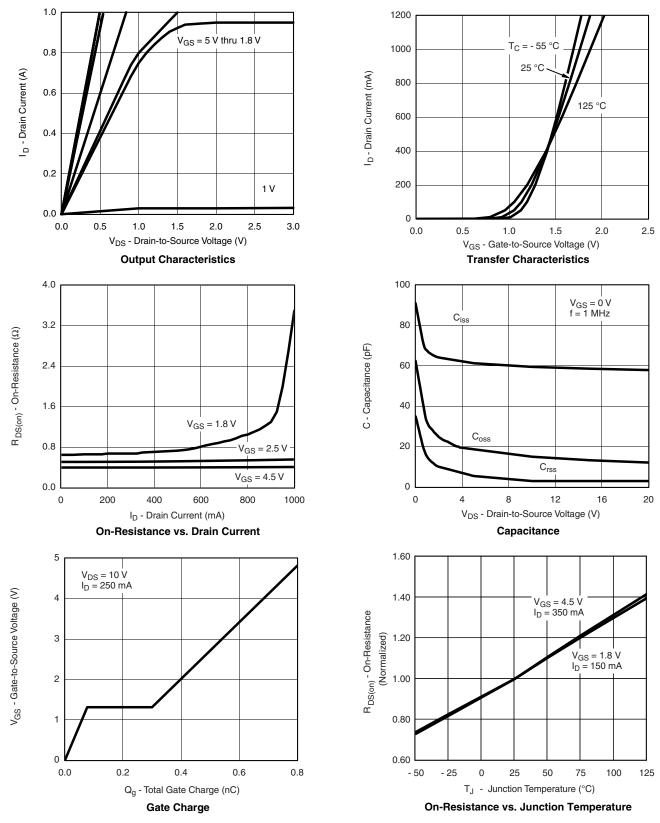
a. Pulse test; pulse width  $\leq$  300  $\mu s,$  duty cycle  $\leq$  2 %.

b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

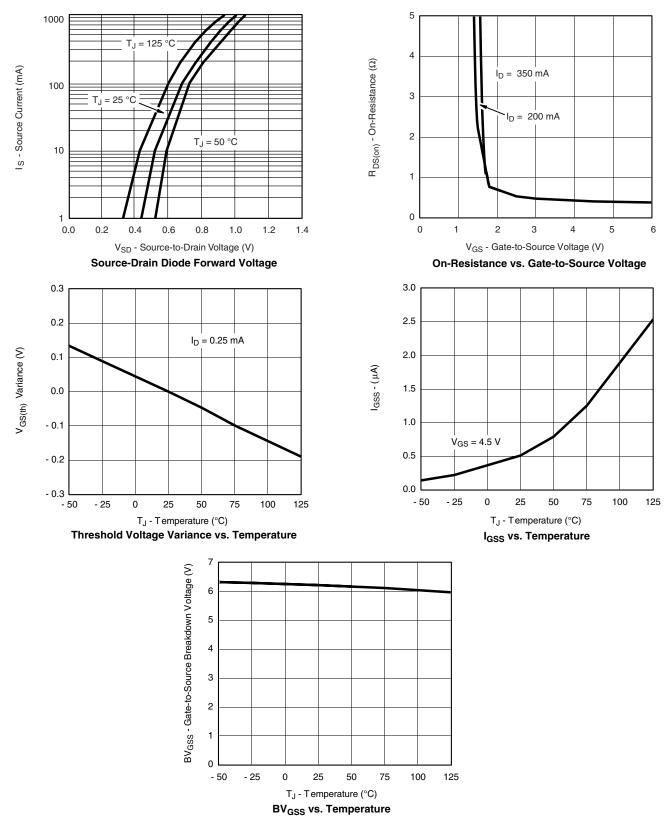


#### **N-CHANNEL TYPICAL CHARACTERISTICS** (T<sub>A</sub> = 25 °C, unless otherwise noted)





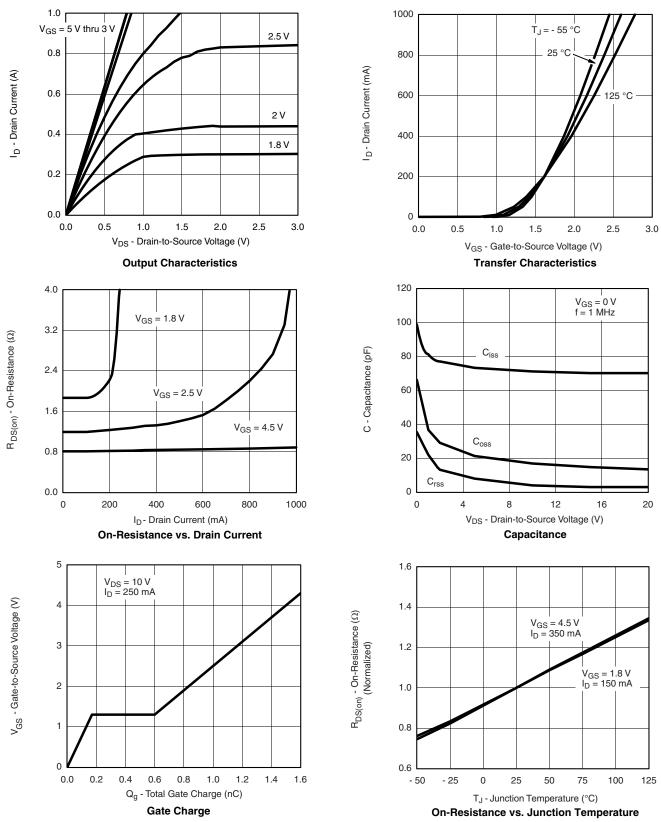
#### **N-CHANNEL TYPICAL CHARACTERISTICS** ( $T_A = 25 \text{ °C}$ , unless otherwise noted)



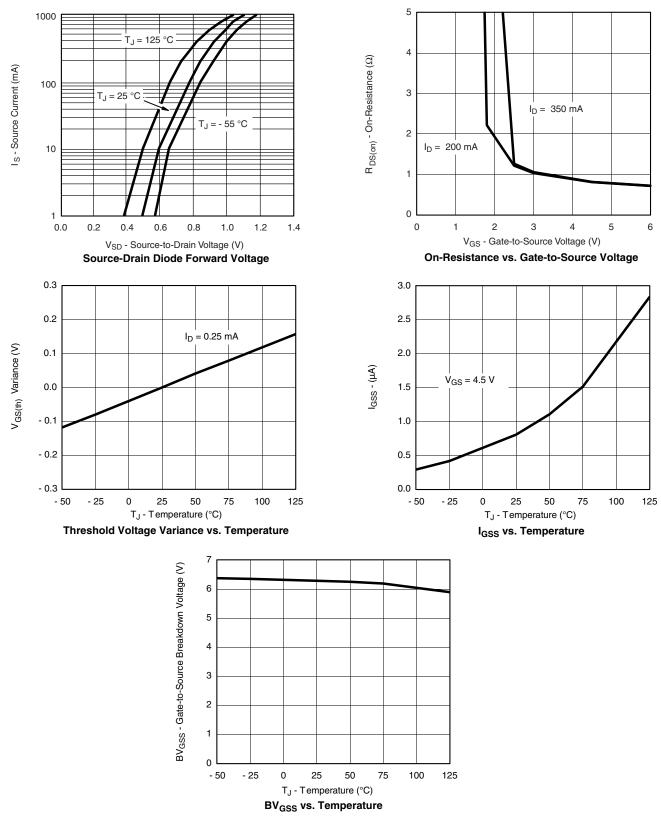


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#### **P-CHANNEL TYPICAL CHARACTERISTICS** ( $T_A = 25$ °C, unless otherwise noted)



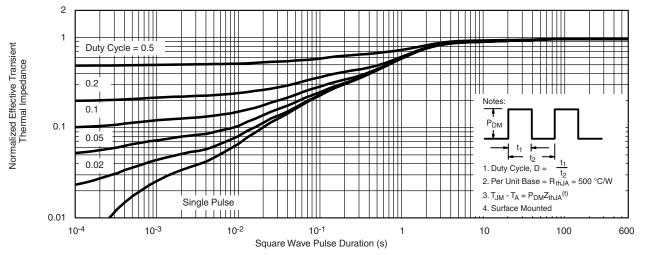




**ISHA** 



#### N- OR P-CHANNEL TYPICAL CHARACTERISTICS (T<sub>A</sub> = 25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see <a href="http://www.vishay.com/ppg271168">www.vishay.com/ppg271168</a>.



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### SC-89 6-Leads (SOT-563F)



Notes

- 1. Dimensions in millimeters.
- Dimension D does not include mold flash, protrusions or gate burrs. Mold flush, protrusions or gate burrs shall not exceed 0.15 mm per dimension E1 does not include interlead flash or protrusion, interlead flash or protrusion shall not exceed 0.15 mm per side.
- Dimensions D and E1 are determined at the outmost extremes of the plastic body exclusive of mold flash, the bar burrs, gate burrs and interlead flash, but including any mismatch between the top and the bottom of the plastic body.

A Datums A, B and D to be determined 0.10 mm from the lead tip.

 $\triangle$  Terminal numbers are shown for reference only.

These dimensions apply to the flat section of the lead between 0.08 mm and 0.15 mm from the lead tip.









DIM.		MILLIMETERS	
	MIN.	NOM.	MAX.
А	0.56	0.58	0.60
A1	0	0.02	0.10
b	0.15	0.22	0.30
С	0.10	0.14	0.18
D	1.50	1.60	1.70
E	1.50	1.60	1.70
E1	1.15	1.20	1.25
е	0.45	0.50	0.55
e1	0.95	1.00	1.05
L	0.25	0.35	0.50
L1	0.10	0.20	0.30
C14-0439-Rev DWG: 5880	v. C, 11-Aug-14		

Revision: 11-Aug-14

1 For technical questions, contact: <u>analogswitchtechsupport@vishay.com</u> Document Number: 71612

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# Application Note 826

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#### **RECOMMENDED MINIMUM PADS FOR SC-89: 6-Lead**



Recommended Minimum Pads Dimensions in Inches/(mm)

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