MOSFET - Power, Complementary, ChipFET 20 V, +5.5 A /-4.2 A

Features

- Complementary N-Channel and P-Channel MOSFET
- Small Size, 40% Smaller than TSOP-6 Package
- Leadless SMD Package Provides Great Thermal Characteristics
- Leading Edge Trench Technology for Low On Resistance
- Reduced Gate Charge to Improve Switching Response
- This is a Pb-Free Device

Applications

- DC-DC Conversion Circuits
- Load/Power Switching
- Single or Dual Cell Li-Ion Battery Supplied Devices
- Ideal for Power Management Applications in Portable, Battery Powered Products

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Parame	Symbol	Value	Unit		
Drain-to-Source Voltage			V _{DSS}	20	8
Gate-to-Source Voltage		N-Ch	V _{GS}	±8.0	V
	Ī	P-Ch		±8.0	
N-Channel Continuous Drain	Steady State	$T_A = 25^{\circ}C$	Ъ	4.0	Α
Current (Note 1)	State	T _A = 85°C	CEN	2.9	
	t ≤ 5 s	T _A = 25°C	5	5.5	
P-Channel	Steady	T _A = 25°C	I _D	3.1	Α
Continuous Drain Current (Note 1)	State	T _A = 85°C		2.2	
	t≤5s	T _A = 25°C		4.2	
Power Dissipation (Note 1)	Steady State	T _A = 25°C	P _D	1.1	W
	t ≤ 5 s			2.1	
Gate-to-Source ESD Rati (Human Body Model, M		15)	ESD	100	V

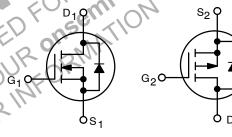
Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.



ON Semiconductor®

http://onsemi.com

V _{(BR)DSS}	R _{DS(on)} TYP	I _D MAX (Note 1)
	29 mΩ @ 4.5 V	
N-Channel 20 V	37 m Ω @ 2.5 V	5.5 A
20 1	48 mΩ @ 1.8 V	0,
	64 mΩ @ 4.5 V	
P-Channel -20 V	83 mΩ @ 2.5 V	-4.2 A
	105 mΩ @ 1.8 V	

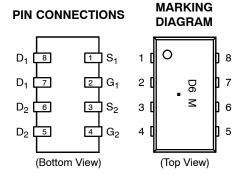


N-Channel MOSFET

P-Channel MOSFET



ChipFET CASE 1206A STYLE 2



D6 = Specific Device Code

M = Date Code

= Pb-Free Package

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 9 of this data sheet.

Surface-mounted on FR4 board using 1 in sq pad size (Cu. area = 1.127 in sq [1 oz] including traces).

MAXIMUM RATINGS (continued) (T_J = 25°C unless otherwise noted)

Parameter	Symbol	Value	Unit		
N-Channel		T _A = 25°C	I _D	3.0	Α
Continuous Drain Current (Note 3)	State	T _A = 85°C		2.2	
P-Channel	Steady	T _A = 25°C	I _D	2.3	Α
Continuous Drain Current (Note 3)	State	T _A = 85°C		1.7	
Power Dissipation (Note 3)	•	T _A = 25°C	P_{D}	0.6	W
Pulsed Drain Current	N-Ch	tp = 10 μs	I _{DM}	16	Α
	P-Ch]		12.6	
Operating Junction and Storage Temperature	•	•	T _J , T _{STG}	-55 to 150	°C
Source Current (Body Diode)	Source Current (Body Diode)				
Lead Temperature for Soldering Purposes (1/8" from case for 10 se	conds)		T_L	260	°C

THERMAL RESISTANCE RATINGS

Parameter Sy	ymbol	Max	Unit
Junction-to-Ambient - Steady State (Note 2)	$R_{ heta JA}$	110	°C/W
Junction-to-Ambient - t ≤ 5 s (Note 2)	N	60	
Junction-to-Ambient - Steady State (Note 3)		195	

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Parameter	Symbol	N/P	Test Condition	ons	Min	Тур	Max	Unit
OFF CHARACTERISTICS			OF	ON NA	1,			
Drain-to-Source Breakdown Voltage	V _{(BR)DSS}	N	V _{QS} = 0 V	I _D = 250 μA	20			V
(Note 4)		Р	VGS = 0 V	I _D = -250 μA	-20			
Drain-to-Source Breakdown Voltage Temperature Coefficient	V _{(BR)DSS} /T _J	N	0, 0, 0			20.2		mV/°C
Temperature Coefficient		P	TAUCON			16.2		
Zero Gate Voltage Drain Current	I _{DSS}	N	$V_{GS} = 0 \text{ V}, V_{DS} = 16 \text{ V}$	T _J = 25 °C			1.0	μΑ
	NOC	P	$V_{GS} = 0 \text{ V}, V_{DS} = -16 \text{ V}$	1)=25 0			-1.0	
	2 NSV	N	$V_{GS} = 0 \text{ V}, V_{DS} = 16 \text{ V}$	T _{.1} = 85 °C			5.0	
,,CF	I.E. CI	<u>a</u>	$V_{GS} = 0 \text{ V}, V_{DS} = -16 \text{ V}$	11 = 05 0			-5.0	
Gate-to-Source Leakage Current	l _{GSS}	N	$V_{DS} = 0 V, V_{GS} =$	±8.0 V			±100	nA
.60	P	Р	$V_{DS} = 0 V, V_{GS} =$	±8.0 V			±100	

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

- 2. Surface-mounted on FR4 board using 1 in sq pad size (Cu area = 1.127 in sq [1 oz] including traces).
- Surface-mounted on FR4 board using the minimum recommended pad size (Cu area = TBD in sq).
 Switching characteristics are independent of operating junction temperatures.

ELECTRICAL CHARACTERISTICS (continued) ($T_J = 25^{\circ}C$ unless otherwise noted)

Parameter	Symbol	N/P	Test Conditions		Min	Тур	Max	Unit
ON CHARACTERISTICS (Note 5)	-	- 1					-	-
Gate Threshold Voltage	V _{GS(TH)}	N		I _D = 250 μA	0.4		1.2	V
		Р	$V_{GS} = V_{DS}$	I _D = -250 μA	-0.4		-1.2	
Drain-to-Source On Resistance	R _{DS(on)}	N	V _{GS} = 4.5 V , I _D =	= 4.4 A		29	45	mΩ
		Р	V _{GS} = -4.5 V , I _D =	= -3.2 A		64	80	
		N	V _{GS} = 2.5 V , I _D =	= 4.1 A		37	50	
		Р	$V_{GS} = -2.5 \text{ V}, I_D =$	-2.5 A		83	110	
		N	V _{GS} = 1.8 V , I _D =	= 1.9 A		48	70	
		Р	V _{GS} = -1.8 V, I _D =	-0.6 A		105	150	
Forward Transconductance	9FS	N	V _{DS} = 10 V, I _D =	4.4 A		7.7		S
		Р	$V_{DS} = -10 \text{ V}$, $I_D =$	-3.2 A		5.9	Ln.	
CHARGES, CAPACITANCES AND (GATE RESISTAI	NCE				·G	0,	•
Input Capacitance	C _{ISS}	N		V _{DS} = 10 V		510		pF
		Р		$V_{DS} = -10 \text{ V}$	N,	650		
Output Capacitance	C _{OSS}	N		V _{DS} = 10 V		100		
		Р	$f = 1.0 \text{ MHz}, V_{GS} = 0 \text{ V}$ $V_{DS} = -10 \text{ V}$			100		
Reverse Transfer Capacitance	C _{RSS}	N		V _{DS} = 10 V		50		
		Р	EL	V _{DS} = -10 V	1	50		
Total Gate Charge	Q _{G(TOT)}	N	$V_{GS} = 4.5 \text{ V}, V_{DS} = 10$	V, I _D = 4.4 A		5.8	7.9	nC
		Р	$V_{GS} = -4.5 \text{ V}, V_{DS} = -10$	V, I _D = -3.2 A		6.6	8.9	
Threshold Gate Charge	Q _{G(TH)}	N	V _{GS} = 4.5 V, V _{DS} = 10	V, I _D = 4.4 A		0.96		
		P	$V_{GS} = -4.5 \text{ V}, V_{DS} = -10$	$V, I_D = -3.2 A$		0.98		
Gate-to-Source Charge	Q _{GS}	N	V _{GS} = 4.5 V, V _{DS} = 10	V, I _D = 4.4 A		1.2		
	1 70,	P	$V_{GS} = -4.5 \text{ V}, V_{DS} = -10$	$V, I_D = -3.2 A$		1.4		
Gate-to-Drain Charge	Q _{GD}	N	V _{GS} = 4.5 V, V _{DS} = 10	V, I _D = 4.4 A		1.56		
CE	ERS	P	V _{GS} = -4.5 V, V _{DS} = -10	$V, I_D = -3.2 A$		1.64		
SWITCHING CHARACTERISTICS (lote 6)							
Turn-On Delay Time	t _{d(ON)}					7.2		ns
Rise Time	t _r	N	V _{GS} = 4.5 V, V _{DD}	= 10 V,		15.9		
Turn-Off Delay Time	t _{d(OFF)}		I _D = 4.4 A, R _G =	2.5 Ω		15.7		
Fall Time	t _f					4.6		
Turn-On Delay Time	t _{d(ON)}					6.4		
Rise Time	t _r	P	$V_{GS} = -4.5 \text{ V}, V_{DD}$	= -10 V,		16.9		
Turn-Off Delay Time	t _{d(OFF)}] [$V_{GS} = -4.5 \text{ V}, V_{DD}$ $I_{D} = -3.2 \text{ A}, R_{G} =$	2.5 Ω		16.4		
Fall Time	t _f					15.0		

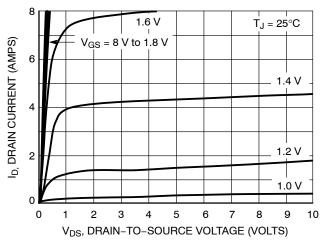
^{5.} Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.
6. Switching characteristics are independent of operating junction temperatures.

ELECTRICAL CHARACTERISTICS (continued) (T_J = 25°C unless otherwise noted)

Parameter	Symbol	N/P	Test Conditions			Тур	Max	Unit
DRAIN-SOURCE DIODE CHARACTE	RISTICS							
Forward Diode Voltage	V _{SD}	N		I _S = 1.7 A		0.68	1.2	V
		Р	V_{GS} = 0 V, T_J = 25 °C	I _S = -1.7 A		-0.7	-1.2	
Reverse Recovery Time	t _{RR}	N		I _S = 1.7 A		13.5		ns
		Р		I _S = -1.7 A		12.6		
Charge Time	t _a	N		I _S = 1.7 A		8.6		
		Р	V _{GS} = 0 V,	I _S = -1.7 A		8.4		
Discharge Time	t _b	N	V_{GS} = 0 V, dI _S / dt = 100 A/ μ s	I _S = 1.7 A		4.9		
		Р		I _S = -1.7 A		4.2		
Reverse Recovery Charge	Q_{RR}	N		I _S = 1.7 A		7.0		nC
		Р		I _S = -1.7 A		6.0	190	
OEVICE P	NOTE	RECO	OMMENDED OMNENDED OMTACTORIN ATIVE FOR IN	FOR MA				

TYPICAL N-CHANNEL PERFORMANCE CURVES

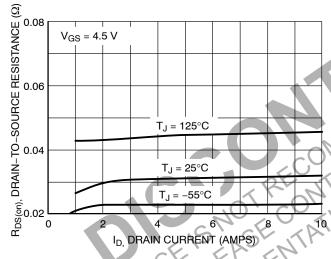
(T_J = 25°C unless otherwise noted)



8
(SdWe)
6
4
2
25°C
T_J = -55°C
0
0
0.4
0.8
1.2
1.6
2.0
V_{GS}, GATE-TO-SOURCE VOLTAGE (VOLTS)

Figure 1. On-Region Characteristics

Figure 2. Transfer Characteristics



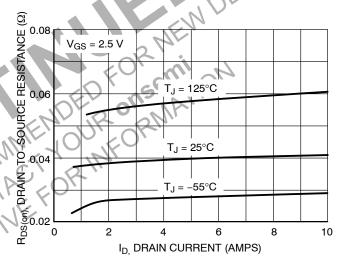
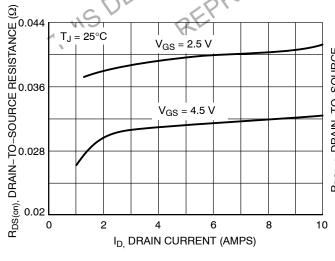


Figure 3. On-Resistance vs. Drain Current

Figure 4. On-Resistance vs. Drain Current and Temperature



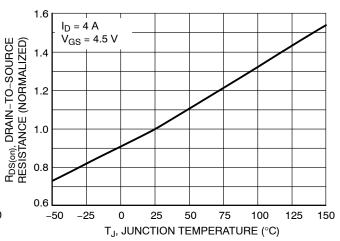
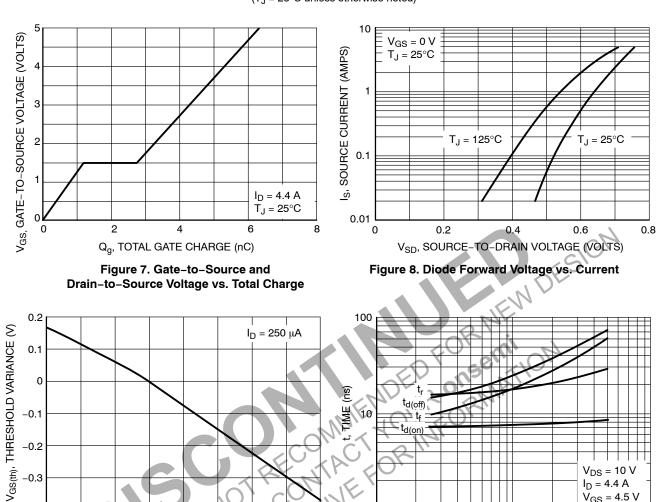


Figure 5. On-Resistance vs. Drain Current

Figure 6. On–Resistance Variation with Temperature

TYPICAL N-CHANNEL PERFORMANCE CURVES

(T_J = 25°C unless otherwise noted)



T_J, JUNCTION TEMPERATURE (°C)

100

Figure 10. Resistive Switching Time Variation vs. Gate Resistance

10

R_G, GATE RESISTANCE (OHMS)

 V_{GS} = 4.5 V

100

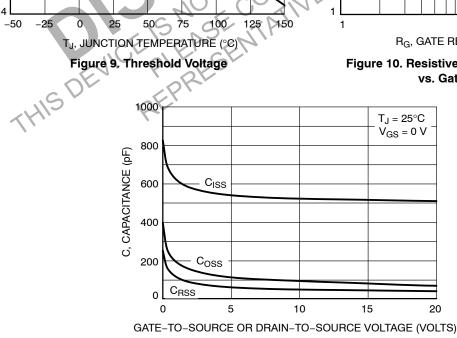
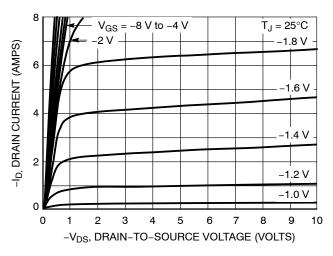


Figure 11. Capacitance Variation

TYPICAL P-CHANNEL PERFORMANCE CURVES

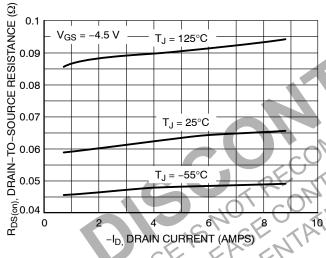
(T_J = 25°C unless otherwise noted)



(Sdwe) Living 4 2 25°C T_J = -55°C 0 0 0.4 0.8 1.2 1.6 2.0 2.4 2.8 -V_{GS}, GATE-TO-SOURCE VOLTAGE (VOLTS)

Figure 12. On-Region Characteristics

Figure 13. Transfer Characteristics



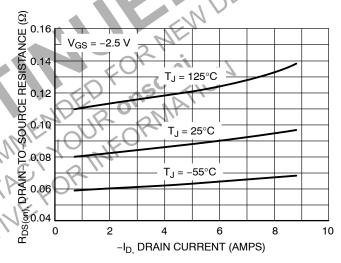
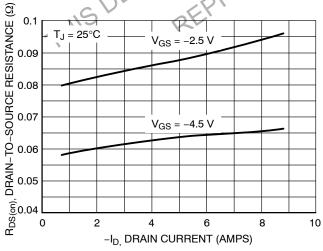


Figure 14. On-Resistance vs. Drain Current

Figure 15. On–Resistance vs. Drain Current and Temperature



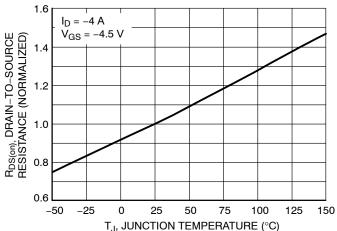


Figure 16. On-Resistance vs. Drain Current

Figure 17. On–Resistance Variation with Temperature

TYPICAL P-CHANNEL PERFORMANCE CURVES

 $(T_J = 25^{\circ}C \text{ unless otherwise noted})$

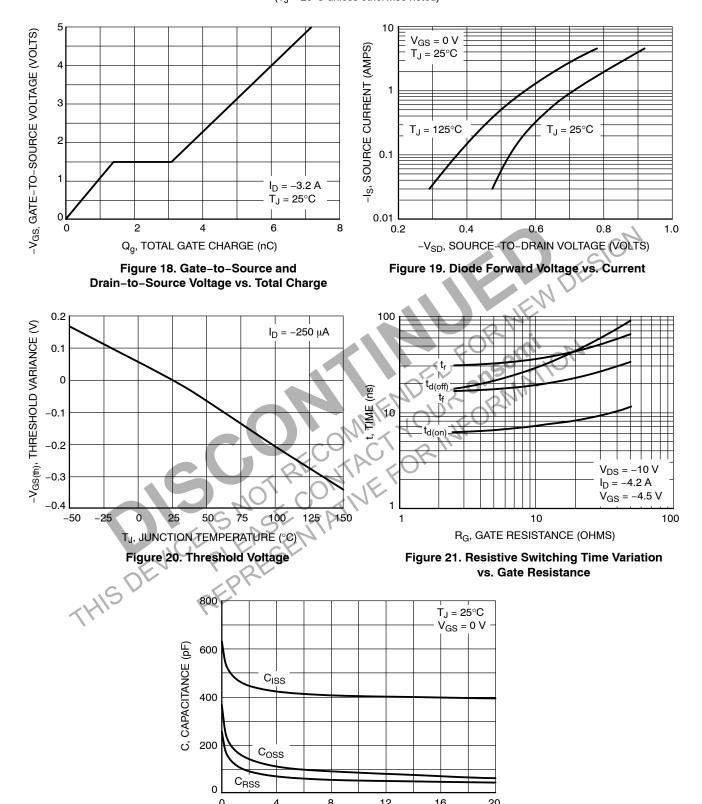


Figure 22. Capacitance Variation

GATE-TO-SOURCE OR DRAIN-TO-SOURCE VOLTAGE (VOLTS)

TYPICAL PERFORMANCE CURVES

(T_J = 25°C unless otherwise noted)

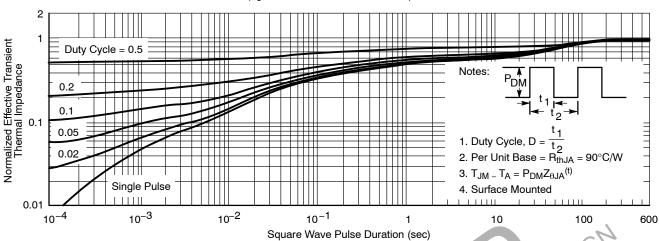


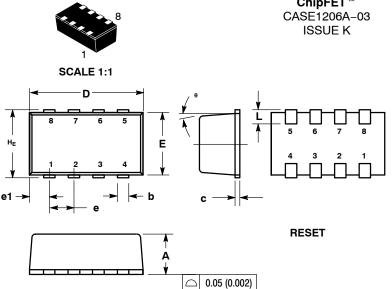
Figure 23. Thermal Response

ORDERING INFORMATION

Device	Package	Shipping [†]
NTHD3102CT1G	ChipFET (Pb-Fr(ee)	3000 Tape & Reel
†For information on tape and reel specifications, in Specification Brochure, BRD8011/D.		please refer to our Tape and Reel Packaging
THIS I RET		

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.





ChipFET™

DATE 19 MAY 2009

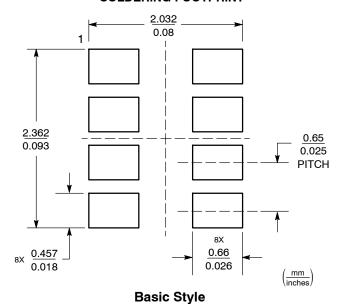
NOTES:

- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982. CONTROLLING DIMENSION: MILLIMETER.
- MOLD GATE BURRS SHALL NOT EXCEED 0.13 MM PER SIDE. LEADFRAME TO MOLDED BODY OFFSET IN HORIZONTAL
- AND VERTICAL SHALL NOT EXCEED 0.08 MM.
 DIMENSIONS A AND B EXCLUSIVE OF MOLD GATE BURRS.
- NO MOLD FLASH ALLOWED ON THE TOP AND BOTTOM LEAD SURFACE.

	MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
Α	1.00	1.05	1.10	0.039	0.041	0.043
b	0.25	0.30	0.35	0.010	0.012	0.014
С	0.10	0.15	0.20	0.004	0.006	0.008
D	2.95	3.05	3.10	0.116	0.120	0.122
E	1.55	1.65	1.70	0.061	0.065	0.067
е	0.65 BSC				0.025 BSC	
e1		0.55 BSC			0.022 BSC	
L	0.28	0.35	0.42	0.011	0.014	0.017
HE	1.80	1.90	2.00	0.071	0.075	0.079
θ		5° NOM			5° NOM	

STYLE 1:	STYLE 2:	STYLE 3:	STYLE 4:	STYLE 5:	STYLE 6:
PIN 1. DRAIN	PIN 1. SOURCE 1	PIN 1. ANODE	PIN 1. COLLECTOR	PIN 1. ANODE	PIN 1. ANODE
DRAIN	2. GATE 1	2. ANODE	2. COLLECTOR	ANODE	2. DRAIN
DRAIN	SOURCE 2	SOURCE	COLLECTOR	DRAIN	3. DRAIN
GATE	4. GATE 2	4. GATE	4. BASE	DRAIN	4. GATE
SOURCE	5. DRAIN 2	5. DRAIN	EMITTER	SOURCE	5. SOURCE
DRAIN	6. DRAIN 2	6. DRAIN	COLLECTOR	GATE	6. DRAIN
DRAIN	7. DRAIN 1	CATHODE	COLLECTOR	CATHODE	7. DRAIN
8. DRAIN	8. DRAIN 1	CATHODE	COLLECTOR	CATHODE	8. CATHODE / DRAIN

SOLDERING FOOTPRINT



GENERIC MARKING DIAGRAM*



XXX = Specific Device Code

М = Month Code = Pb-Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

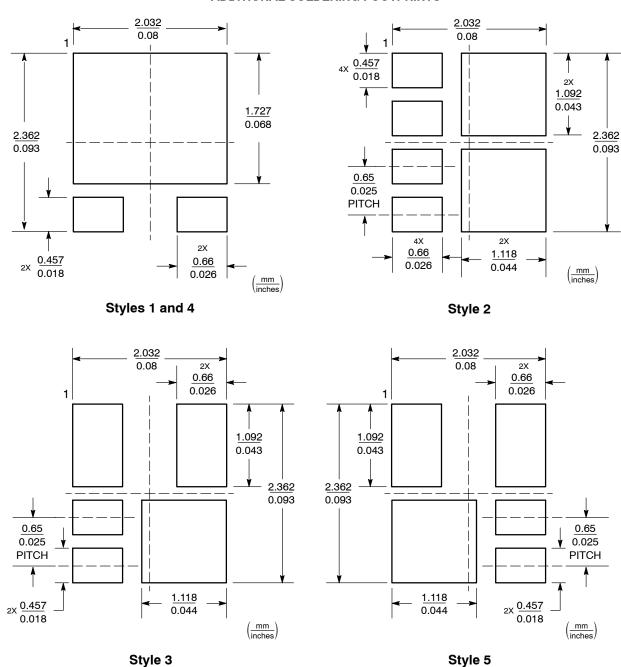
OPTIONAL SOLDERING FOOTPRINTS ON PAGE 2

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DATE 19 MAY 2009

ADDITIONAL SOLDERING FOOTPRINTS*



*For additional information on our Pb-Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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