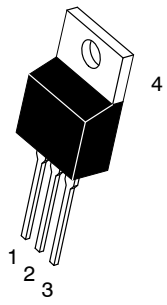
High Voltage NPN Silicon Power Transistors

TIP47G, TIP48G, TIP50G

This series is designed for line operated audio output amplifier, SWITCHMODE power supply drivers and other switching applications.

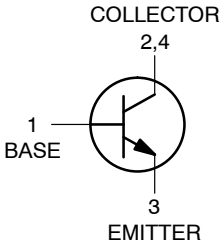
Features

- Popular TO−220 Plastic Package
- Complementary to the MJE5730 and MJE5731 Series
- These Devices are Pb−Free and are RoHS Compliant*



TO−220AB
CASE 221A
STYLE 1

1.0 AMPERE
POWER TRANSISTORS
NPN SILICON
250 − 300 − 400 VOLTS
40 WATTS



MAXIMUM RATINGS

Symbol	Rating	TIP47	TIP48	TIP50	Unit
V_{CEO}	Collector − Emitter Voltage	250	300	400	Vdc
V_{CB}	Collector − Base Voltage	350	400	500	Vdc
V_{EB}	Emitter − Base Voltage	5.0			Vdc
I_C	Collector Current − Continuous	1.0			Adc
I_{CM}	Collector Current − Peak	2.0			Adc
I_B	Base Current	0.6			Adc
P_D	Total Power Dissipation @ T_C = 25°C Derate above 25°C	40 0.32			W W/°C
P_D	Total Power Dissipation @ T_C = 25°C Derate above 25°C	2.0 0.016			W W/°C
E	Unclamped Inducting Load Energy (See Figure 8)	20			mJ
T_J, T_{stg}	Operating and Storage Junction Temperature Range	−65 to +150			°C

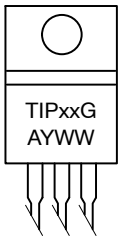
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS

Symbol	Characteristic	Max	Unit
$R_{\theta JC}$	Thermal Resistance, Junction−to−Case	3.125	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction−to−Ambient	62.5	°C/W

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

MARKINGDIAGRAM



TIPxx	= Device Code
xx	= 47, 48, or 50
A	= Assembly Location
Y	= Year
WW	= Work Week
G	= Pb−Free Package

ORDERING INFORMATION

See detailed ordering and shipping information on page 5 of this data sheet.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Symbol	Characteristic		Min	Max	Unit
OFF CHARACTERISTICS					
$V_{CEO(sus)}$	Collector−Emitter Sustaining Voltage (Note 1) (I_C = 30 mAdc, I_B = 0)	TIP47 TIP48 TIP50	250 300 400	– – –	Vdc
I_{CEO}	Collector Cutoff Current (V_{CE} = 150 Vdc, I_B = 0) (V_{CE} = 200 Vdc, I_B = 0) (V_{CE} = 300 Vdc, I_B = 0)	 TIP47 TIP48 TIP50	 – – –	 1.0 1.0 1.0	mAdc
I_{CES}	Collector Cutoff Current (V_{CE} = 350 Vdc, V_{BE} = 0) (V_{CE} = 400 Vdc, V_{BE} = 0) (V_{CE} = 500 Vdc, V_{BE} = 0)	 TIP47 TIP48 TIP50	 – – –	 1.0 1.0 1.0	mAdc
I_{EBO}	Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		–	1.0	mAdc
ON CHARACTERISTICS (Note 1)					
h_{FE}	DC Current Gain (I_C = 0.3 Adc, V_{CE} = 10 Vdc) (I_C = 1.0 Adc, V_{CE} = 10 Vdc)		 30 10	 150 –	–
$V_{CE(sat)}$	Collector−Emitter Saturation Voltage (I_C = 1.0 Adc, I_B = 0.2 Adc)		–	1.0	Vdc
$V_{BE(on)}$	Base−Emitter On Voltage (I_C = 1.0 Adc, V_{CE} = 10 Vdc)		–	1.5	Vdc
DYNAMIC CHARACTERISTICS					
f_T	Current−Gain − Bandwidth Product (I_C = 0.1 Adc, V_{CE} = 10 Vdc, f = 2.0 MHz)		10	–	MHz
h_{fe}	Small−Signal Current Gain (I_C = 0.2 Adc, V_{CE} = 10 Vdc, f = 1.0 kHz)		25	–	–

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

1. Pulse Test: Pulse width ≤ 300 μs, Duty Cycle ≤ 2.0%.

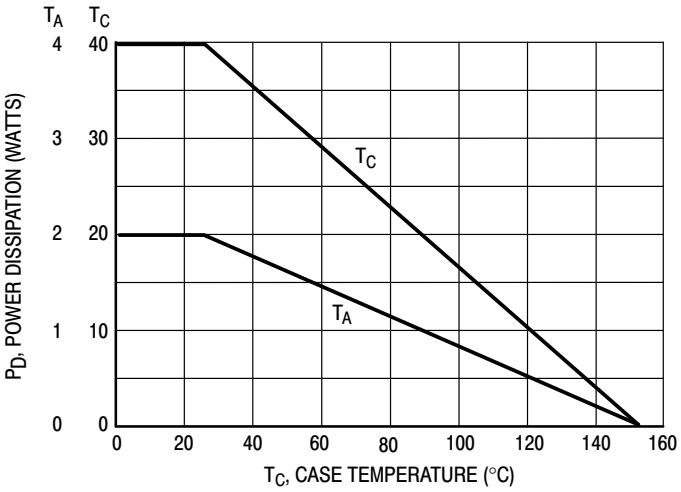


Figure 1. Power Derating

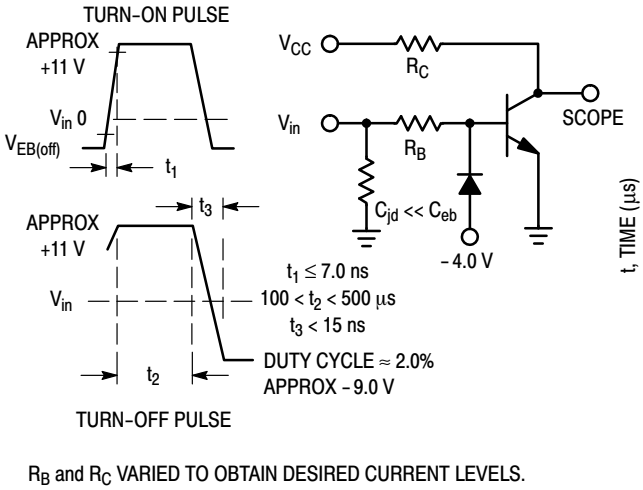


Figure 2. Switching Time Equivalent Circuit

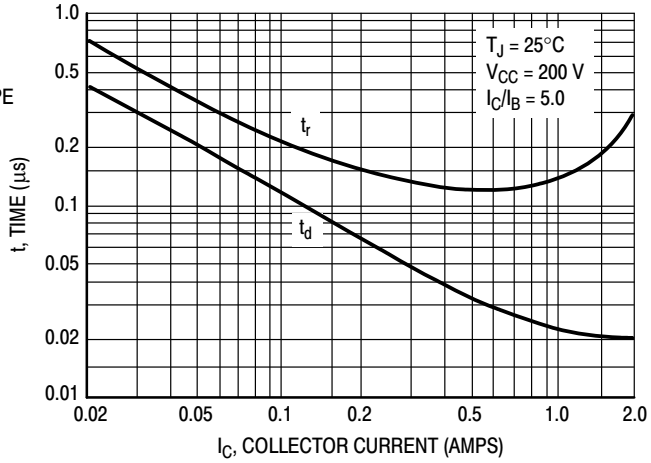


Figure 3. Turn−On Time

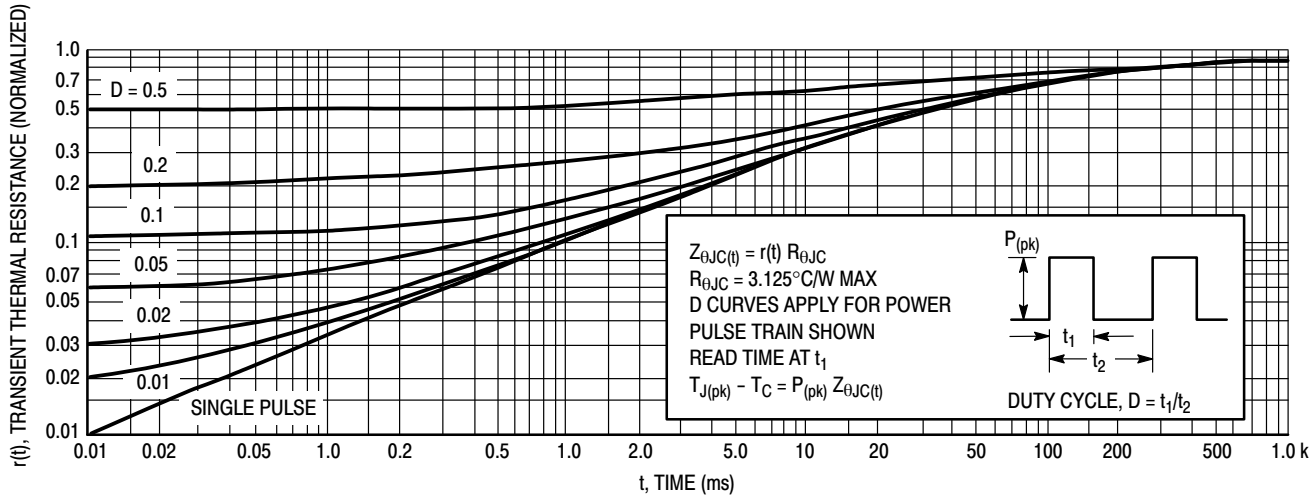


Figure 4. Thermal Response

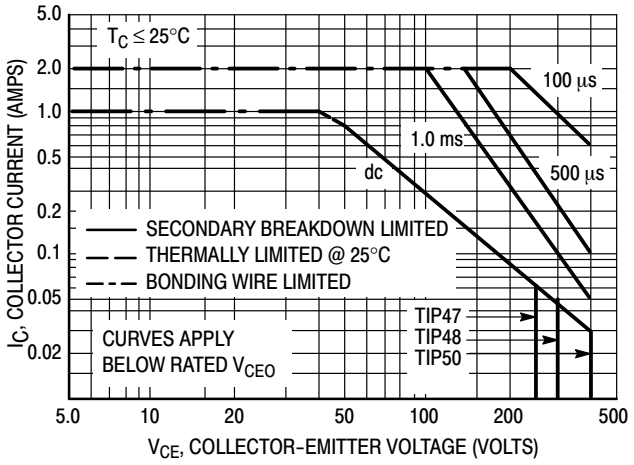


Figure 5. Active Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 150°C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \le 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

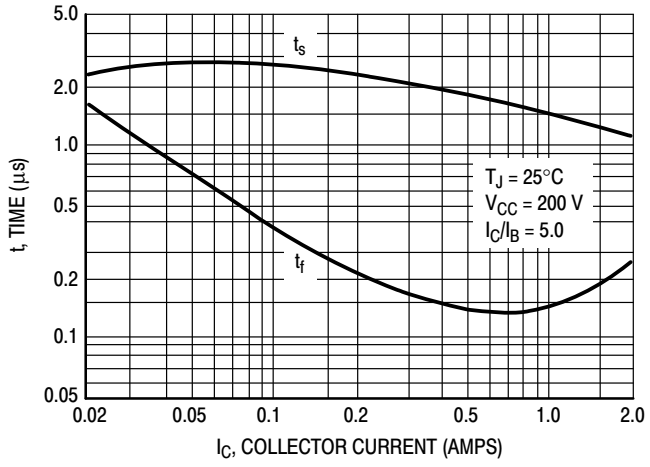


Figure 6. Turn−Off Time

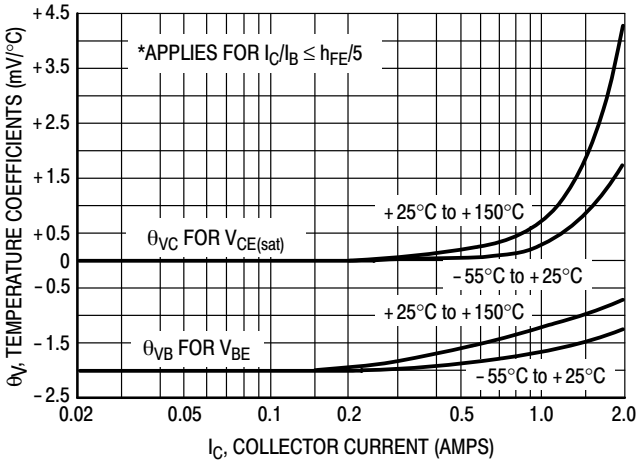
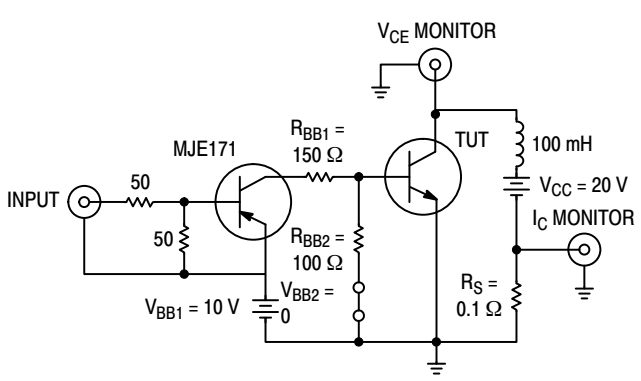
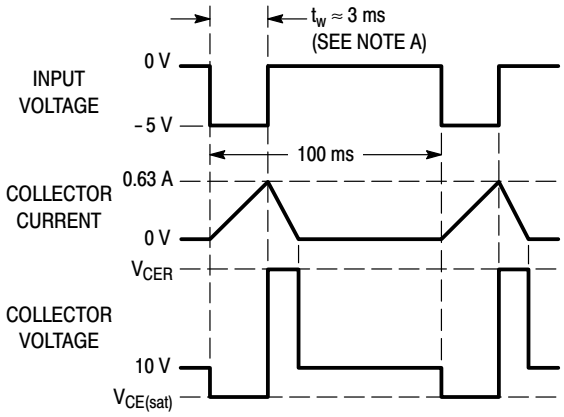


Figure 7. Temperature Coefficients





Note A: Input pulse width is increased until $I_{CM} = 0.63$ A.

Figure 8. Inductive Load Switching

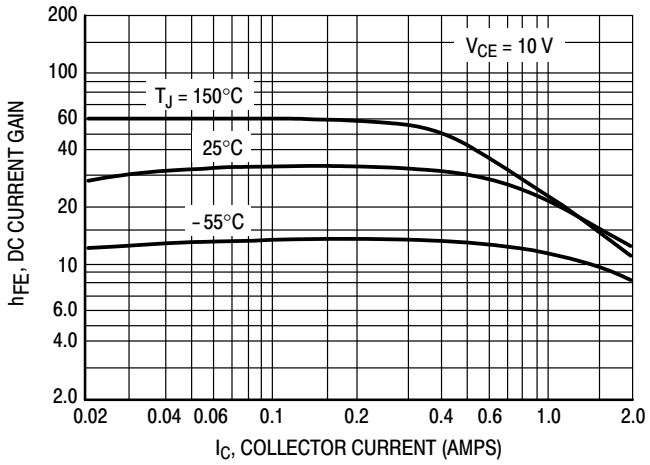


Figure 9. DC Current Gain

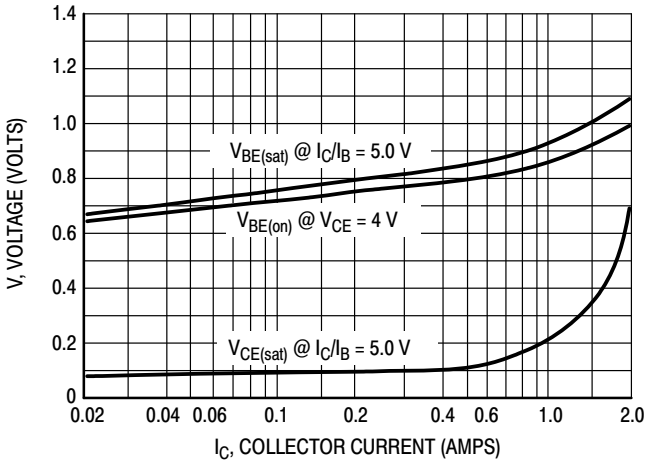


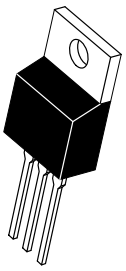
Figure 10. "On" Voltages

ORDERING INFORMATION

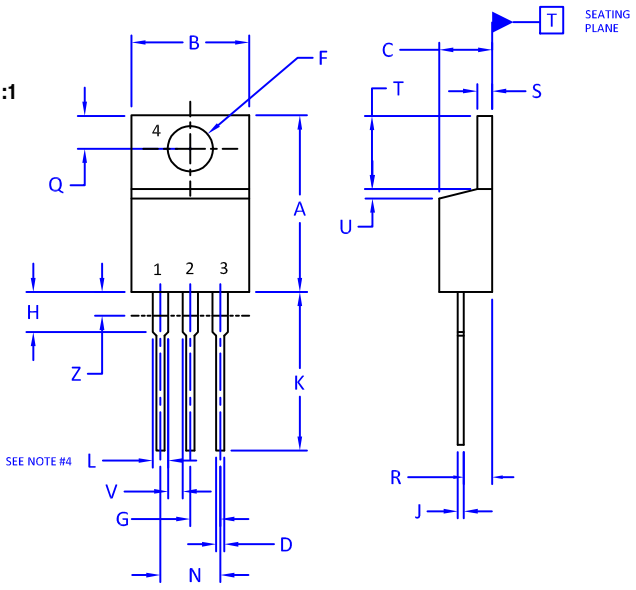
Device	Package	Shipping
TIP47G	TO−220 (Pb−Free)	50 Units / Rail
TIP48G	TO−220 (Pb−Free)	50 Units / Rail
TIP49G	TO−220 (Pb−Free)	50 Units / Rail
TIP50G	TO−220 (Pb−Free)	50 Units / Rail

TO−220
CASE 221A
ISSUE AK

DATE 13 JAN 2022



SCALE 1:1



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 2009.
2. CONTROLLING DIMENSION: INCHES
3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.
4. MAX WIDTH FOR F102 DEVICE = 1.35MM

	INCHES		MILLIMETERS	
DIM	MIN.	MAX.	MIN.	MAX.
A	0.570	0.620	14.48	15.75
B	0.380	0.415	9.66	10.53
C	0.160	0.190	4.07	4.83
D	0.025	0.038	0.64	0.96
F	0.142	0.161	3.60	4.09
G	0.095	0.105	2.42	2.66
H	0.110	0.161	2.80	4.10
J	0.014	0.024	0.36	0.61
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.15	1.52
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.110	2.04	2.79
S	0.045	0.055	1.15	1.41
T	0.235	0.255	5.97	6.47
U	0.000	0.050	0.00	1.27
V	0.045	----	1.15	---
Z	----	0.080	---	2.04

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 2:
PIN 1. BASE
2. EMITTER
3. COLLECTOR
4. EMITTER

STYLE 3:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

STYLE 4:
PIN 1. MAIN TERMINAL 1
2. MAIN TERMINAL 2
3. GATE
4. MAIN TERMINAL 2

STYLE 5:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

STYLE 6:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. CATHODE

STYLE 7:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. ANODE

STYLE 8:
PIN 1. CATHODE
2. ANODE
3. EXTERNAL TRIP/DELAY
4. ANODE

STYLE 9:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 10:
PIN 1. GATE
2. SOURCE
3. DRAIN
4. SOURCE

STYLE 11:
PIN 1. DRAIN
2. SOURCE
3. GATE
4. SOURCE

STYLE 12:
PIN 1. MAIN TERMINAL 1
2. MAIN TERMINAL 2
3. GATE
4. NOT CONNECTED

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DESCRIPTION:	**TO−220**	**PAGE 1 OF 1**

ADDITIONAL INFORMATION

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Technical Library: www.onsemi.com/design/resources/technical−documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support
For additional information, please contact your local Sales Representative at www.onsemi.com/support/sales