

NST3906DXV6T1, NST3906DXV6T5

Dual General Purpose Transistor

The NST3906DXV6T1 device is a spin-off of our popular SOT-23/SOT-323 three-leaded device. It is designed for general purpose amplifier applications and is housed in the SOT-563 six-leaded surface mount package. By putting two discrete devices in one package, this device is ideal for low-power surface mount applications where board space is at a premium.

- h_{FE} , 100-300
- Low $V_{CE(sat)}$, ≤ 0.4 V
- Simplifies Circuit Design
- Reduces Board Space
- Reduces Component Count
- Lead-Free Solder Plating

MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
|--------------------------------|-----------|-----------------------|------|
| Collector- Emitter Voltage | V_{CEO} | -40 | Vdc |
| Collector- Base Voltage | V_{CBO} | -40 | Vdc |
| Emitter- Base Voltage | V_{EBO} | -5.0 | Vdc |
| Collector Current - Continuous | I_C | -200 | mAdc |
| Electrostatic Discharge | ESD | HBM>16000, MM>2000 | V |

THERMAL CHARACTERISTICS

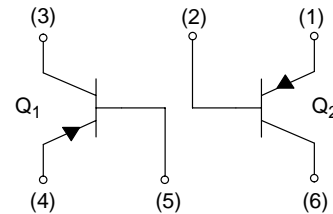
| Characteristic (One Junction Heated) | Symbol | Max | Unit |
|--|-----------------|------------------------------------|----------------------------|
| Total Device Dissipation $T_A = 25^\circ\text{C}$ Derate above 25°C | P_D | 357 (Note 1) 2.9 (Note 1) | mW mW/ $^\circ\text{C}$ |
| Thermal Resistance Junction-to-Ambient | $R_{\theta JA}$ | 350 (Note 1) | $^\circ\text{C}/\text{W}$ |
| Characteristic (Both Junctions Heated) | Symbol | Max | Unit |
| Total Device Dissipation $T_A = 25^\circ\text{C}$ Derate above 25°C | P_D | 500 (Note 1) 4.0 (Note 1) | mW mW/ $^\circ\text{C}$ |
| Thermal Resistance Junction-to-Ambient | $R_{\theta JA}$ | 250 (Note 1) | $^\circ\text{C}/\text{W}$ |
| Junction and Storage Temperature Range | T_J, T_{stg} | - 55 to +150 | $^\circ\text{C}$ |

1. FR-4 @ Minimum Pad

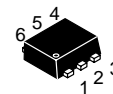


ON Semiconductor®

<http://onsemi.com>



NST3906DXV6T1



SOT-563
CASE 463A
PLASTIC

MARKING DIAGRAM



A2 = Specific Device Code
D = Date Code

ORDERING INFORMATION

| Device | Package | Shipping |
|---------------|---------|--------------------------------|
| NST3906DXV6T1 | SOT-563 | 4 mm pitch 4000/Tape & Reel |
| NST3906DXV6T5 | SOT-563 | 2 mm pitch 8000/Tape & Reel |

NST3906DXV6T1, NST3906DXV6T5

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

| Characteristic | Symbol | Min | Max | Unit |
|----------------|--------|-----|-----|------|
|----------------|--------|-----|-----|------|

OFF CHARACTERISTICS

| | | | | |
|--|----------------------|------|-----|------|
| Collector - Emitter Breakdown Voltage (Note 2) | V _{(BR)CEO} | -40 | - | Vdc |
| Collector - Base Breakdown Voltage | V _{(BR)CBO} | -40 | - | Vdc |
| Emitter - Base Breakdown Voltage | V _{(BR)EBO} | -5.0 | - | Vdc |
| Base Cutoff Current | I _{BL} | - | -50 | nAdc |
| Collector Cutoff Current | I _{CEX} | - | -50 | nAdc |

ON CHARACTERISTICS (Note 2)

| | | | | |
|---|----------------------|-----------------------------|-------------------------|-----------------------|
| DC Current Gain (I _C = -0.1 mAdc, V _{CE} = -1.0 Vdc) (I _C = -1.0 mAdc, V _{CE} = -1.0 Vdc) (I _C = -10 mAdc, V _{CE} = -1.0 Vdc) (I _C = -50 mAdc, V _{CE} = -1.0 Vdc) (I _C = -100 mAdc, V _{CE} = -1.0 Vdc) | h _{FE} | 60 80 100 60 30 | - - 300 - - | - - - - - |
| Collector - Emitter Saturation Voltage (I _C = -10 mAdc, I _B = -1.0 mAdc) (I _C = -50 mAdc, I _B = -5.0 mAdc) | V _{CE(sat)} | - - | -0.25 -0.4 | Vdc |
| Base - Emitter Saturation Voltage (I _C = -10 mAdc, I _B = -1.0 mAdc) (I _C = -50 mAdc, I _B = -5.0 mAdc) | V _{BE(sat)} | -0.65 - | -0.85 -0.95 | Vdc |

SMALL- SIGNAL CHARACTERISTICS

| | | | | |
|---|------------------|-----|------|--------------------|
| Current - Gain - Bandwidth Product | f _T | 250 | - | MHz |
| Output Capacitance | C _{obo} | - | 4.5 | pF |
| Input Capacitance | C _{ibo} | - | 10.0 | pF |
| Input Impedance (V _{CE} = -10 Vdc, I _C = -1.0 mAdc, f = 1.0 kHz) | h _{ie} | 2.0 | 12 | k Ω |
| Voltage Feedback Ratio (V _{CE} = -10 Vdc, I _C = -1.0 mAdc, f = 1.0 kHz) | h _{re} | 0.1 | 10 | X 10 ⁻⁴ |
| Small - Signal Current Gain (V _{CE} = -10 Vdc, I _C = -1.0 mAdc, f = 1.0 kHz) | h _{fe} | 100 | 400 | - |
| Output Admittance (V _{CE} = -10 Vdc, I _C = -1.0 mAdc, f = 1.0 kHz) | h _{oe} | 3.0 | 60 | μmhos |
| Noise Figure (V _{CE} = -5.0 Vdc, I _C = -100 μAdc, R _S = 1.0 k Ω, f = 1.0 kHz) | NF | - | 4.0 | dB |

SWITCHING CHARACTERISTICS

| | | | | | |
|--------------|--|----------------|---|-----|----|
| Delay Time | (V _{CC} = -3.0 Vdc, V _{BE} = 0.5 Vdc) | t _d | - | 35 | ns |
| Rise Time | (I _C = -10 mAdc, I _{B1} = -1.0 mAdc) | t _r | - | 35 | |
| Storage Time | (V _{CC} = -3.0 Vdc, I _C = -10 mAdc) | t _s | - | 225 | ns |
| Fall Time | (I _{B1} = I _{B2} = -1.0 mAdc) | t _f | - | 75 | |

2. Pulse Test: Pulse Width ≤ 300 μs; Duty Cycle ≤ 2.0%.

NST3906DXV6T1, NST3906DXV6T5

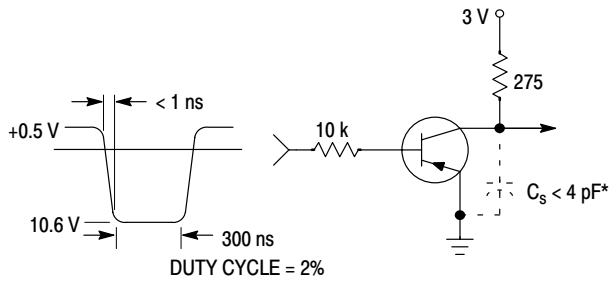


Figure 1. Delay and Rise Time Equivalent Test Circuit

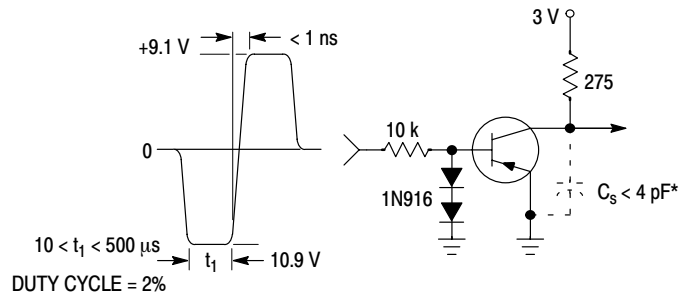


Figure 2. Storage and Fall Time Equivalent Test Circuit

* Total shunt capacitance of test jig and connectors

TYPICAL TRANSIENT CHARACTERISTICS

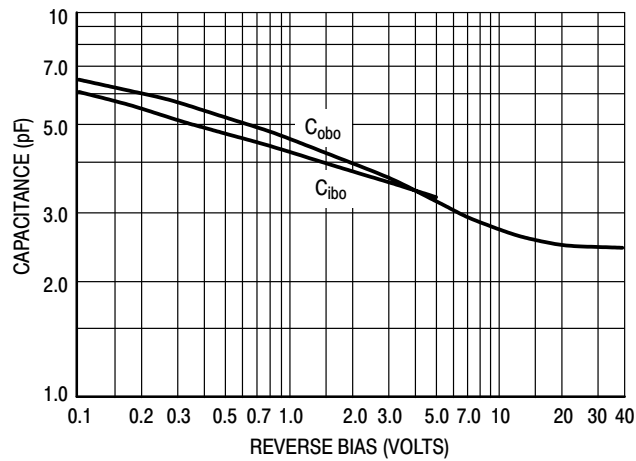


Figure 3. Capacitance

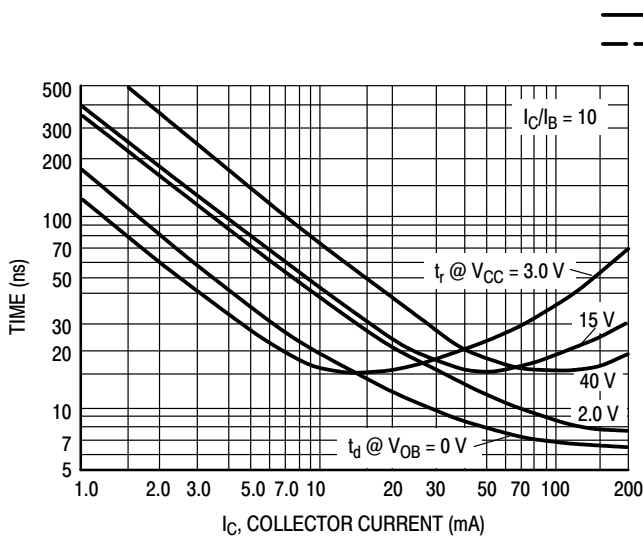


Figure 4. Turn-On Time

— $T_J = 25^\circ\text{C}$
 - - - $T_J = 125^\circ\text{C}$

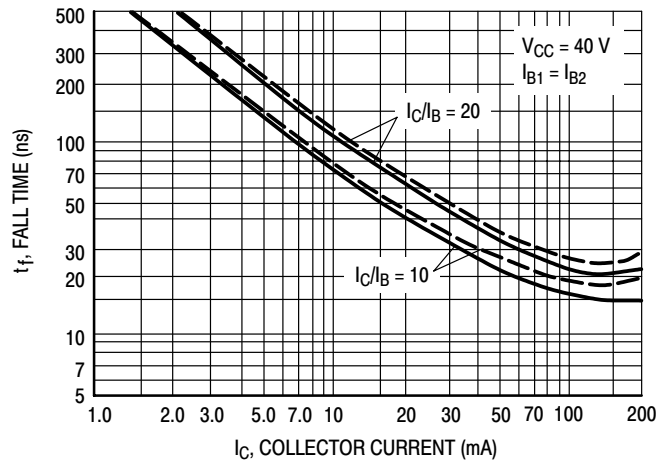


Figure 5. Fall Time

NST3906DXV6T1, NST3906DXV6T5

TYPICAL AUDIO SMALL-SIGNAL CHARACTERISTICS NOISE FIGURE VARIATIONS

($V_{CE} = -5.0$ Vdc, $T_A = 25^\circ\text{C}$, Bandwidth = 1.0 Hz)

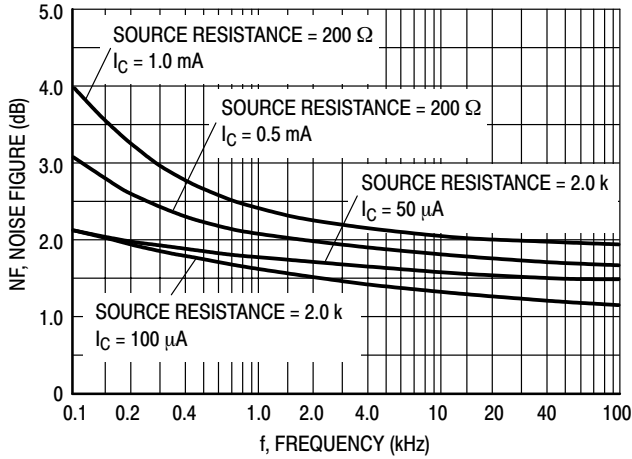


Figure 6.

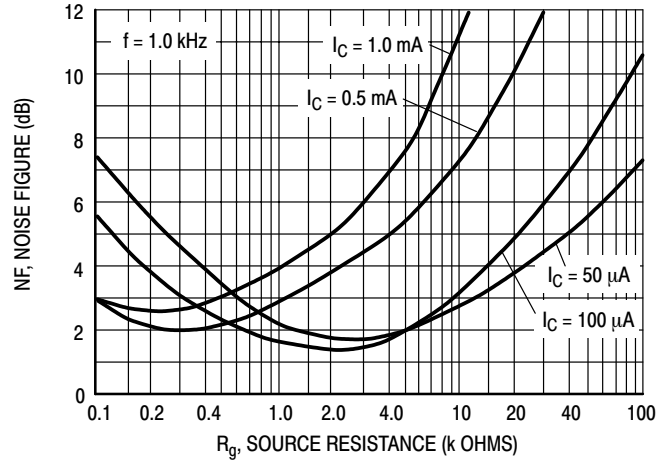


Figure 7.

h PARAMETERS

($V_{CE} = -10$ Vdc, $f = 1.0$ kHz, $T_A = 25^\circ\text{C}$)

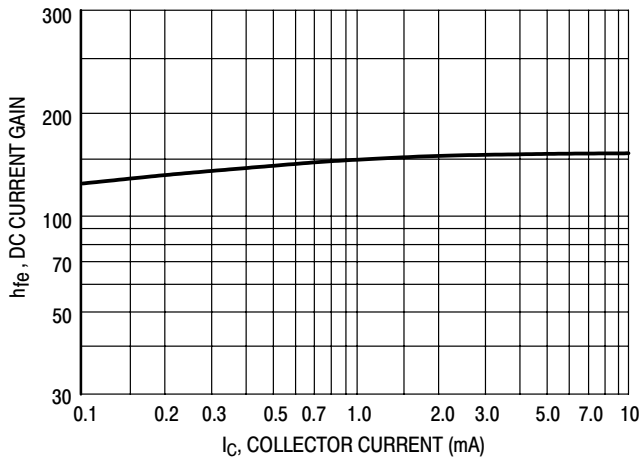


Figure 8. Current Gain

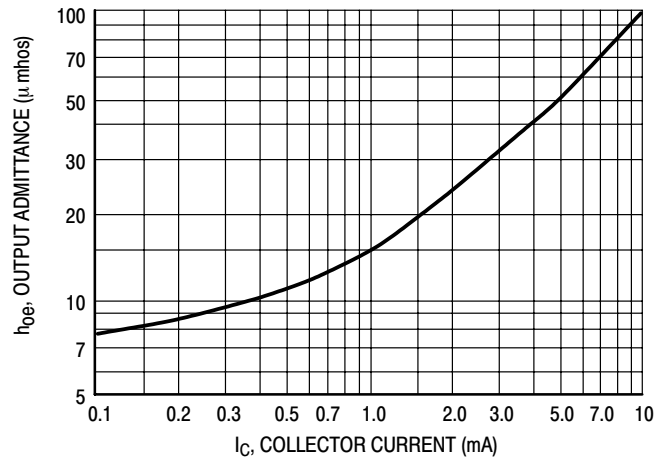


Figure 9. Output Admittance

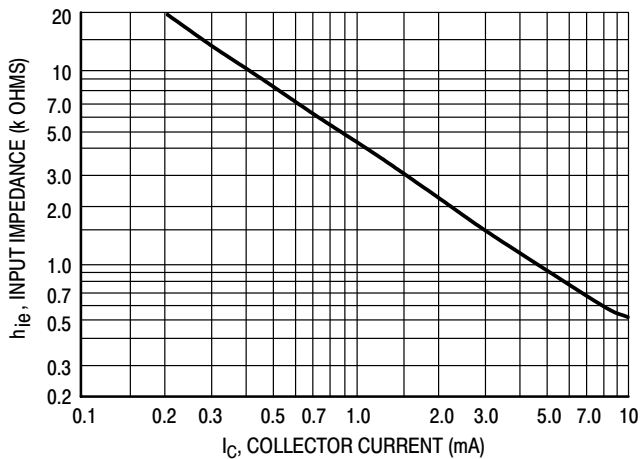


Figure 10. Input Impedance

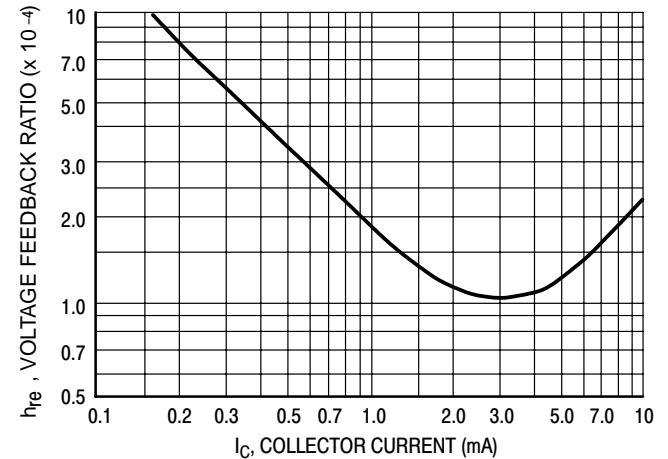


Figure 11. Voltage Feedback Ratio

NST3906DXV6T1, NST3906DXV6T5

TYPICAL STATIC CHARACTERISTICS

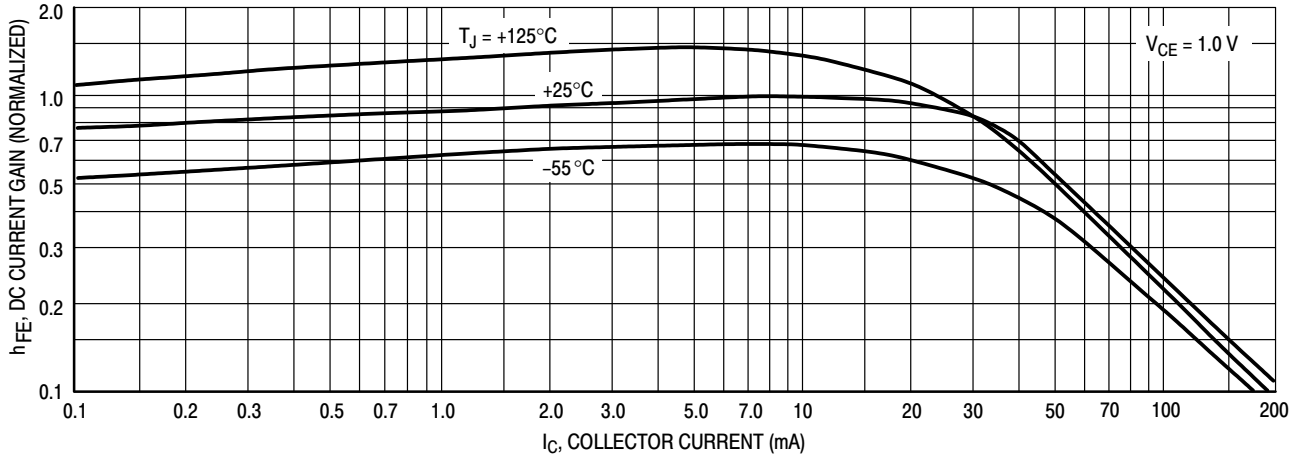


Figure 12. DC Current Gain

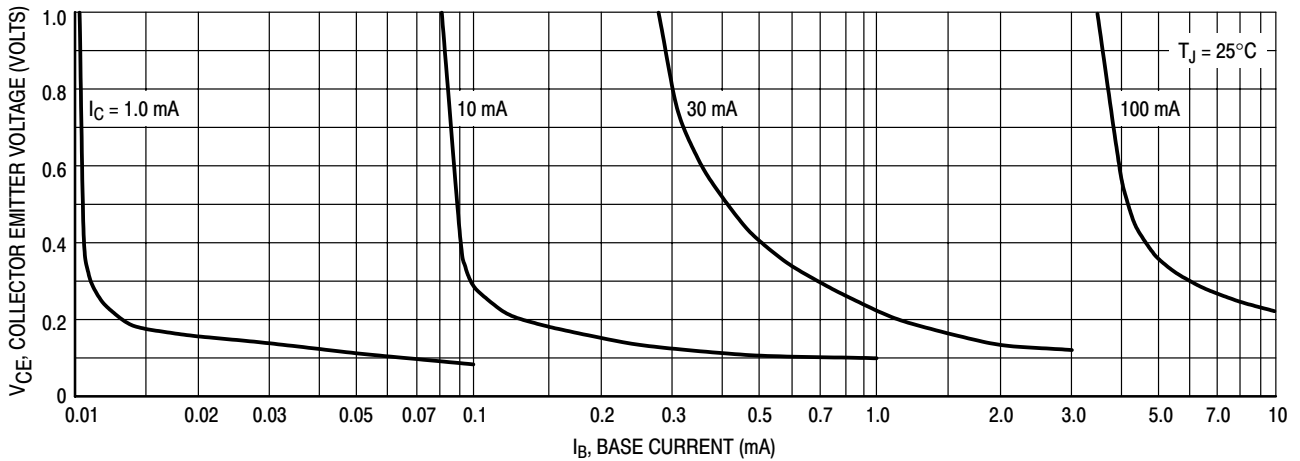


Figure 13. Collector Saturation Region

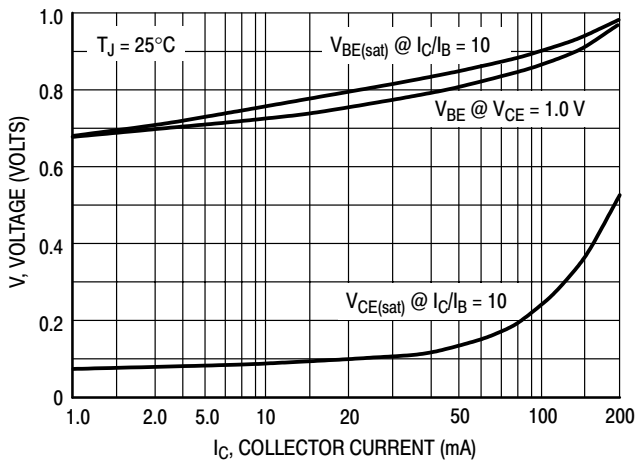


Figure 14. "ON" Voltages

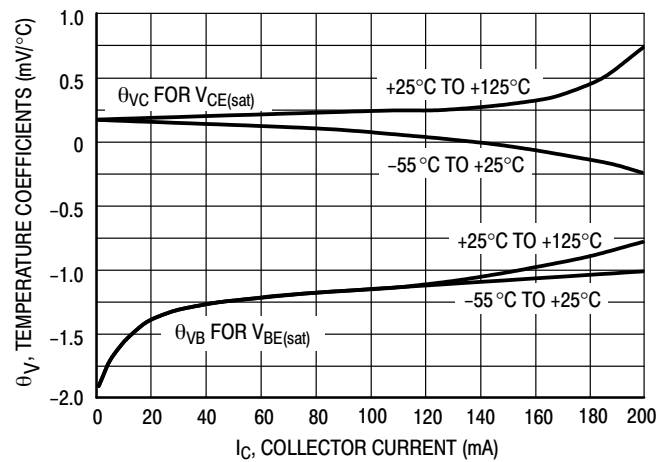
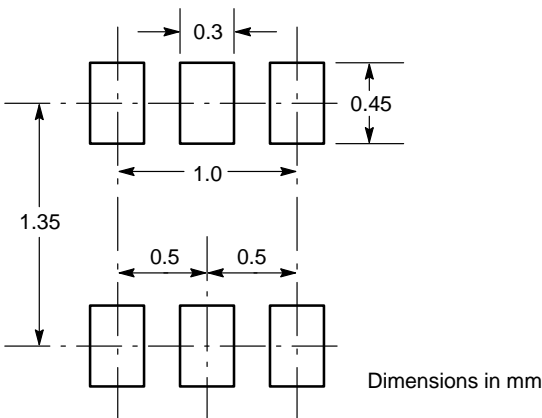


Figure 15. Temperature Coefficients

INFORMATION FOR USING THE SOT-563 SURFACE MOUNT PACKAGE
MINIMUM RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to insure proper solder connection

interface between the board and the package. With the correct pad geometry, the packages will self align when subjected to a solder reflow process.



SOT-563

SOT-563 POWER DISSIPATION

The power dissipation of the SOT-563 is a function of the pad size. This can vary from the minimum pad size for soldering to a pad size given for maximum power dissipation. Power dissipation for a surface mount device is determined by $T_{J(max)}$, the maximum rated junction temperature of the die, $R_{\theta JA}$, the thermal resistance from the device junction to ambient, and the operating temperature, T_A . Using the values provided on the data sheet for the SOT-563 package, P_D can be calculated as follows:

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

The values for the equation are found in the maximum ratings table on the data sheet. Substituting these values into the equation for an ambient temperature T_A of 25°C, one can calculate the power dissipation of the device which in this case is 150 milliwatts.

$$P_D = \frac{150^\circ\text{C} - 25^\circ\text{C}}{833^\circ\text{C/W}} = 150 \text{ milliwatts}$$

The 833°C/W for the SOT-563 package assumes the use of the recommended footprint on a glass epoxy printed circuit board to achieve a power dissipation of 150 milliwatts. There are other alternatives to achieving higher power dissipation from the SOT-563 package. Another alternative would be to use a ceramic substrate or an aluminum core board such as Thermal Clad®. Using a board material such as Thermal Clad, an aluminum core board, the power dissipation can be doubled using the same footprint.

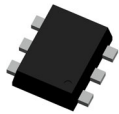
Thermal Clad is a registered trademark of the Bergquist Company.

SOLDERING PRECAUTIONS

The melting temperature of solder is higher than the rated temperature of the device. When the entire device is heated to a high temperature, failure to complete soldering within a short time could result in device failure. Therefore, the following items should always be observed in order to minimize the thermal stress to which the devices are subjected.

- Always preheat the device.
- The delta temperature between the preheat and soldering should be 100°C or less.*
- When preheating and soldering, the temperature of the leads and the case must not exceed the maximum temperature ratings as shown on the data sheet. When using infrared heating with the reflow soldering method, the difference shall be a maximum of 10°C.
- The soldering temperature and time shall not exceed 260°C for more than 10 seconds.
- When shifting from preheating to soldering, the maximum temperature gradient shall be 5°C or less.
- After soldering has been completed, the device should be allowed to cool naturally for at least three minutes. Gradual cooling should be used as the use of forced cooling will increase the temperature gradient and result in latent failure due to mechanical stress.
- Mechanical stress or shock should not be applied during cooling.

* Soldering a device without preheating can cause excessive thermal shock and stress which can result in damage to the device

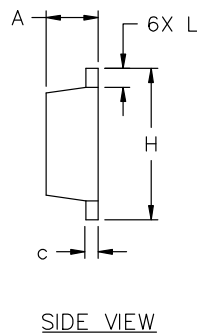
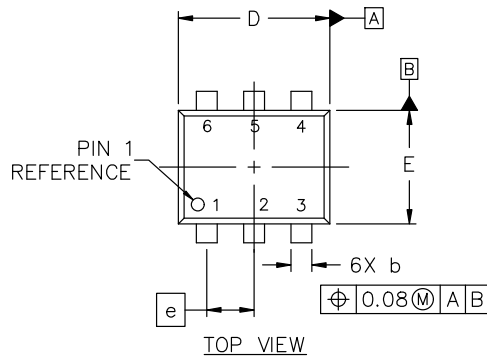


SOT-563-6 1.60x1.20x0.55, 0.50P
CASE 463A
ISSUE J

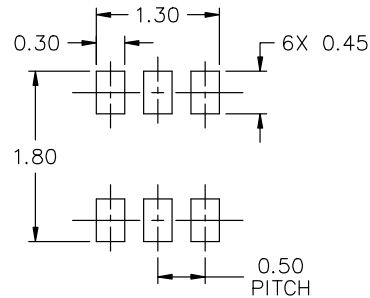
DATE 15 FEB 2024

NOTES:

1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5-2018.
2. ALL DIMENSION ARE IN MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.



| DIM | MILLIMETERS | | |
|-----|-------------|------|------|
| | MIN. | NOM. | MAX. |
| A | 0.50 | 0.55 | 0.60 |
| b | 0.17 | 0.22 | 0.27 |
| c | 0.08 | 0.13 | 0.18 |
| D | 1.50 | 1.60 | 1.70 |
| E | 1.10 | 1.20 | 1.30 |
| e | 0.50 BSC | | |
| H | 1.50 | 1.60 | 1.70 |
| L | 0.10 | 0.20 | 0.30 |



STYLE 1:
PIN 1. EMITTER 1
2. BASE 1
3. COLLECTOR 2
4. EMITTER 2
5. BASE 2
6. COLLECTOR 1

STYLE 2:
PIN 1. EMITTER 1
2. EMITTER 2
3. BASE 2
4. COLLECTOR 2
5. BASE 1
6. COLLECTOR 1

STYLE 3:
PIN 1. CATHODE 1
2. CATHODE 1
3. ANODE/ANODE 2
4. CATHODE 2
5. CATHODE 2
6. ANODE/ANODE 1

STYLE 4:
PIN 1. COLLECTOR
2. COLLECTOR
3. BASE
4. EMITTER
5. COLLECTOR
6. COLLECTOR

STYLE 5:
PIN 1. CATHODE
2. CATHODE
3. ANODE
4. ANODE
5. CATHODE
6. CATHODE

STYLE 6:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. CATHODE
5. CATHODE
6. CATHODE

STYLE 7:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. CATHODE
5. ANODE
6. CATHODE

STYLE 8:
PIN 1. DRAIN
2. DRAIN
3. GATE
4. SOURCE
5. DRAIN
6. DRAIN

STYLE 9:
PIN 1. SOURCE 1
2. GATE 1
3. DRAIN 2
4. SOURCE 2
5. GATE 2
6. DRAIN 1

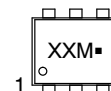
STYLE 10:
PIN 1. CATHODE 1
2. N/C
3. CATHODE 2
4. ANODE 2
5. N/C
6. ANODE 1

STYLE 11:
PIN 1. EMITTER 2
2. BASE 2
3. COLLECTOR 1
4. EMITTER 1
5. BASE 1
6. COLLECTOR 2

RECOMMENDED MOUNTING FOOTPRINT*

* FOR ADDITIONAL INFORMATION ON OUR Pb-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERM/D.

GENERIC MARKING DIAGRAM*



XX = Specific Device Code
M = Month Code
▪ = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

| | | |
|------------------|---------------------------------|--|
| DOCUMENT NUMBER: | 98AON11126D | Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red. |
| DESCRIPTION: | SOT-563-6 1.60x1.20x0.55, 0.50P | PAGE 1 OF 1 |

onsemi and onsemi are trademarks of Semiconductor Components Industries, LLC dba onsemi or its subsidiaries in the United States and/or other countries. onsemi reserves the right to make changes without further notice to any products herein. onsemi makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does onsemi assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. onsemi does not convey any license under its patent rights nor the rights of others.

onsemi, **Onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:

Technical Library: www.onsemi.com/design/resources/technical-documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support

For additional information, please contact your local Sales Representative at www.onsemi.com/support/sales

