

General purpose transistor (isolated dual transistors)

IMX25

●Features

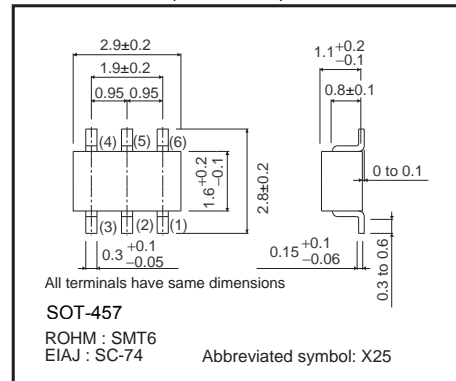
- 1) Two 2SD2704K chips in a SMT package.
- 2) Mounting possible with SMT3 automatic mounting machine.
- 3) Transistor elements are independent, eliminating interference.
- 4) Mounting cost and area can be cut in half.

●Structure

Epitaxial planar type
NPN silicon transistor

The following characteristics apply to both Tr₁ and Tr₂.

●Dimensions (Unit : mm)

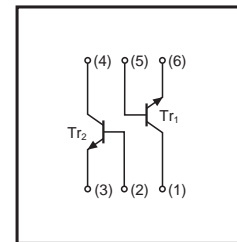


●Absolute maximum ratings (Ta=25°C)

Parameter	Symbol	Limits	Unit
Collector-base voltage	V _{CB0}	50	V
Collector-emitter voltage	V _{CEO}	20	V
Emitter-base voltage	V _{EBO}	25	V
Collector current	I _c	300	mA
Power dissipation	P _d	300(TOTAL)	mW *
Junction temperature	T _j	150	°C
Storage temperature	T _{stg}	-55 to +150	°C

* 200mW per element must not be exceeded.

●Inner circuit



●Electrical characteristics (Ta=25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Collector-base breakdown voltage	BV _{CB0}	50	-	-	V	I _c =10μA
Collector-emitter breakdown voltage	BV _{CEO}	20	-	-	V	I _c =1mA
Emitter-base breakdown voltage	BV _{EBO}	25	-	-	V	I _E =10μA
Collector cutoff current	I _{cBO}	-	-	0.1	μA	V _{CB} =50V
Emitter cutoff current	I _{EBO}	-	-	0.1	μA	V _{EB} =25V
Collector-emitter saturation voltage	V _{CE(sat)}	-	50	100	mV	I _c /I _B =30mA/3mA
DC current transfer ratio	h _{FE}	820	-	2700	-	V _{CE} =2V, I _c =4mA
Transition frequency	f _T	-	35	-	MHz	V _{CE} =6V, I _E =-4mA, f=10MHz
Output capacitance	C _{ob}	-	3.9	-	pF	V _{CB} =10V, I _E =0A, f=1MHz
Output On-resistance	R _{on}	-	0.7	-	Ω	I _B =5mA, V _i =100mV _{rms} , f=1kHz

●Packaging specifications

Part No.	Packaging type	Taping
	Code	T110
	Basic ordering unit (pieces)	3000
IMX25		○

●Electrical characteristic curves

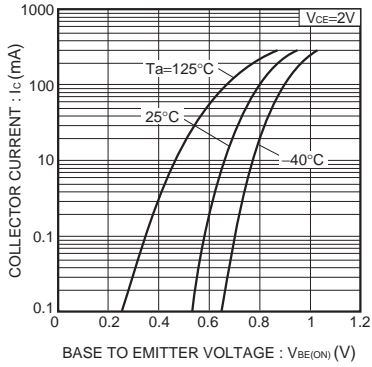


Fig.1 Grounded emitter propagation characteristics (I)

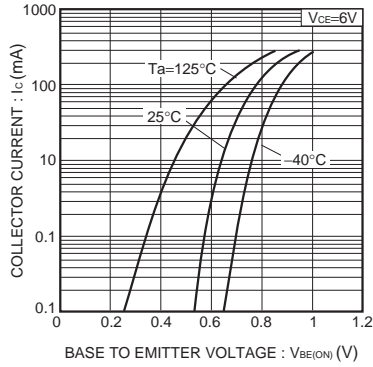


Fig.2 Grounded emitter propagation characteristics (II)

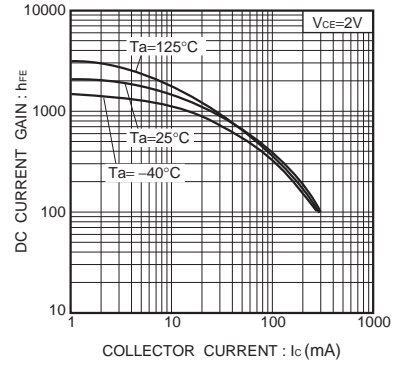


Fig.3 DC current gain vs. collector current (I)

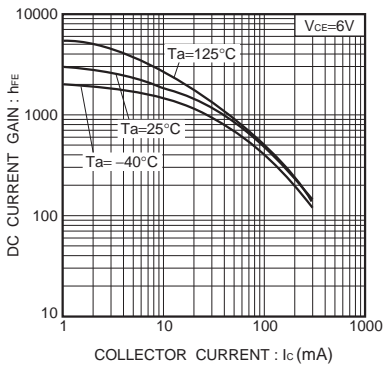


Fig.4 DC current gain vs. collector current (II)

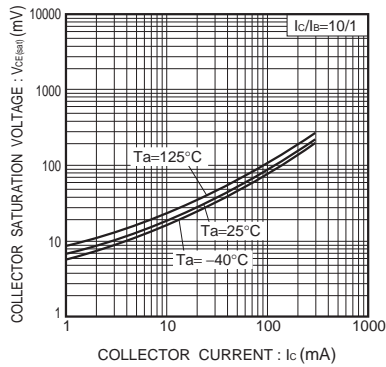


Fig.5 Collector-emitter saturation voltage vs. collector current (I)

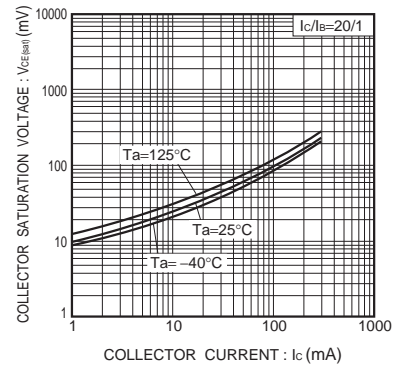


Fig.6 Collector-emitter saturation voltage vs. collector current (II)

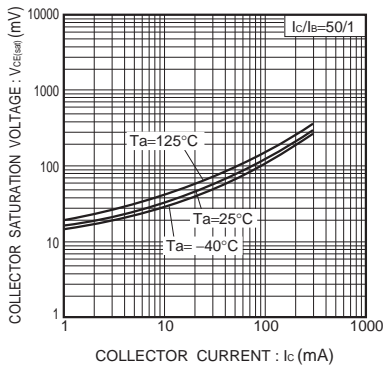


Fig.7 Collector-emitter saturation voltage vs. collector current (III)

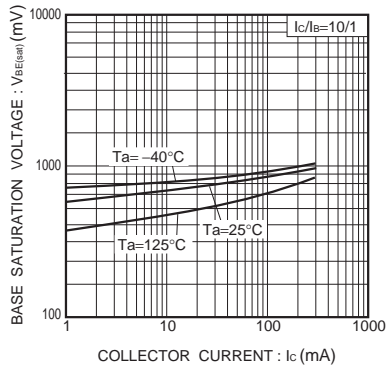


Fig.8 Base-emitter saturation voltage vs. collector current (I)

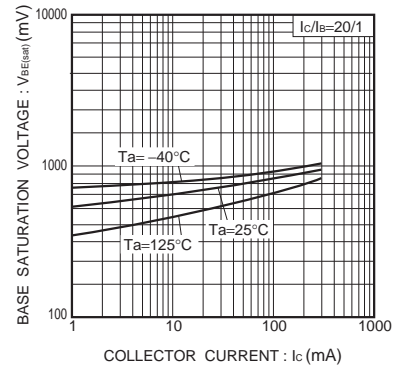


Fig.9 Base-emitter saturation voltage vs. collector current (II)

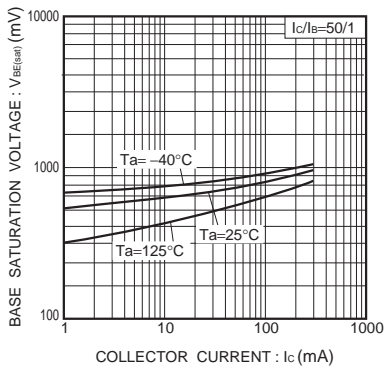


Fig.10 Base-emitter saturation voltage vs. collector current (III)

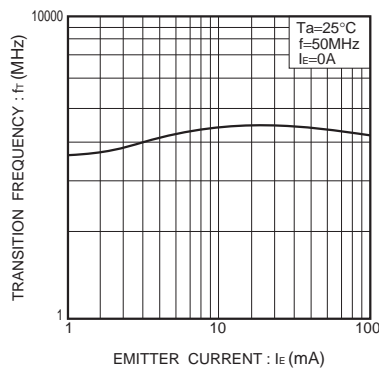


Fig.11 Gain bandwidth product vs. emitter current

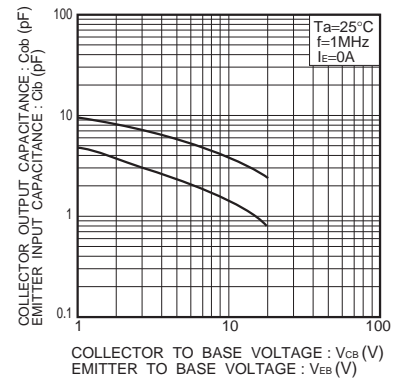


Fig.12 Collector output capacitance vs. collector-base voltage
Emitter input capacitance vs. emitter-base voltage

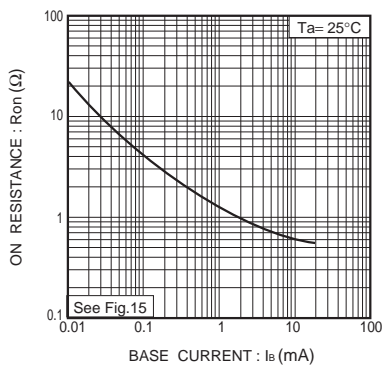


Fig.13 Output-on resistance vs. base current (I)

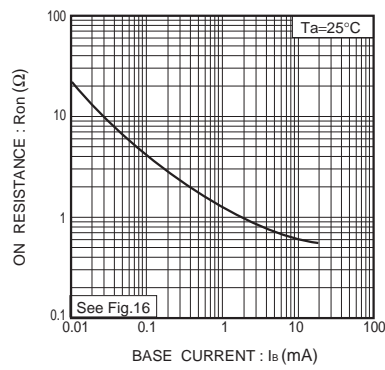


Fig.14 Output-on resistance vs. base current (II)

●Ron measurement circuit

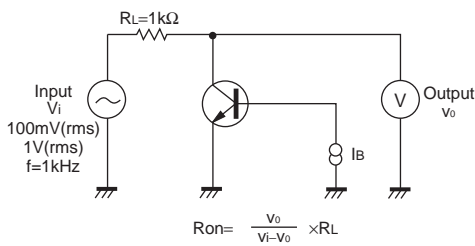


Fig.15 Ron measurement circuit (I)

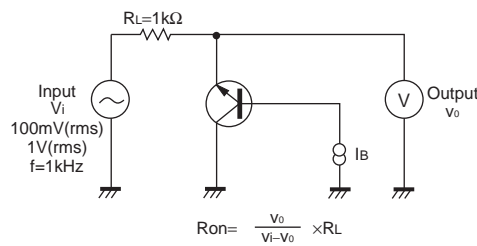


Fig.16 Ron measurement circuit (II)

This product might cause chip aging and breakdown under the large electrified environment. Please consider to design ESD protection circuit.

Notes

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