Application Note AN-50
LinkSwitch™-PL Family

Design Guide (Flyback Topology)

Introduction

The LinkSwitch-PL family of highly integrated monolithic off-line switcher ICs enables implementation of single-stage isolated or non-isolated, power factor corrected, constant current output drivers for LED lighting applications. Non-isolated designs are compatible with low cost TRIAC based dimmers and provide >300:1 dimming range. The low component count simplifies meeting space constraints of LED retrofit designs (e.g. A19 and candelabra lamp sizes) while the >0.9 PF, low THD and harmonic input currents allows a single driver design to be used worldwide.

Scope

This application note is intended for engineers designing an isolated or non-isolated AC to DC power supply driving a constant current LED load. It provides step-by-step guidance on the use of the PIXIs design spreadsheet, part of the PI Expert™ software suite, selection of key components and optimization of designs especially for TRIAC based dimmers. The LinkSwitch-PL may be used in both the flyback or buck-boost topologies however only the flyback is covered in this document. Support, with a separate PIXIs spreadsheet, for the buck-boost topology is planned and will be covered in a separate application note.
In addition to this application note, the reader may also find the Reference Design Kits (RDKs) useful. Each contains a fully functional engineering prototype board, engineering report and device samples. Further details on downloading PI Expert, obtaining an RDK, reviewing additional Design Example Reports (DERs) and updates to this document can be found at www.powerint.com.

Basic Circuit Configuration

A typical application schematic is shown below for a TRIAC dimmable, non-isolated LED driver. Circuit blocks required for interface with TRIAC based phase angle control dimmers are labeled Passive, Active Damper, and Bleeder and can be removed for non-dimming applications.

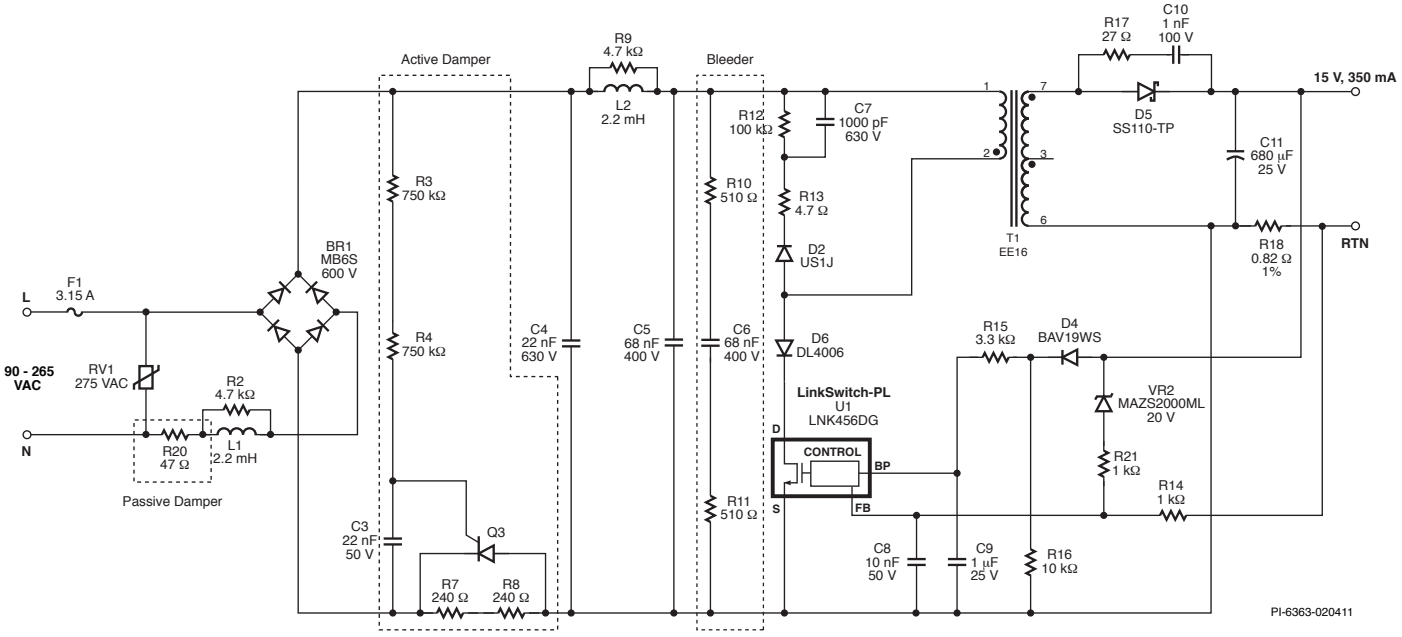

Figure 1. Typical TRIAC Dimmable Application Schematic using a LinkSwitch-PL Device.

Quick Start

Readers familiar with power supply design and Power Integrations design software may elect to skip the step-by-step design approach described later, and can use the following information to quickly design the transformer and select the components necessary for a first prototype. For this approach, only the information described below needs to be entered into the PIXIs spreadsheet, other parameters will be automatically selected based on typical design requirements. References to spreadsheet cell locations (visible in the PIXIs software) are provided in square brackets [cell reference].

- Enter AC input voltage range VAC_{MIN}, VAC_{MAX} and minimum line frequency f_L [B3, B4, B5]
- Enter nominal output voltage V_O [B6]
- Enter nominal output current I_O [B9]
- Enter efficiency estimate [B10]
- Enter loss allocation factor Z [B11]
- Select the enclosure type by clicking on cell [B12] and click on the down arrow to select “open frame” or “retrofit lamp” application
- Select dimming or non-dimming design via the drop down menu or directly entering Yes or No [B13]
- Enter the output diode forward drop [B15]. Use 0.7 V for fast or ultrafast diodes and 0.5 V for Schottky diodes.
- If any warnings are generated, make changes to the design following instruction in the spreadsheet column F
- Build transformer following guidance on transformer construction sheet
- Select key components. See steps 3 and 6
- Build prototype and iterate design as necessary, replacing estimates in the spreadsheets with measured values as appropriate (e.g. efficiency).
- Power Integrations offers transformer prototyping services and links to other vendors: for details see www.powerint.com/componentsuppliers.htm

Step-by-Step Transformer Design Procedure

Step 1. Enter Application Variables VAC_{MIN}, VAC_{MAX}, f_L, V_O, $V_{O(MIN)}$, $V_{O(MAX)}$, I_O, η, Z, Enclosure, Dimming Application, P_O and V_D

Determine the input voltage range from Table 1.

Nominal Input Voltage (VAC)	VAC_{MIN}	VAC_{MAX}	Note
100/115	85	132	Japan / USA
230/240	195	265	EU / Various
277	250	308	Worldwide Single Phase
Universal	85	265	USA 3 Phase

Table 1. Input Voltage Ranges.

Line Frequency, f_L
50 Hz for universal or single 230 VAC input, 60 Hz for single 115 VAC input. 50 Hz for single 100 VAC input. Line frequency is not a direct design parameter but is used within the spreadsheet for correct calculation of parameters such as primary RMS current.

Nominal Output Voltage, V_O (V)
Enter the nominal output voltage.

Typical operating voltage range recommended is V_O ±25%. For comparison the expected LED string voltage variation including tolerance and effect of temperature is < ±15%. Wider output voltage variations are possible with considerations for the practical limitations as described below.

Minimum Output Voltage, $V_{O(MIN)}$
Enter the minimum LED string voltage.

The minimum output voltage is determined by the output power level at which cycle skipping will occur under high-line conditions. Cycle skipping operation maintains output current regulation but degrades PF and THD. Cycle skipping occurs when the voltage across the output current sense resistor (R18 in Figure 1) ≥ 520 mV. A warning will be displayed if the entered output voltage will cause this to occur.

Maximum Output Voltage, $V_{O(MAX)}$
Enter the maximum LED string voltage.

The practical limitation is determined by the maximum peak drain voltage (effect of reflected output voltage).

Nominal Output Current, I_O (A)
Enter the average output current. I_O is the desired average output current. The output current from the converter is a DC current with a super imposed line frequency ripple as an AC component. The amplitude of ripple will be determined by the amount of output capacitance and load resistance.

ENTER APPLICATION VARIABLES					
VACMIN	85		85	V	Minimum AC input voltage
VACMAX	265		265	V	Maximum AC input voltage
FL			50	Hz	Minimum line frequency
VO	15.00		15.0	V	Nominal Output Voltage
VO_MIN			15.0	V	Minimum output voltage tolerance
VO_MAX			15.0	V	Maximum output voltage tolerance
IO	0.40		0.400	A	Average output current
n			0.7	%/100	Total power supply efficiency
Z			0.5		Loss allocation factor.
Enclosure	Open Frame		Open Frame		Enclosure selections determines thermal conditions and maximum power
Dimming Application	Yes		Yes		Dimming applications generally require lower flux density to avoid audible noise problems
PO			6.00	W	Average output power
VD			0.5	V	Output diode forward voltage drop

Figure 2. Application Variable Section of LinkSwitch-PL Spreadsheet.

Power Supply Efficiency, η
Enter the estimated efficiency of the complete power supply measured at the output terminals under worst case line input voltage. The worst case will occur at either the lowest or highest input voltage. Start with a value of 78% until a prototype can be measured.

Power Supply Loss Allocation Factor, Z
This factor represents the proportion of losses between the primary and secondary of the power supply. Z factor is used together with the efficiency number to determine the actual power that must be delivered by the power stage. For example, losses in the input stage (EMI filter, rectification, damper, bleeder, etc.) are not processed by the power stage (transferred through the transformer) and therefore, although they reduce efficiency, the transformer design is not affected by their effect on efficiency.

Z = (secondary side losses)/(total losses)

Examples of primary side losses are losses incurred in the input rectifier and EMI filter, MOSFET conduction losses and primary side winding losses. Examples of side secondary losses include the losses in the secondary diode, secondary winding and core losses, losses associated with the primary clamp circuit and the bias winding.

Starting values: For non-dimming designs 0.5, for dimming designs 0.4.

Enclosure
Select Open Frame or Retrofit Lamp. Open Frame enclosure allows higher output power before a thermal warning is issued by the spreadsheet. Retrofit Lamp applications are assumed to be self heated by the LED load which reduces allowable device dissipation and therefore output power is reduced.

Dimming Application
Enter “YES” for LED dimming, “NO” for non-dimming applications.

Average Output Power, P_O (W)
This is the calculated average output power at V_O and I_O.

Output Diode Forward Voltage Drop, V_D (V)
Enter the estimated output diode forward voltage drop. Use 0.7 for ultra fast rectifiers and 0.5 for Schottky diodes.

Output Power Table

Product	85-265 VAC	
	Minimum Output Power	Maximum Output Power
LNK454D	1.5 W	3 W
LNK456D	3 W	6 W
LNK457D/K/V	4 W	8 W
LNK458K/V	6 W	11.5 W
LNK460K/V	8 W	16 W

Table 2. Output Power Table.

Number of Serial LEDs	Output Current			
	350 mA	500 mA	700 mA	1000 mA
1	LNK454	LNK454	LNK454	LNK456
2	LNK454	LNK456	LNK456	LNK457
3	LNK456	LNK456	LNK457	LNK458
4	LNK456	LNK457	LNK458	LNK460
5	LNK457	LNK458	LNK460	
6	LNK457	LNK458	LNK460	
7	LNK458	LNK460		
8	LNK458	LNK460		
9	LNK458	LNK460		
10	LNK460			
11	LNK460			
12	LNK460			

Table 3. Device Selection Based on Length of Output LED Series String and Current. A Typical Voltage Drop of 3.5 V per LED is Assumed.

Step 2. Enter the LinkSwitch-PL Design Variables

Device
Enter the desired device or select Auto (automatically selects the device). Table 2 and 3 provide guidance based on output power, LED drive current and number of LEDs per string (V_O).

Select the device from Table 2 or Table 3.

Reflected Output Voltage, V_{OR} (V)
V_{OR} is the output voltage that is reflected back on the primary winding. $V_{OR} = (V_O + V_D) \times (N_P/N_S)$.

Turns Ratio
Transformer primary to secondary turns ratio (N_P/N_S).

MOSFET On-Time, t_{ON} (μs)
The minimum on-time of the MOSFET when the input voltage is at VAC_{MIN}. This is provided for information only.

LinkSwitch-PL DESIGN VARIABLES					
Device	Auto		LNK457		Chose device PO max in Open Frame: 7.36W, PO Max in Retrofit Lamp: 6.89 W.
VOR			102.3	V	Reflected output voltage
Turns Ratio			6.6		Primary to secondary turns ratio
TON			3.32	us	Expected on-time of MOSFET at low line and PO
FSW			122.1	kHz	Expected switching frequency at low line and PO
Duty Cycle			40.6	%	Expected operating duty cycle at low line and PO
VDRAIN			569	V	Estimated worst case drain voltage at VACMAX and VO_MAX
IRMS			0.161	A	Worst case primary RMS current at VO
IPK			0.834	A	Worst case peak primary current at VO
ILIM_MAX			1.020	A	Device peak current
KDP			1.25		Ratio between off-time of switch and reset time of core at VACMIN

Figure 3. Design Variables Section of Spreadsheet.

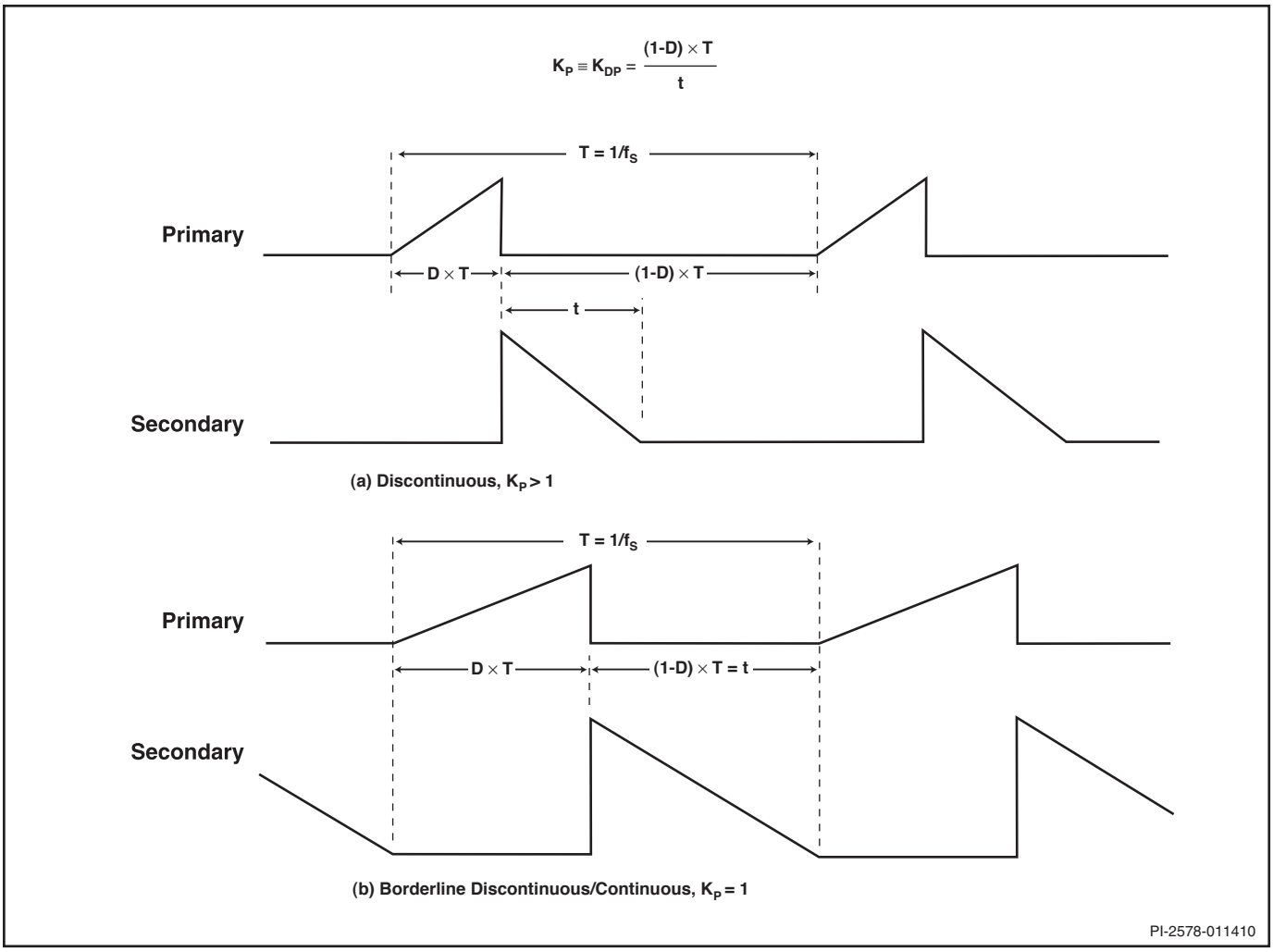

Figure 4. Discontinuous Mode Current Waveform, $K_p \geq 1$.

Switching Frequency, F_{SW}
Expected maximum switching frequency which occurs when the input voltage is at VAC_{MIN}.

Duty Cycle
Expected maximum duty cycle at VAC_{MIN}.

V_{DRAIN} (V)
Expected maximum MOSFET drain voltage. This voltage assumes typical design with nominal transformer leakage inductance and an appropriately designed drain clamp circuit.

Primary RMS Current, I_{RMS} (A)
Calculated maximum primary RMS current. This is calculated over an entire AC cycle at both VAC_{MIN} and VAC_{MAX} with the larger of the two values displayed.

Primary Peak Current, I_{PK} (A)
Calculated peak drain current.

Device Peak Current, $I_{LIM(MAX)}$ (A)
The device's maximum internal current limit.

Off-Time vs. Reset Time, K_{DP}
The ratio of the off-time of the switch and the reset time of the core.

Step 3. LinkSwitch-PL External Component Calculations

Output Current Sense Resistor, R_{SENSE}
R_{SENSE} is the calculated output current sense resistor value necessary to set the output current to the value entered of I_O. Entering in a different value will change the average output current when a prototype is constructed. This change must be entered into the spreadsheet by also changing the value for I_O in the Application Variable section in the spreadsheet.

Standard R_{SENSE}
This is the closest standard 1% value of R_{SENSE}.

Power Dissipated by Sense Resistor, P_{SENSE} (W)
This is the calculated power dissipation of R_{SENSE} ($P_{SENSE} = I_O^2 \times R_{SENSE}$).

LinkSwitch-PL EXTERNAL COMPONENT CALCULATIONS					
RSENSE			0.725	Ohms	Output current sense resistor
Standard RSENSE			0.73	Ohms	Closest 1% value for RSENSE
PSENSE			0.116	W	Power dissipated by RSENSE

Figure 5. External Component Calculations of Spreadsheet.

Step 4. Enter Transformer Core/Construction Variables

ENTER TRANSFORMER CORE/CONSTRUCTION VARIABLES					
Core Type	EE19		EE19		Core Type
Core Part Number			PC40EE19-Z		Core Part Number (if Available)
Bobbin Part Number			BE-19-118CPH		Bobbin Part Number (if available)
AE			23.00	mm^2	Core Effective Cross Sectional Area
LE			39.40	mm	Core Effective Path Length
AL			1250	nH/T^2	Ungapped Core Effective Inductance
BW			9	mm	Bobbin Physical Winding Width
L			3		Number of primary winding layers
NS			18	Turns	Number of Secondary Turns

Figure 6. Transformer Core/Construction Variables of Spreadsheet.

Core Type
Enter the core type. If the entered core type is in the spreadsheet database, values for A_E, L_E, A_L and BW will show in the spreadsheet's output column. If the entered core is not in the database, enter the values as described below.

Core Effective Cross Sectional Area, A_E (mm^2)
Enter the core's effective cross sectional area.

Core Effective Path Length, L_E (mm)
Enter the core's effective path length.

Ungapped Core Effective Inductance, A_L (nH/T^2)
Enter the core's ungapped inductance constant (nH/T^2).

Bobbin Physical Winding Width, BW (mm)
Enter the bobbin's winding width. In an isolated design (non dimming only) reduce the value of BW by the total tape margin width used (6.4 mm for 230 VAC or 4 mm for 115 VAC).

Number of Primary Layers, L
Enter the desired number of primary winding layers. To keep the leakage inductance to a manageable level, it is advised to keep the primary layers to 3 or less. If the CMA in the Transformer Primary Design Parameters section is less than 200 Cmils/A (greater than 9.75 A/mm^2), use a larger core size.

Number of Secondary Turns, N_S
This is the number of secondary winding turns.

Step 5. Transformer's Primary Side Design Parameters

Primary Inductance, L_P (mH)
This is the required nominal primary inductance.

Primary Inductance Tolerance, L_P
This is the primary inductance tolerance specification. The default is 10%.

Number of Primary Turns, N_P
This is the required number of primary turns.

Gapped Core Effective Inductance, A_{LG} (nH/T^2)
This is the gapped core effective inductance.

Operating Flux Density, B_M (Gauss)
To keep the core from saturating, a maximum recommended flux density is 3000 Gauss (0.3 T). In dimming applications, a value of 2000 Gauss (0.2 T) is recommended to minimize audible noise.

BAC
Worst case AC Flux Density for Core Loss Curves (0.5 × peak to peak).

TRANSFORMER PRIMARY DESIGN PARAMETERS					
LP			0.660	mH	Primary Inductance
LP Tolerance			10	%	Tolerance of Primary Inductance
NP			120	Turns	Primary Winding Number of Turns
ALG			46	nH/T^2	Gapped Core Effective Inductance
BM			1995	Gauss	Operating Flux Density
BAC			998	Gauss	Worst case AC Flux Density for Core Loss Curves (0.5 X Peak to Peak)
BP			2683	Gauss	Calculated Worst Case Peak Flux Density (BP < 3600 G)
LG			0.631	mm	Gap Length (Lg > 0.1 mm)
BWE			27	mm	Effective Bobbin Width
OD			0.23	mm	Maximum Primary Wire Diameter including insulation
INS			0.04	mm	Estimated Total Insulation Thickness (= 2 * film thickness)
DIA			0.18	mm	Bare conductor diameter
AWG			33	AWG	Primary Wire Gauge (Rounded to next smaller standard AWG value)
CM			51	Cmils	Bare conductor effective area in circular mils
CMA			315	Cmils/Amp	Primary Winding Current Capacity (200 < CMA < 500)
Primary Current Density (J)			6.34	A/mm^2	Primary Winding Current density (3.8 < J < 9.75 A/mm^2)

Figure 7. Transformer Primary Design Parameters of Spreadsheet.

Peak Flux Density, B_P (Gauss)
This is the peak flux density that may occur in start-up or during transient line or load conditions. A limit of 3600 Gauss (0.36 T) is recommended to prevent core saturation especially in designs with high operating core temperatures.

Core Gap, L_G (mm)
This is the core's gap length needed for the desired primary inductance. This is useful if gapping cores in the laboratory. When specifying to a vendor, A_{LG} should be used.

Bobbin Width, BWE (mm)
This is the effective bobbin width. It is calculated by multiplying the bobbin width by the number of layers of the primary.

Primary Wire Diameter, OD (mm)
This is the maximum primary wire diameter that will fit into the BWE. The actual OD may be entered if it differs from value calculated by the spreadsheet. This will improve the accuracy of the primary winding current density calculation.

Insulation Thickness, INS (mm)
This is the estimated total insulation thickness applied to the primary wire (= 2 × insulation thickness). This is used to calculate the bare copper wire thickness (DIA).

DIA (mm)
This is the maximum bare copper wire thickness that will fit on the bobbin in the specified number of layers.

AWG
The recommend primary wire gauge.

CM
Bare primary wire effective area Cmils.

CMA
CMA is the primary wire current capacity. If the CMA is less than 200 Cmils/Amp (>9.75 A/mm^2), the efficiency will be reduced and the transformer temperature rise may be unacceptable. To increase the CMA, increase the primary layers (L) or increase the maximum flux density (B_M) by reducing secondary turns (N_S). If the primary layers (L) is at 3 layer and the maximum flux density (B_M) is at 3000 Gauss. Then a larger transformer core is required to increase CMA.

Primary Current Density (J)
Primary current density and CMA are related. It is recommended to keep the current density between 3.8 A/mm^2 and 9.75 A/mm^2.

Step. 6 Transformer's Secondary Side Design Parameters

Secondary Peak Current, I_{SP} (A)
This value determines the peak current through the output rectifier and the output switching noise voltage (I_{SP} × ESR of output capacitor).

Secondary Winding Current, I_{SRMS} (A)
Secondary winding RMS Current.

Output Current, I_O (A)
I_O is the average output current. Select an output diode with a current rating equal to or above this value.

Peak Inverse Voltage PIVs (V)
This value is the secondary peak inverse voltage applied to the output rectifier. The PIVS value includes a 10% margin for reverse recovery voltage spike. Select a diode voltage rating equal to or above this value.

CMS1
Recommended output winding bare conductor in circular mils.

AWGS (mm)
Recommended output winding wire gauge.

DIAS (mm)
Recommended minimum bare conductor diameter.

Maximum Wire Diameter, ODS (mm)
Maximum outside diameter (useful when using Triple Insulated Wire). Note: triple insulated wire is only required for an isolated design.

SECONDARY DESIGN PARAMETERS					
ISP			5.56	A	Worst Case Peak Secondary Current
ISRMS			1.23	A	Worst Case Secondary RMS current
IO			0.40	A	Output Current
PIVS			71.8	V	Peak Inverse Voltage at VO_MAX on output diode
CMS1			246	Cmils	Output Winding Bare Conductor minimum circular mils
AWGS			26	AWG	Wire Gauge (Rounded up to next larger standard AWG value)
DIAS			0.41	mm	Minimum Bare Conductor Diameter
ODS			1.50	mm	Maximum Outside Diameter for Wire

Figure 8. Secondary Design Parameters of Spreadsheet.

LinkSwitch-PL Application Example

The circuit shown in Figure 9 provides a single constant current output of 350 mA with an LED string voltage of 15 V. The output current can be reduced using a standard AC mains TRIAC dimmer down to 1% (3 mA) without instability or flickering of the LED load. The board is compatible with both low cost leading edge and more sophisticated trailing edge dimmers.

The board was optimized to operate over the universal AC input voltage range (85 VAC to 265 VAC, 47 Hz to 63 Hz) but suffers no damage over an input range of 0 VAC to 300 VAC. This increases field reliability and lifetime during line sags and swells. LinkSwitch-PL based designs provide high power factor (>0.9 at 115 VAC / 230 VAC) and low THD (<15% at 230 VAC, <10% at 115 VAC) enabling compliance to all current international requirements and enabling a single design to be used worldwide.

The form factor of the board was chosen to meet the requirements for standard pear shaped (A19) LED replacement lamps. The output is non-isolated and requires the mechanical design of the enclosure to isolate both the supply and the LED load from the user.

AC Line TRIAC Dimmer Interface Circuits

The requirement to provide output dimming with low cost, TRIAC based, leading edge phase dimmers introduces a number of trade-offs in the design.

Due to the much lower power consumed by LED lighting compared to incandescent lighting, the current drawn by the lamp is below the holding current of the TRIAC dimmer. This causes undesirable behavior such as limited dimming range and/or flickering. Inrush current that flows to charge the input capacitance when the TRIAC turns on causes current ringing. This too can cause similar undesirable behavior as the ringing may cause the TRIAC current to fall to zero and turn off for the remainder of the AC cycle or rapidly turn on and off.

To overcome these issues the design includes three circuit blocks, a passive damper, an active damper and a bleeder. The drawback of these blocks is increased power dissipation and therefore reduced efficiency of the supply. In this design, the values selected allow flicker-free operation with a single lamp connected to a single dimmer at high-line. For flicker-free operation with multiple lamps in parallel or at low line voltages only (100 / 115 VAC) then the values may be optimized to reduce dissipation and increase efficiency.

As these blocks are only required for dimming applications, for non-dimming designs these components can simply be omitted and jumpers used to replace R7, R8 and R20.

Active and Passive Damper Circuits

Resistor R20 forms a passive damper that together with the active damper limits the peak inrush current when the TRIAC fires on each half cycle. This prevents input current ringing that can cause the TRIAC current to fall to zero and therefore cause the TRIAC to turn off. This can result in flicker and/or shimmer of the output LED load as the TRIAC turns on an off multiple times in one AC cycle. It should be a flameproof type to safely fail during a single point fault (e.g. failure of a bridge diode). Worst case dissipation occurs during 90 degree TRIAC conduction angle.

The active damper circuit connects a series resistance (R7 and R8) with the input rectifier for a period of each AC half-cycle, it is then bypassed for the remainder of the AC cycle by a parallel SCR (Q3). Resistor R3, R4 and C3 determine the delay before the turn-on of Q3 which then shorts out the damper resistors R7 and R8.

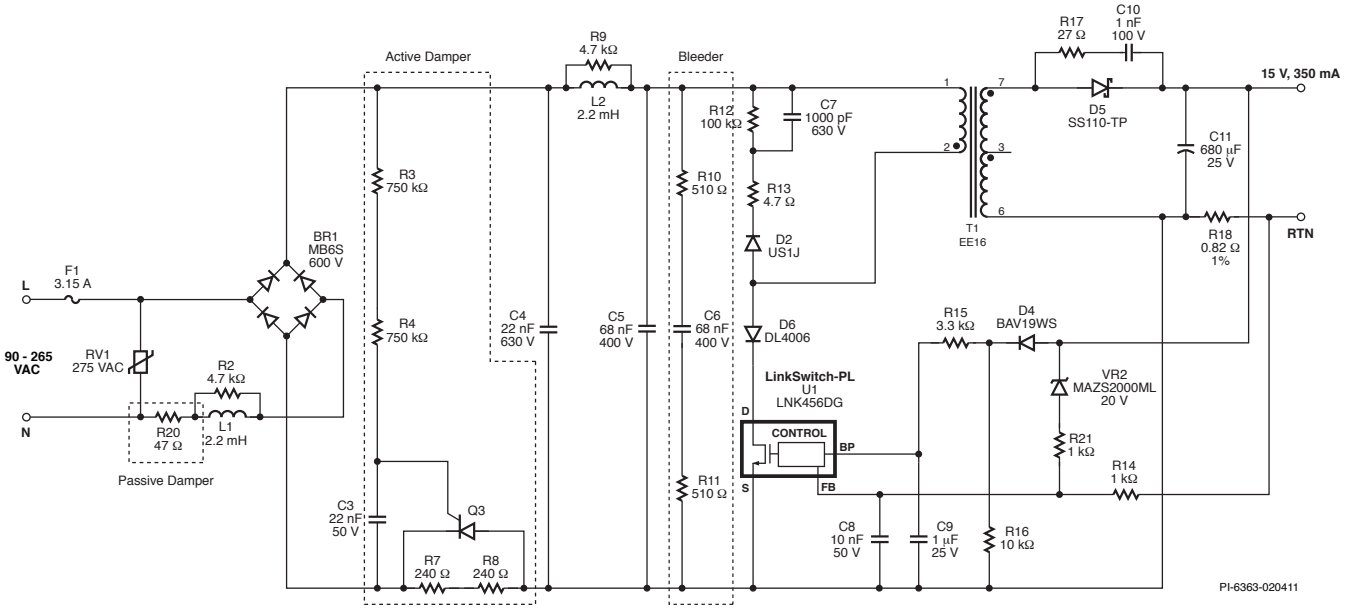

Figure 9. Schematic of a 5 W, 15 V LED Driver for A19 Incandescent Lamp Replacement.

Bleeder Circuit
Resistor R10, R11 and C6 form a bleeder network which ensures the initial input current is high enough meet the TRIAC holding current requirement, especially during small conduction angles. For non-dimming application R10, R11 and C6 may be omitted.

Input Rectifier and EMI Filter
EMI filtering is provided by L1 and a pi (π) filter formed by C4, L2 and C5. Resistors R2 and R9 dampen the self resonances of the filter stages and reduce the resultant peaks in the conducted EMI spectrum. As shown the design meets EN55015 conducted limits with >20 dB margin.

The incoming AC is rectified by BR1 and filtered by C4 and C5. The total effective input capacitance, the sum of C4 and C5, was selected to ensure correct zero crossing detection of the AC input by the LinkSwitch-PL device, necessary for correct dimming operation.

Primary Components
The LNK456DG device (U1) incorporates the power switching device, oscillator, CC control engine, start-up, and protection functions. The integrated 725 V power MOSFET provides extended design margin, improving robustness during line surge events even in high-line applications. The device is powered from the BYPASS pin via the decoupling capacitor C9. At start-up, C9 is charged by U1 from an internal current source via the DRAIN pin and then during normal operation it is supplied by the output via R15 and D4. For non-dimming designs D4 and R15 may be omitted.

The rectified and filtered input voltage is applied to one end of the primary winding of T1. The other side of the transformer's primary winding is driven by the integrated power MOSFET in U1. The leakage inductance drain voltage spike is limited by an RCD-R clamp consisting of D2, R13, R12, and C7.

Diode D6 is used to protect the IC from negative ringing (drain voltage below source voltage) when the power MOSFET is off and the input voltage is below the reflected output voltage (V_{OR}).

Output Rectification
The secondary of the transformer is rectified by D5, a Schottky barrier type for higher efficiency, and filtered by C11. Resistor R17 and C10 damp high frequency ringing and improve conducted and radiated EMI.

Output Feedback
The CC mode set-point is determined by the voltage drop that appears across R18 which is then fed to the FEEDBACK pin of U1. Output overvoltage protection is provided by VR2 and R21.

Application Considerations

Input Capacitor Selection

For correct operation during dimming, the LinkSwitch-PL device must detect line voltage zero crossing. This is sensed internally via the drain node at the point the DC bus falls to <19 V. The requirement for the DC bus to reach this level on each half-cycle limits the maximum capacitance on the DC side of the input bridge rectifier (C4 + C5 in Figure 9). Typically the maximum capacitance value needed for high power factor also results in meeting the 19 V limit however during development, this voltage should be verified on an oscilloscope.

If a reduction in capacitance is required and this results in increased conducted EMI then capacitance may be added before the input rectifier which effectively isolates it from the bus capacitance.

For applications intended for use with leading edge TRIAC dimmers, film capacitors are recommended as ceramic capacitors typically create audible noise.

Output Capacitor Selection
Output capacitance has a direct effect on the output load (LED) ripple current. The larger the capacitance, the lower the ripple current. Excessive capacitance can prevent the output reaching regulation within the auto-restart time and either cause failure to start or require several start-up attempts (hiccups). Too little capacitance can cause the voltage of the FEEDBACK pin to exceed the cycle skipping mode threshold, degrading PF and causing output flicker while dimming.

Therefore the output capacitance value should be selected such that the ripple voltage across the output current sense resistor (R18 in Figure 9) and fed into the FEEDBACK pin is within the range of 100 mVp-p $\leq V_{FEEDBACK} \leq$ 400 mVp-p with a target value of 290 mVp-p.

The output capacitor type is not critical. Non-electrolytic capacitors are attractive in terms of lifetime (ceramics and solid dielectric types do not have an electrolyte that evaporates over time) however electrolytic types offer the best volumetric efficiency vs. cost. If multi-layer ceramics are selected, verify the data sheet curves of capacitance vs. applied voltage and temperature coefficient. The typical capacitance value may be 50% lower across temperature and/or close to rated voltage. For all capacitor types verify the capacitor(s) selected are rated for the output ripple current. For electrolytic types, this requires selecting a low ESR type. A temperature rating of 105 °C or higher is recommended for long lifetime. For typical designs there is minimal self heating of the output capacitor and therefore lifetime is determined by the internal ambient temperature and broadly follows the Arrhenius equation, i.e. lifetime doubles for every 10 °C drop in operating temperature. For example the selection of a capacitor with a rated life of 5,000 hours at 105 °C would have an expected lifetime of 40,000 hours at 75 °C. End of life is typically defined for an electrolytic capacitor as a doubling of the ESR and the capacitance reducing by 20%. This often has little impact to the performance seen by the end user and extends the fit for purpose lifetime.

Feedback Pin Signal
During normal non-dimming (full power) operation, the FEEDBACK pin threshold voltage (the voltage developed across the current sense resistor) is 290 mV. For best output current regulation, between 100 mVp-p to 400 mVp-p of voltage ripple is recommended.

This can be achieved through selecting the appropriate value of output capacitance and the value of the current sense resistor. If the peak of the ripple voltage exceeds 520 mV, the device will enter cycle skipping mode which will reduce PFC performance (lower PF and increase THD).

Transformer Considerations for use with Leading Edge TRIAC Dimmers

Audible noise can be created in the transformer due to the abrupt change in flux when the TRIAC turns on. This can be minimized by selecting cores with higher mechanical resonant frequencies. Cores with long narrow legs should be avoided (e.g. EEL types). RM and other pot core types are good choices and produce less audible noise than EE cores for the same flux density. Reducing the core flux density (B_M) also reduces audible noise generation. A value below 1500 Gauss usually eliminates any noise generation but reduces the power capability of a given core size.

Working with TRIAC Dimmers

The requirement to provide output dimming with low cost, TRIAC based, leading edge phase dimmers introduces a number of trade-offs in the design.

For correct operation incandescent phase angle dimmers typically have a specified minimum load, typically ~40 W for a 230 VAC rated unit. This is to ensure that the current through the internal TRIAC stays above its specified holding current threshold.

Due to the much lower power consumed by LED lighting the input current drawn by the lamp is below the holding current of the TRIAC within the dimmer. The input capacitance of the driver allows large inrush currents to flow when the TRIAC fires. This then generates input current ringing with the input stage and line inductance which may cause the current to fall below the TRIAC holding current. Both of these mechanisms cause undesirable behavior such as limited dimming range and/or flickering.

To overcome these issues two circuit blocks, damper and bleeder, are incorporated in dimming applications. The drawback of these circuits is increased dissipation and therefore reduced efficiency of the supply.

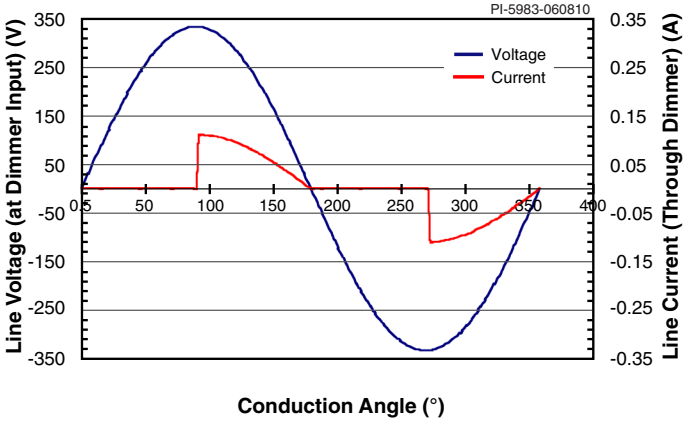

Figure 10. Ideal Input Voltage and Current Waveforms for a Leading Edge TRIAC Dimmer at 90° Conduction Angle.

Figure 10 shows the line voltage and current at the input of a leading edge TRIAC dimmer. In this example, the TRIAC conducts at 90 degrees.

Figure 10 shows the desired rectified bus voltage and current.

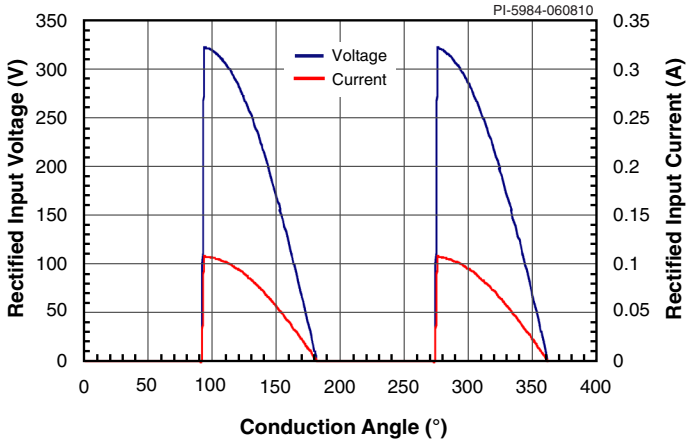

Figure 11. Resultant Waveforms Following Rectification of Ideal TRIAC Dimmer Output.

Figure 12 shows undesired rectified bus voltage and current with the TRIAC turning off prematurely and restarting. On the first half cycle this is due to the input current ringing below the holding current of the TRIAC, excited by the initial inrush current. The second half cycle also shows the TRIAC turning off due to the current falling below the holding current towards the end of the conduction angle. This difference in behavior on alternate half cycles is often seen due to a difference in the holding current of the TRIAC between the two operating quadrants.

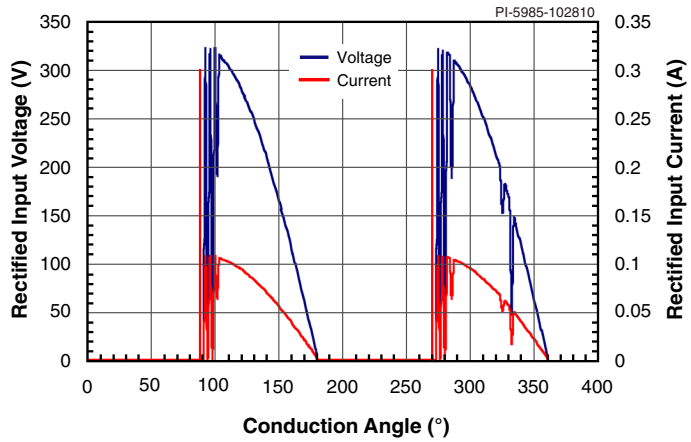

Figure 12. Example of Phase Angle Dimmer Showing Erratic Firing.

If the TRIAC is turning off before the end of the half cycle or rapidly turning on and off then a bleeder and damper circuit are required.
In general as power dissipated in the bleeder and damper circuits increases, so does dimmer compatibility.

Initially install a bleeder network across the rectified power bus (R10, R11 and C6 in Figure 9) with initial values of 0.1 µF and a total resistance of 1 kΩ and power rating of 2 W.

Reduce the capacitance value to find the minimum acceptable value. Reducing the capacitance value reduces power dissipation and therefore increases efficiency.

If the bleeder circuit does not maintain conduction in the TRIAC, then add a damper. The purpose of the damper is to limit the inrush current (as the input capacitance charges) and associated ringing that occurs when the TRIAC turns on.

Initially add a passive damper which is a simple resistor in series with the AC input (R20 in Figure 9). Values in the range of 10 Ω – 100 Ω are typical with the upper range being limited by the allowed dissipation / temperature rise and reduction in efficiency. Values below 10 Ω may also be used but are less effective especially in high AC line input designs.

If a passive damper is insufficient to prevent incorrect TRIAC operation then an active damper can be added. This is typical in high-line applications due to the much larger inrush current that flows when the TRIAC turns on. A low cost active damper circuit is formed by R3, R4, C3, Q3, R7 and R8 in Figure 9. Resistor R7 and R8 limit the inrush current and can be a much higher value than the passive case as they are in circuit for only a fraction of the line cycle. Silicon controlled rectifier (SCR) Q3 shorts R7 and R8 after a delay defined by R3, R4 and C3. The delay is adjusted to give the shortest time that provides acceptable dimmer performance to minimize the dissipation in the resistors. The SCR required is a low current, low cost device available with very low gate current requirements. The gate drive requirement of the selected SCR together with the minimum specified line voltage defines the maximum value of R3 and R4. SCRs with low gate trigger currents are recommended (Table 4). Maximum dissipation in the resistors of the damper and bleeder occurs at 90 degree TRIAC conduction and therefore thermal testing should be performed under this condition to verify component temperatures. For high-line designs it may be necessary to use a wirewound construction for the active damper resistor to prevent failure. This is due to the high instantaneous power dissipated when AC is first applied. In this case a single resistor is acceptable, for example the CRF series from Vitrohm.

It's common for different dimmers to behave differently across manufacturers and power ratings. For example a 300 W dimmer requires less dampening and requires less power loss in the bleeder than a 600 W or 1000 W dimmer due to the use of a lower current rating TRIAC which typically have lower holding currents. Line impedance differences can also cause variation in behavior so during development the use of an AC source is recommended for consistency however testing using AC mains power should also be performed.

Electronic Trailing Edge Dimmers

Figure 13 shows the line voltage and current at the input of the power supply with a trailing edge electronic dimmer. In this example, the dimmer conducts at 90 degrees. This type of dimmer typically uses a power MOSFET or IGBT to provide the switching function and therefore no holding current is necessary. Also since the conduction begins at the zero crossing, high current surges and line ringing are not an issue. Use of these types of dimmers typically does not require damper and bleeder circuits.

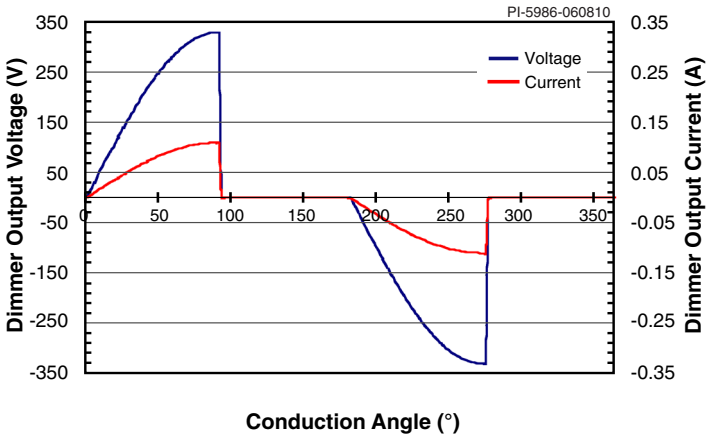

Figure 13. Ideal Dimmer Output Voltage and Current Waveforms for a Trailing Edge Dimmer at 90° Conduction Angle.

Thermal Considerations

Lighting applications present unique thermal challenges for the power supply designer. In many cases the LED load and associated heat sink determine the power supply ambient temperature. Therefore it is important to properly heat sink and verify the operating temperatures of all devices. For the LinkSwitch-PL device a SOURCE pin (D package) or exposed pad (K or V package) temperature of <115 °C is recommended to allow margin for unit to unit variation. Worst case conditions are typically maximum output power, maximum external ambient and either minimum or maximum input voltage.

PCB Layout Considerations

Primary Side Connections

The BYPASS pin capacitor should be located as close to the BYPASS pin and connected as close to the SOURCE pin as possible. The SOURCE pin trace should not be shared with the main power MOSFET switching currents. All FEEDBACK pin components that connect to the SOURCE pin should follow the same guideline as for the BYPASS pin capacitor.

It is critical that the main power MOSFET switching currents return to the bulk capacitor with the shortest path possible. Long high current paths create excessive conducted and radiated noise.

Secondary Side Connections

The output rectifier and output filter capacitor should be as close as possible. The transformer output return pin should have a short trace to the return side of the output filter capacitor. These currents should not flow through the primary side source pin currents. The primary side source pin and secondary side return should be connected with a short trace.

Part Number	Supplier	Specification
MCRZZ-6	On Semi	1.5 A, 400 V, TO-92, 200 µA
P0118DA	ST	0.8 A, 400 V, TO-92, 5 µA

Table 4. Example of SCRs Suitable for Active Damper.

Quick Design Checklist

Maximum Drain Voltage
Verify that the peak V_{DS} does not exceed 700 V under all operating conditions including start-up and fault conditions.

Maximum Drain Current
Measure the peak drain current under all operation conditions including start-up and fault conditions. Look for signs of transformer saturation (usually occurs at high ambient temperatures). Verify that the peak current is less than stated in the Absolute Maximum Ratings section.

Thermal Check
At maximum output power, both minimum and maximum line voltage and ambient temperature; verify that temperature specifications are not exceeded for the LinkSwitch-PL, transformer, output diodes, output capacitors and drain clamp components.

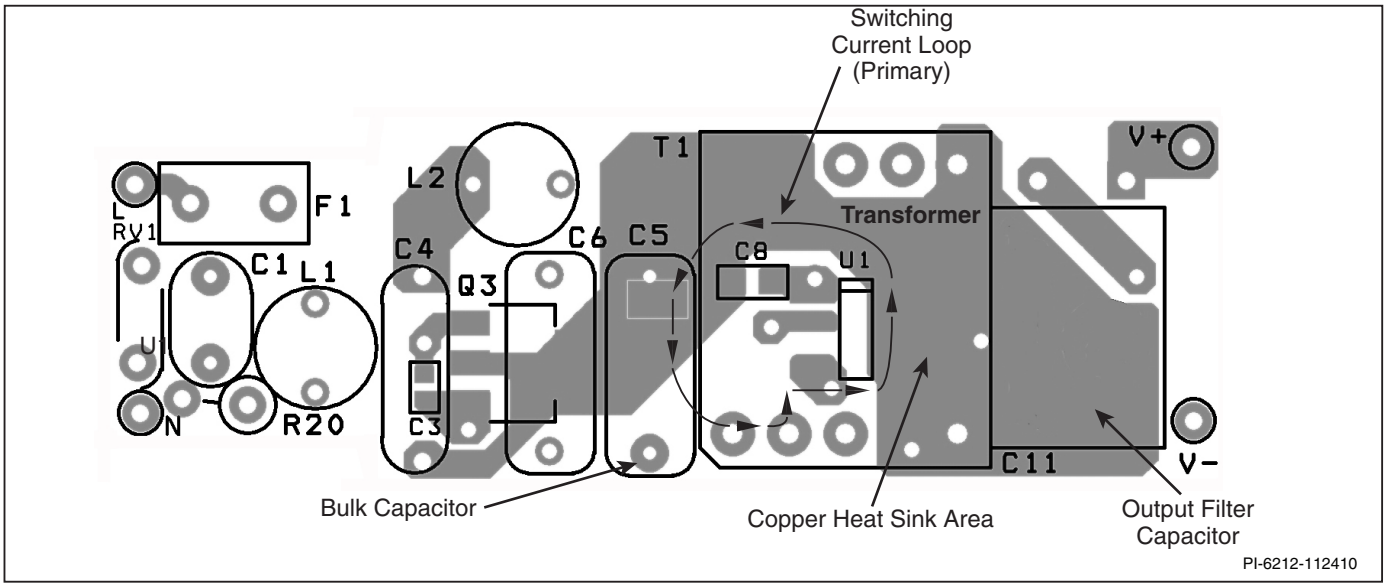

Figure 14. RD-251 PCB Top View.

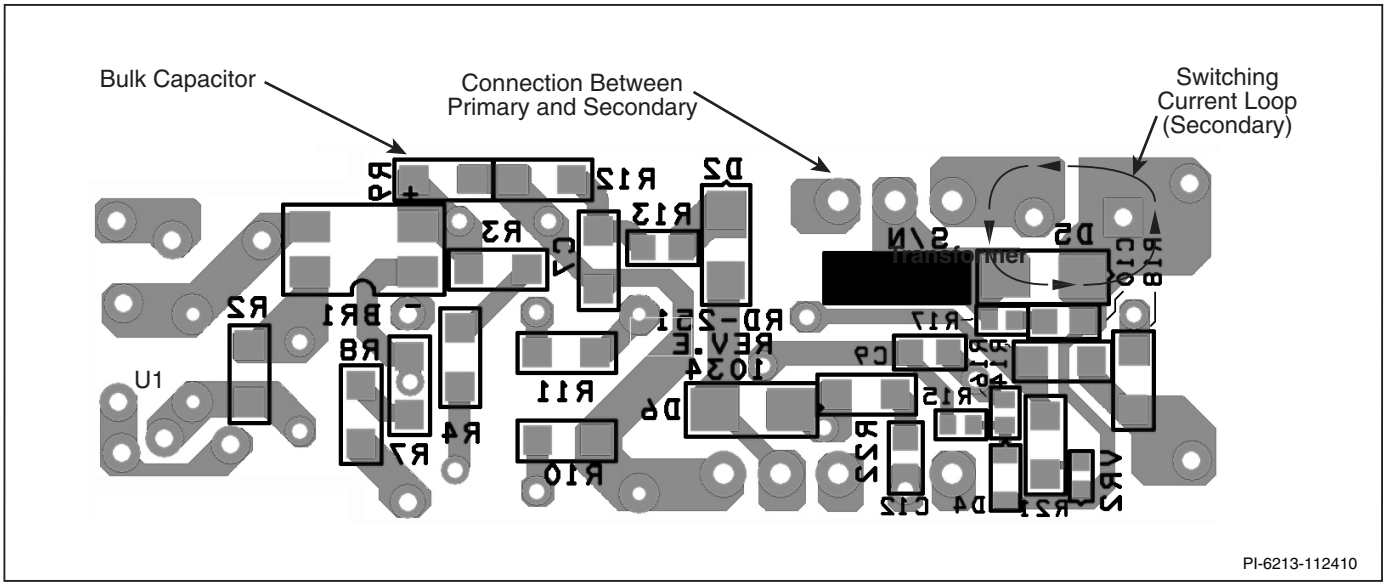

Figure 15. RD-251 PCB Bottom View.

Revision	Notes	Date
A	Initial Release	02/11

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Power Integrations Worldwide Sales Support Locations

World Headquarters
5245 Hellyer Avenue
San Jose, CA 95138, USA.
Main: +1-408-414-9200
Customer Service:
Phone: +1-408-414-9665
Fax: +1-408-414-9765
e-mail: usasales@powerint.com

China (Shanghai)
Room 1601/1610, Tower 1
Kerry Everbright City
No. 218 Tianmu Road West
Shanghai, P.R.C. 200070
Phone: +86-21-6354-6323
Fax: +86-21-6354-6325
e-mail: chinasales@powerint.com

China (Shenzhen)
Rm A, B & C 4th Floor, Block C,
Electronics Science and
Technology Bldg., 2070
Shennan Zhong Rd,
Shenzhen, Guangdong,
China, 518031
Phone: +86-755-8379-3243
Fax: +86-755-8379-5828
e-mail: chinasales@powerint.com

Germany
Rüeckertstrasse 3
D-80336, Munich
Germany
Phone: +49-89-5527-3910
Fax: +49-89-5527-3920
e-mail: eurosales@powerint.com

India
#1, 14th Main Road
Vasanthanagar
Bangalore-560052 India
Phone: +91-80-4113-8020
Fax: +91-80-4113-8023
e-mail: indiasales@powerint.com

Italy
Via De Amicis 2
20091 Bresso MI
Italy
Phone: +39-028-928-6000
Fax: +39-028-928-6009
e-mail: eurosales@powerint.com

Japan
Kosei Dai-3 Bldg.
2-12-11, Shin-Yokomana,
Kohoku-ku
Yokohama-shi Kanagwan
222-0033 Japan
Phone: +81-45-471-1021
Fax: +81-45-471-3717
e-mail: japansales@powerint.com

Korea
RM 602, 6FL
Korea City Air Terminal B/D, 159-6
Samsung-Dong, Kangnam-Gu,
Seoul, 135-728, Korea
Phone: +82-2-2016-6610
Fax: +82-2-2016-6630
e-mail: koreasales@powerint.com

Singapore
51 Newton Road
#19-01/05 Goldhill Plaza
Singapore, 308900
Phone: +65-6358-2160
Fax: +65-6358-2015
e-mail: singaporesales@powerint.com

Taiwan
5F, No. 318, Nei Hu Rd., Sec. 1
Nei Hu Dist.
Taipei, Taiwan 114, R.O.C.
Phone: +886-2-2659-4570
Fax: +886-2-2659-4550
e-mail: taiwansales@powerint.com

Europe HQ
1st Floor, St. James's House
East Street, Farnham
Surrey GU9 7TJ
United Kingdom
Phone: +44 (0) 1252-730-141
Fax: +44 (0) 1252-727-689
e-mail: eurosales@powerint.com

Applications Hotline
World Wide +1-408-414-9660

Applications Fax
World Wide +1-408-414-9760