AN-2098 LM3450 Evaluation Board

1 Introduction

The LM3450 evaluation board is designed to provide an AC to LED solution for a 15W LED load. Specifically, it takes an AC mains input and converts it to a constant current output of 350mA for a series string of 1 to 14 LEDs (maximum LED stack voltage of 45V). There are two assembly versions designed to operate from two different nominal AC input voltages, $120V_{AC}$ or $230V_{AC}$.

The board employs a two stage design with an LM3450 flyback primary stage and an LM3409 secondary stage. The LM3450 provides an isolated 50V regulated output voltage and a power factor corrected input current. The LM3409 uses the 50V flyback output as its input and provides a constant current of 350mA to the LED load. This two-stage design provides excellent line and load regulation as well as isolation. The board is comprised of two copper layers with components on both sides and an FR4 dielelctric.

The two stage design has several key advantages over a single stage design including:

- No 120Hz LED current ripple.
- Better dimming performance at low dimming levels.
- Better line disturbance rejection.
- Better efficiency using small LED stack voltages.

2 Specifications

$120V_{AC}$ 15W Version

- Input Voltage Range: V_{IN} = $90V_{AC}$ – $135V_{AC}$
- Regulated Flyback Output Voltage: V_{OUT} = 50V
- Maximum LED Stack Voltage: V_{LED} < 45V
- Regulated LED Current: I_{LED} = 350mA

$230V_{AC}$ 15W Version

- Input Voltage Range: V_{IN} = $180V_{AC}$ – $265V_{AC}$
- Regulated Flyback Output Voltage: V_{OUT} = 50V
- Maximum LED Stack Voltage: V_{LED} < 45V
- Regulated LED Current: I_{LED} = 350mA

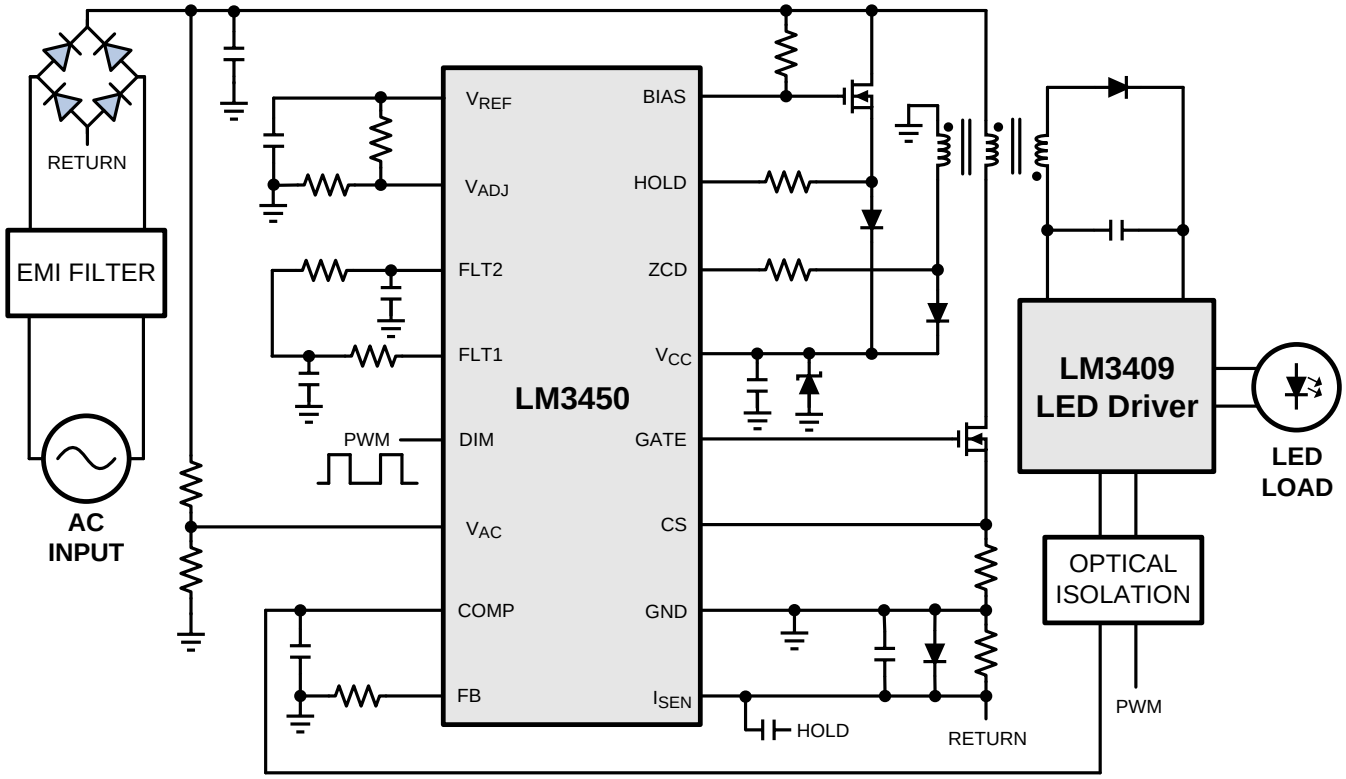


Figure 1. Board Design

3 Typical Performance

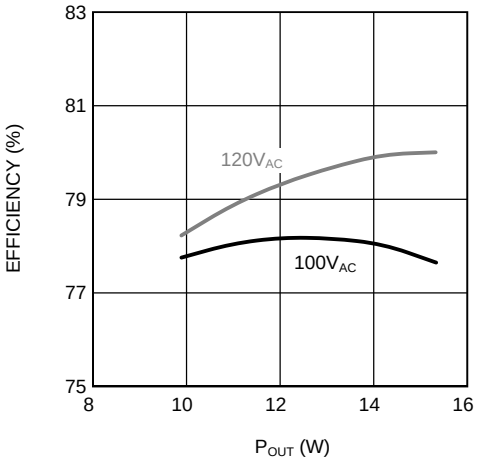


Figure 2. 120V 15W Version Efficiency vs. Output Power

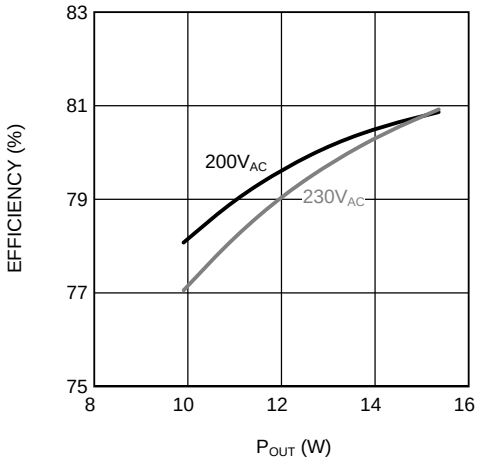


Figure 3. 230V 15W Version Efficiency vs. Output Power

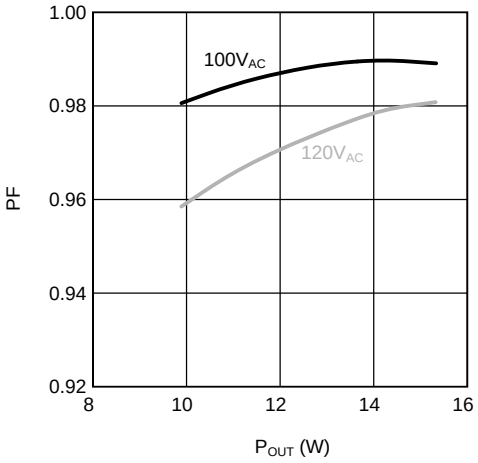


Figure 4. 120V 15W Version Power Factor vs. Output Power

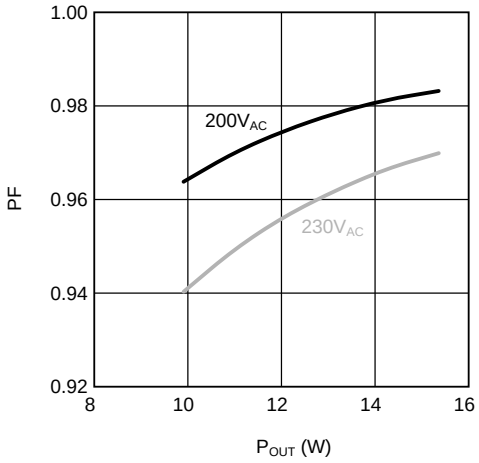


Figure 5. 230V 15W Version Power Factor vs. Output Power

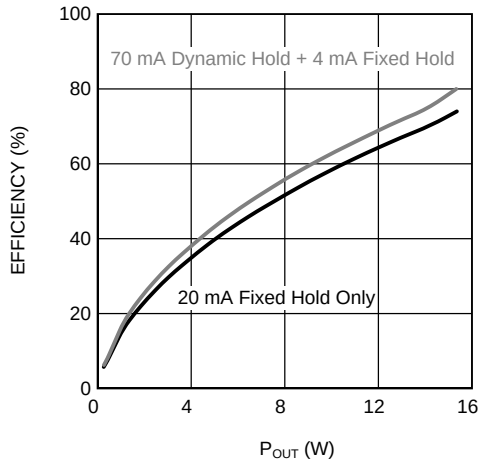


Figure 6. Dimming Efficiency Comparison

4 EMI Performance

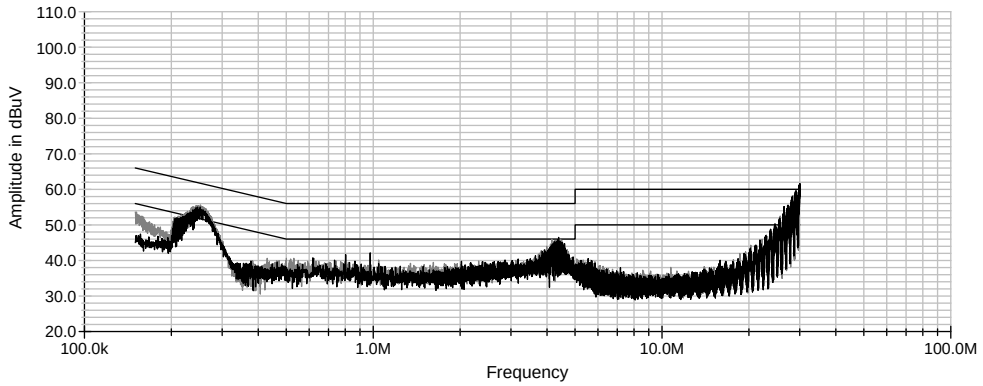


Figure 7. 120V 15W Conducted EMI Peak Scan
Line and Neutral - CISPR/FCC Class B Quasi Peak and Average Limits

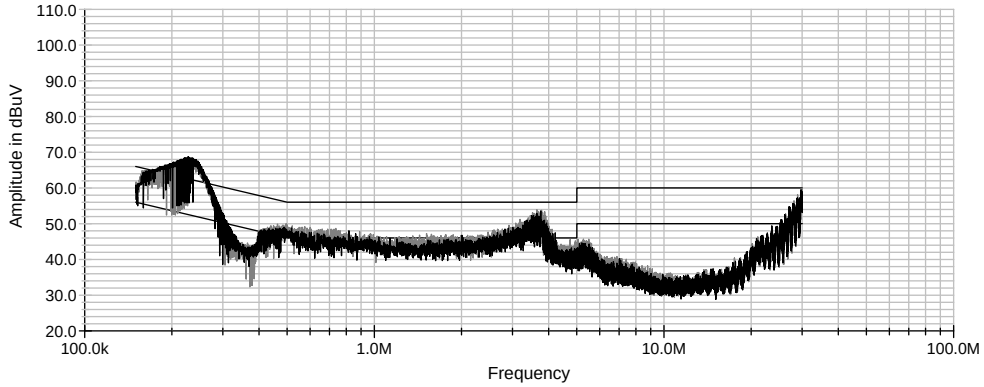


Figure 8. 230V 15W Conducted EMI Peak Scan
Line and Neutral - CISPR/FCC Class B Quasi Peak and Average Limits

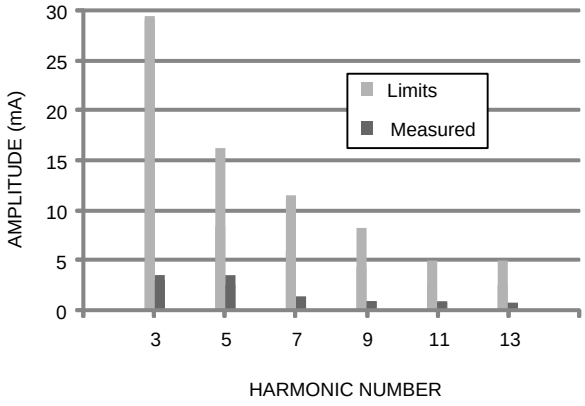


Figure 9. 120V 15W THD Measurements
EN 61000-3 Class C Limits

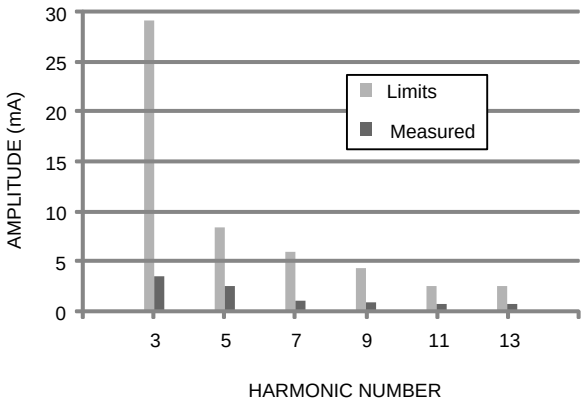
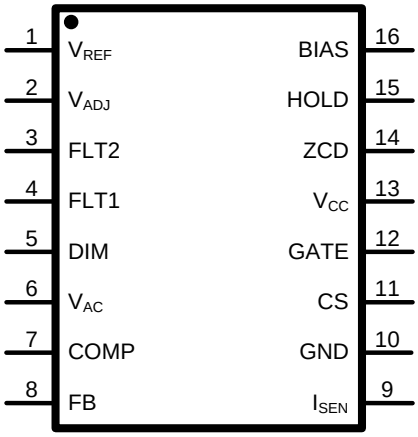


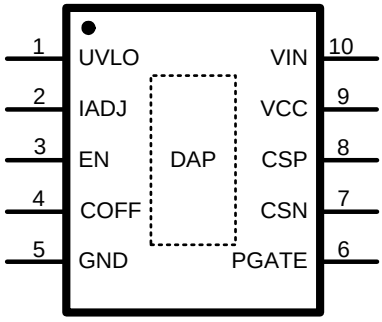
Figure 10. 230V 15W THD Measurements
EN 61000-3 Class C Limits

5 LM3450 Pin Descriptions



Pin	Name	Description	Application Information
1	V_{REF}	3V Reference	Reference Output: Connect directly to V_{ADJ} or to resistor divider feeding V_{ADJ} and to necessary external circuits.
2	V_{ADJ}	Analog Adjust	Analog Dim and Phase Dimming Range Input: Connect directly to V_{REF} to force standard 70% phase dimming range. Connect to resistor divider from V_{REF} to extend usable range of some phase dimmers or for analog dimming. Connect to GND for low power mode.
3	FLT2	Filter 2	Ramp Comparator Input: Connect a series resistor from FLT1 capacitor and a capacitor to GND to establish second filter pole.
4	FLT1	Filter 1	Angle Decoder Output: Connect a series resistor to a capacitor to ground to establish first filter pole.
5	DIM	500 HzPWM Output	Open Drain PWM Dim Output: Connect to dimming input of output stage LED driver (directly or with isolation) to provide decoded dimming command.
6	V_{AC}	SampledRectified Line	Multiplier and Angle Decoder Input: Connect to resistor divider from rectified AC line.
7	COMP	Compensation	Error Amplifier Output and PWM Comparator Input: Connect a capacitor to GND to set the compensation.
8	FB	Feedback	Error Amplifier Inverting Input: Connect to output voltage via resistor divider to control PFC voltage loop for non-isolated designs. Connect to a 5.11kΩ resistor to GND for isolated designs (bypasses error amplifier). Also includes over-voltage protection and shutdown modes.
9	I_{SEN}	Input Current Sense	Input Current Sense Non-Inverting Input: Connect to diode bridge return and resistor to GND to sense input current for dynamic hold. Connect a 0.1µF capacitor and Schottky diode to GND, and a 0.22µF capacitor to HOLD.
10	GND	Power Ground	System Ground
11	CS	Current Sense	MosFET Current Sense Input: Connect to positive terminal of sense resistor in PFC MosFET source.
12	GATE	Gate Drive	Gate Drive Output: Connect to gate of main power MosFET for PFC.Gate Drive Output: Connect to gate of main power MosFET for PFC.
13	V_{CC}	Input Supply	Power Supply Input: Connect to primary bias supply. Connect a 0.1µF bypass capacitor to ground.
14	ZCD	Zero Crossing Detector	Demagnetization Sense Input: Connect a resistor to transformer/inductor winding to detect when all energy has been transferred.
15	HOLD	Dynamic Hold	Open Drain Dynamic Hold Input: Connect to holding resistor which is connected to source of passFET.
16	BIAS	Pre-regulator Gate Bias	Pre-regulator Gate Bias Output: Connect to gate of passFET and to resistor to rectified AC (drain of passFET) to aid with startup.

6 LM3409HV Pin Descriptions



Pin	Name	Description	Application Information
1	UVLO	Input Under Voltage Lock-out	Connect to a resistor divider from V_{IN}. UVLO threshold is 1.24V and hysteresis is provided by a 22µA current source.
2	I_{ADJ}	Analog LED Current Adjust	Apply a voltage between 0 - 1.24V, or connect a resistor from this pin to GND, to set the current sense threshold voltage.
3	EN	Logic Level Enable	Apply a voltage >1.6V to enable device, a PWM signal to dim, or a voltage <0.6V for low power shutdown.
4	COFF	Off-time programming	Connect an external resistor from V_O to this pin, and a capacitor from this pin to GND to set the off-time.
5	GND	Power Ground	Connect to the system ground.
6	PGATE	Gate Drive	Connect to the gate of the external PFET.
7	CSN	Negative Current Sense	Connect to the negative side of the sense resistor.
8	CSP	Positive Current Sense	Connect to the positive side of the sense resistor (also connected to V_{IN}).
9	V_{CC}	V_{IN}-referenced Linear Regulator Output	Connect at least a 1 µF ceramic capacitor from this pin to CSN. The regulator provides power for P-FET drive.
10	V_{IN}	Input Voltage	Connect to the input voltage.
DAP	DAP	Thermal PAD on bottom of IC	Connect to pin 5 (GND). Place 4-6 vias from DAP to bottom layer GND plane.

7 Simplified Evaluation Board Schematic

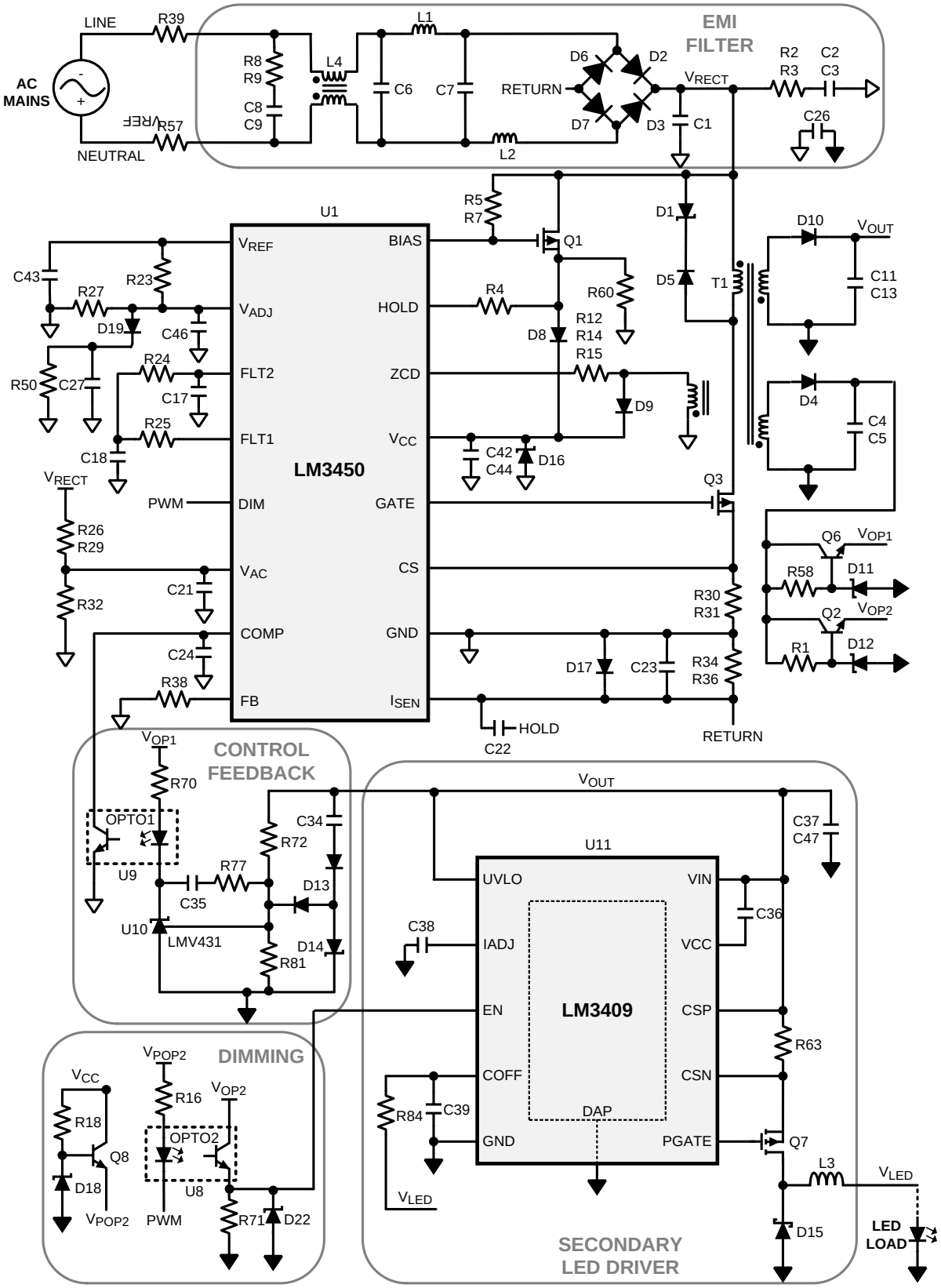


Figure 11. Simplified Board Schematic

8 Design Information

The following section explains how to design using the LM3450 power factor controller and phase dimming decoder. Refer to *AN-1953 LM3409HV Evaluation Board* (SNVA390) for a detailed design procedure of the LM3409HV secondary stage and to the *LM3450/A LED Drivers with Active Power Factor Correction and Phase Dimming Decoder*(SNVS681) data sheet for specific details regarding the function of the LM3450 device. All reference designators refer to the Figure 11. Note that parallel and series resistances are combined in one schematic symbol for simplification. To improve readability of this design document, each sub-section is followed by a list of definitions for new terms used in the calculations. Section 10 should be consulted for I/O connections and test points. There is also a Bill of Materials for each assembly version.

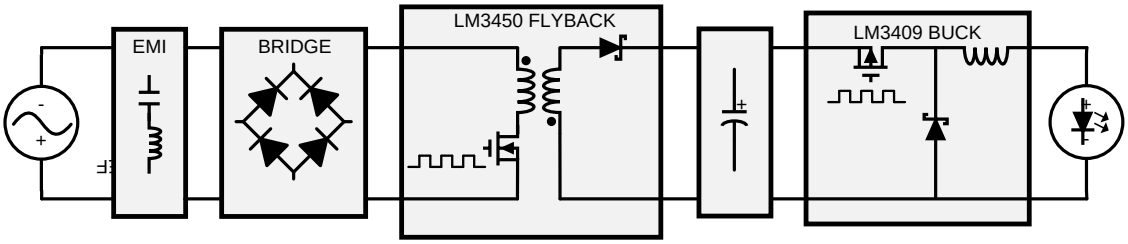


Figure 12. Two-Stage PFC LED Driver

8.1 1ST Stage - CRM Flyback

The first stage of the evaluation board PFC LED Driver is a critical conduction mode (CRM) flyback converter controlled with the LM3450. CRM converters operate at the boundary of continuous conduction mode (CCM) and discontinuous conduction mode (DCM). CRM is implemented by turning on the main switching FET (Q3) until the primary current rises to a peak threshold. Q3 is then turned off and the current falls until a zero crossing is detected. At this point, Q3 is turned on and the cycle repeats.

In the CRM flyback PFC application shown, the rectified AC input is fed forward to the control loop, yielding a sinusoidal peak current threshold. This peak threshold creates a sinusoidal primary peak current envelope $I_{P\text{-}pk}$ as shown in . The secondary peak current envelope $I_{S\text{-}pk}$ will simply be a scaled version of the primary according to the turns ratio of the transformer. Assuming good attenuation of the switching ripple via the EMI filter, the average input current $I_{IN}(t)$ can also be approximated as a sinusoid. Since the input current has the same shape and phase as the input voltage, high power factor (PF) can easily be achieved.

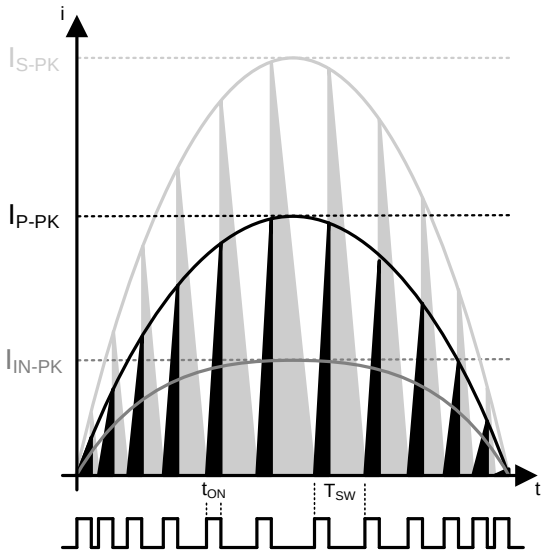


Figure 13. CRM Flyback Current Waveforms

The input current shaping happens instantly in CRM due to the feed-forward mechanism; however, the converter must also regulate the flyback output voltage with a traditional feedback loop. This is accomplished with a narrow bandwidth error amplifier coupled with energy storage capacitance at the output to limit the twice line frequency ripple. The output of the error amplifier is multiplied with the scaled rectified AC voltage to achieve both input current shaping and output voltage regulation. Refer to the datasheet for a more detailed explanation of the power factor controller.

The LM3450 also has a phase decoder that interprets the phase dimming angle and maps it to a 500Hz PWM open-drain output. This signal is then be directly connected to an opto-isolator to send across the isolation boundary to the second stage LED driver. In addtion, the LM3450 provides a dynamic hold circuit to ensure that the holding current requirement is satisfied in forward phase dimmers.

8.2 2ND Stage - Buck LED Driver

The second stage of the evaluation board PFC LED Driver is a buck LED driver controlled with the LM3409HV. The input to this stage is the flyback output voltage and the output is a regulated constant current of 350mA to a stack of <45V of LEDs. The LM3409HV is a hysteretic PFET controller using peak current detection and a constant off-timer to provide regulated LED current with a constant switching frequency ripple. Coupled with the flyback energy storage capacitance, the LM3409 is able to remove all 120HZ ripple content from the LED output. The 500Hz PWM signal from the first stage is used as the dimming input to the LM3409HV. The output of the opto-isolator is connected directly to the DIM pin to provide a PWM dimmed LED current according to the detected phase angle at the primary.

The LM3409HV design is not included in this document. Refer to AN-1953 for a detialed design procedure. The specifications for the second stage are:

- Nominal Input Voltage = 50V
- Regulated LED Current = 350mA
- Nominal LED Stack Voltage = 45V
- Switching Frequency at Nominal Input = 100kHz
- Inductor/LED Current Ripple = 100mA

8.3 CRM Flyback Converter

Operating Points

The AC mains voltage, at the line frequency f_L, is assumed to be perfectly sinusoidal and the diode bridge ideal. This yields a perfect rectified sinusoid at the input to the flyback. The input voltage $V_{in}(t)$ is defined in terms of the peak input voltage:

$$V_{in}(t) = V_{IN\text{-}PK} \times \left|\sin(2 \times \pi \times f_L \times t)\right|$$
$$V_{IN\text{-}PK} = V_{IN} \times \sqrt{2} \quad (1)$$

The controller and the transformer are also assumed to be ideal. These assumptions yield a sinusoidal peak primary current envelope $I_{P\text{-}pk}(t)$ and peak secondary current envelope $I_{S\text{-}pk}(t)$ as shown in . Both are defined in terms of the peak primary current:

$$I_{P\text{-}pk}(t) = I_{P\text{-}PK} \times \left|\sin(2 \times \pi \times f_L \times t)\right|$$
$$I_{S\text{-}pk}(t) = n \times I_{P\text{-}pk}(t) \quad (2)$$

The output voltage reflected to the primary is defined:

$$V_R = n \times V_{OUT} \quad (3)$$

CRM control yields a variable duty cycle over a single line cycle with a minimum occurring at the peak input voltage:

$$D(t) = \frac{V_R}{V_R + V_{in}(t)}$$
$$D_{MIN} = \frac{V_R}{V_R + V_{IN\text{-}PK}} \quad (4)$$

The resulting sinusoidal average input current $I_{in}(t)$, shown in , is approximated as the average of each triangular current pulse during a switching period. The peak input current occurs at the peak primary current:

$$I_{in}(t) = \frac{I_{P-PK} \times D(t)}{2}$$
$$I_{IN-PK} = \frac{I_{P-PK} \times D_{MIN}}{2} \quad (5)$$

Turns Ratio

The first thing to decide with an isolated design is the desired transformer turns ratio. This should be based on the specified output voltage and the maximum peak input voltage. Frequently the MosFET is already chosen for a design, given its cost and availability. With a desired MosFET voltage, the maximum reflected voltage at the primary is calculated:

$$V_{R-MAX} = \frac{2}{3} \times (V_{T-DES-MAX} - V_{IN-PK-MAX}) \quad (6)$$

Generally, an integer turns ratio is selected to achieve a reflected voltage at or below the defined maximum:

$$n < \frac{V_{R-MAX}}{V_{OUT}} \quad (7)$$

Switching MosFET

The main switching MosFET (Q3) can be sized as desired; to block the maximum drain-to-source voltage, operate at the maximum RMS current, and dissipate the maximum power:

$$V_{T-MAX} = V_{IN-PK-MAX} + (1.5 \times V_R)$$
$$I_{T-PK-MAX} = I_{P-PK-MAX}$$
$$I_{T-RMS-MAX} = I_{P-PK-MAX} \times \sqrt{\frac{D_{@IIN-PK-MAX}}{3}}$$
$$P_{T-MAX} = I_{T-RMS-MAX}^{2} \times R_{DS-ON} \quad (8)$$

The peak current limit should be at least 25% higher than the maximum peak input current:

$$R30 \,||\, R31 = \frac{1.5V}{I_{LIM}} \quad (9)$$

The parallel sense resistor combination (R30||R31) has to dissipate the maximum power:

$$P_{R30||R31} = I_{T-RMS-MAX}^{2} \times R30 \,||\, R31 \quad (10)$$

Switching Diode

The main switching diode (D10) should be sized to block the maximum reverse voltage , operate at the maximum average current, and dissipate the maximum power:

$$V_{RD-MAX} = V_{OUT} + \left(\frac{V_{IN-PK-MAX}}{n}\right)$$
$$I_{D-MAX} = I_{IN-PK-MAX} \times 2$$
$$I_{D-PK-MAX} = I_{P-PK-MAX} \times 2$$
$$P_{D-MAX} = I_{D-MAX} \times V_{FD} \quad (11)$$

Definitions

n – Primary to Secondary Turns Ratio

V_{OUT} – Regulated Output Voltage

V_{IN} – Nominal AC Input Voltage

V_{IN-PK} – Peak Input Voltage

$V_{IN-PK-MAX}$ – Maximum Peak Input Voltage

I_{P-PK} – Peak Primary Current

I_{S-PK} – Peak Secondary Current

I_{IN-PK} – Peak Input Current

I_{LIM} – Peak Current Limit

D_{MIN} – Minimum Duty Cycle over Line Cycle

V_R – Output Voltage Reflected to Primary

V_{R-MAX} – Maximum Tolerable Reflected Voltage

$V_{T-DES-MAX}$ – Maximum Tolerable MosFET Voltage

V_{T-MAX} – Maximum MosFET Blocking Voltage

$I_{T-RMS-MAX}$ – Maximum MosFET RMS Current

$I_{T-PK-MAX}$ – Maximum MosFET Peak Current

P_{T-MAX} – Maximum MosFET Power Dissipation

V_{RD-MAX} – Maximum Diode Blocking Voltage

I_{D-MAX} – Maximum Diode Average Current

$I_{D-PK-MAX}$ – Maximum Diode Peak Current

P_{D-MAX} – Maximum Diode Power Dissipation

8.4 Transformer

Primary Inductance

The maximum peak input current, occurring at the minimum AC voltage peak, determines the necessary flyback transformer energy storage. As a general rule of thumb, the desired duty cycle at this worst-case operating point should be specified near 0.5 to limit large conduction losses associated with high voltage diodes. The maximum input current can be approximated by the maximum output power, expected converter efficiency, and minimum input voltage. Note that there is also a 0.85 multiplier to account for the fact that maximum power with a triac dimmer in-line is demanded at approximately 85% of the full sinusoidal voltage waveform. Given the desired duty cycle, the maximum peak input current and corresponding maximum peak primary current can be approximated:

$$I_{IN-MAX} = \frac{P_{OUT-MAX}}{\eta \times 0.85 \times V_{IN-MIN}}$$
$$I_{IN-PK-MAX} = I_{IN-MAX} \times \sqrt{2}$$
$$I_{P-PK-MAX} = \frac{2 \times I_{IN-PK-MAX}}{D_{@IIN-MAX-PK}} \quad (12)$$

Using the calculated turns ratio and the desired minimum switching frequency, the minimum necessary primary inductance is calculated:

$$L_{P-MIN} > \frac{D_{MIN@IIN-PK-MAX}{}^2 \times V_{IN-MIN}}{2 \times f_{SW-MIN-DES} \times I_{IN-PK-MAX}} \quad (13)$$

Switching Frequency Range

Given a primary inductance that meets the above constraint, the variable switching frequency has the following limits:

$$f_{SW-MAX} = \frac{V_{IN-PK}}{L_P \times I_{P-PK}}$$
$$f_{SW-MIN} = \frac{V_{IN-PK} \times V_R}{L_P \times I_{P-PK} \times (V_R + V_{IN-PK})} \quad (14)$$

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Transformer Geometries and Materials

The length of the gap necessary for energy storage in the flyback transformer can be determined numerically; however, this can lead to non-standard designs. Instead, an appropriate A_L core value (160nH/turns2 is a good standard value to start with) can be chosen that will imply the gap size. A_L is an industry standard used to define how much inductance, per turns squared, that a given core can provide. With the initial chosen A_L value, the number of turns on the primary and secondary are calculated:

$$N_P = \sqrt{\frac{L_P}{A_L}}$$
$$N_S = \frac{N_P}{n} \tag{15}$$

Given the switching frequency range and the maximum output power, a core size can be chosen using the vendor's specifications and recommendations. This choice can then be validated by calculating the maximum operating flux density given the core cross-sectional area of the chosen core.

$$B_{MAX} = \frac{L_P \times I_{P\text{-}PK\text{-}MAX}}{N_P \times A_{E\text{-}MAX}} \tag{16}$$

With most common core materials, the maximum operating flux density should be set between 300mT and 325mT. If the calculation is below this range, then A_L should be increased to the next standard value and the turns and maximum flux density calculations iterated. If the calculation is above this range, then A_L should be decreased to the next standard value and the turns and maximum flux density calculations iterated.

With the flux density appropriately set, the core material for the chosen core size can be determined using the vendor's specifications and recommendations. Note that there are core materials that can tolerate higher flux densities; however, they are usually more expensive and not practical for these designs.

The rest of the transformer design can be done with the aid of the manufacturer. There are calculated trade-offs between the different loss mechanisms and safety constraints that determine how well a transformer performs. This is an iterative process and can ultimately result in the choice of a new core or switching frequency range. The previous steps should reduce the number of iterations significantly but a good transformer manufacturer is invaluable for completion of the process.

Definitions

η – Expected converter efficiency

$P_{OUT\text{-}MAX}$ – Maximum Output Power

$V_{IN\text{-}MIN}$ – Minimum RMS AC Line Voltage

$V_{IN\text{-}PK\text{-}MIN}$ – Minimum Peak Input Voltage

$I_{IN\text{-}PK\text{-}MAX}$ – Maximum Peak Input Current

$I_{P\text{-}PK\text{-}MAX}$ – Maximum Peak Primary Current

$D_{@IIN\text{-}PK\text{-}MAX}$ – Duty Cycle at Maximum Peak Input Current

$L_{P\text{-}MIN}$ – Minimum Necessary Primary Inductance

L_P – Primary Inductance

$f_{SW\text{-}MIN\text{-}DES}$– Desired Minimum Switching Frequency

$f_{SW\text{-}MIN}$ – Minimum Switching Frequency

$f_{SW\text{-}MAX}$ – Maximum Switching Frequency

N_P – Number of Primary Turns

N_S – Number of Secondary Turns

$A_{E\text{-}MAX}$ – Core Cross-Sectional Area

B_{MAX} – Maximum Operating Flux Density

A_L – Transformer Core Figure of Merit

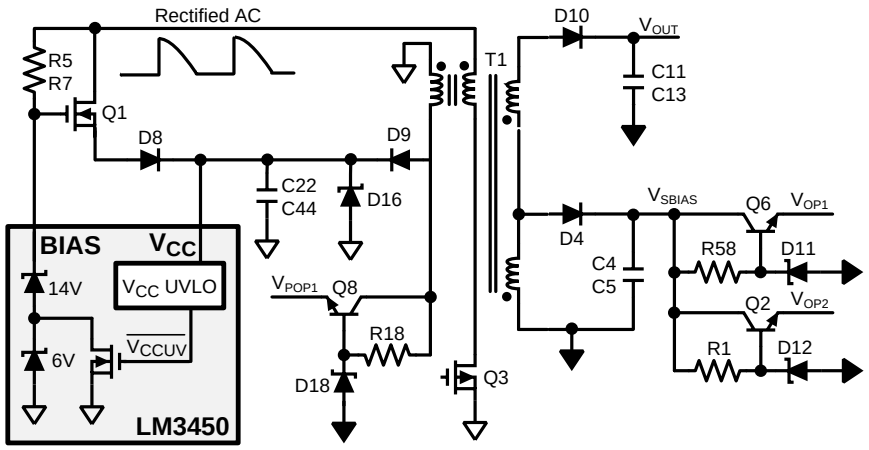


Figure 14. Bias Circuitry

8.5 Bias Supplies and Capacitances

Bias Supplies

The primary bias supply shown in Figure 14 enables instant turn-on through Q1 while providing an auxiliary winding for high efficiency steady state operation. The two bias paths are each connected to V_{CC} through a diode (D8, D9) to ensure the higher of the two is providing V_{CC} current. The LM3450 BIAS pin helps to ensure that the auxiliary winding is always providing V_{CC} during normal operation.

Since there is optical isolation, a secondary bias supply is also necessary. This is accomplished with another auxiliary winding, diode (D4), and capacitance (C4) which creates another flyback output that scales with the regulated output (similar to the auxiliary primary bias winding). During transient conditions, the regulated output voltage may dip or spike due to the low bandwidth of the regulation loop. To ensure the secondary bias moves highly proportional to the regulated flyback output, the output winding is tapped to provide the secondary bias.

It is also advantageous to linear regulate down to approximately 9V, from the 12V bias supplies, for every opto-isolator supply rail (V_{POP1}, V_{OP1}, V_{OP2}) . This will stabilize the opto-isolator rail over the entire operating range, preventing noise coupling into COMP and the dimming input of the LM3409.

The primary and secondary bias outputs for both versions of the evaluation board are set to 12V at the nominal input voltage. A transformer turns ratio and corresponding turns calculation is used to size the primary auxiliary winding and determine the tap point for the secondary winding:

$$n_{AUX} = \frac{V_{OUT}}{V_{CC}}$$

$$N_A = \frac{N_S}{n_{AUX}} \quad (17)$$

The minimum primary bias supply capacitance is calculated, given a minimum V_{CC} ripple specification, to keep V_{CC} above UVLO at the worst-case current:

$$C44 = \frac{I_{CC}}{\Delta v_{CC} \times f_{2L}} \quad (18)$$

Input Capacitance

The input capacitor of the flyback (C1) has to be able to provide energy during the worst-case switching period at the peak of the AC input. C1 should be a high frequency, high stability capacitor (usually a metallized film capacitor, either polypropylene or polyester) with an AC rating equal to the maximum input voltage. C1 should also have a DC voltage rating exceeding the maximum peak input voltage + half of the peak to peak input voltage ripple specification. The minimum required input capacitance is calculated given the same ripple specification:

$$C1 = \frac{L_P \times I_{P\text{-}PK\text{-}MAX}^2}{\left(V_{IN\text{-}PK\text{-}MIN} + \frac{\Delta v_{IN\text{-}PK}}{2}\right)^2 - \left(V_{IN\text{-}PK\text{-}MIN} - \frac{\Delta v_{IN\text{-}PK}}{2}\right)^2} \quad (19)$$

Output Capacitance

Since the LM3450 is a power factor controller, C1 is minimized and the output capacitor (C11) serves as the main energy storage device. C11 should be a high quality electrolytic capacitor that can tolerate the large current pulses associated with CRM operation. The voltage rating should be at least 25% greater than the regulated output voltage and, given the desired voltage ripple, the minimum output capacitance is calculated:

$$C11 = \frac{P_{OUT\text{-}MAX}}{2 \times \pi \times f_L \times V_{OUT} \times \Delta v_{OUT}} \quad (20)$$

Definitions

$\Delta v_{IN\text{-}PK}$ – Peak Input Voltage Switching Ripple

Δv_{OUT} – Nominal Output Voltage Ripple

Δv_{CC} – Nominal Primary Bias Ripple

V_{CC} – Primary Bias Capacitance

n_{AUX} – Primary to Auxiliary Turns Ratio

N_A – Number of Auxiliary Turns

f_{2L} – Twice Line Frequency

8.6 Dimming Decoder and Hold Current

Dynamic Hold

The LM3450 regulates the minimum input current with a dynamic hold circuit to ensure the triac holding current requirement is satisfied. The regulated minimum current is set by choosing the sense resistor (R34||R36):

$$I_{IN\text{-}MIN\text{-}REG} = \frac{200\,mV}{R34 \,||\, R36} \quad (21)$$

The maximum possible holding current (usually occurs during transients when triac fires) is set by choosing the hold resistor (R12||R14||R15) between the source of the Q1 and HOLD:

$$I_{HOLD\text{-}MAX} = \frac{V_{CC}}{R12 \,||\, R14 \,||\, R15 + 30\Omega} \quad (22)$$

Fixed Hold

Since the dynamic hold only regulates the minimum input current during a sample period, the other periods potentially misfire. This can be a problem if the misfire is early in the cycle because the energy transfer to the output is severely reduced and the control loop has to respond to a large system transient at the sampling frequency. A simple effective solution to this problem is to add some fixed holding current after the diode bridge. This can be done by placing a fixed resistance from the source of Q1 to GND. A general rule of thumb is to burn 1 or 2% of total system power in the fixed hold resistance for best system performance. This will help properly shape the energy transfer during non-sampled cycles and will reduce potential lifetime concerns with snubber and damper circuits that could see multiple misfires per cycle.

PassFET

The passFET (Q1) is used in its linear region to stand-off the line voltage from the LM3450 controller. Both the V_{CC} startup current and the phase dimmer holding current are conducted through the device. Since the holding current is far larger than the startup current and is added regularly, it will dominate the calculations. Given this, Q1 has to block the maximum peak input voltage and conduct the maximum holding current at the sampling interval. The surge handling capability of Q1 is also important and is evaluated by looking at the safe operating area (SOA) of the device. Finally, Q1 needs to be able to dissipate the maximum power. The design equations are:

$$V_{Q1} = V_{IN\text{-}PK\text{-}MAX}$$
$$I_{Q1} = \frac{I_{HOLD\text{-}MAX}}{10}$$
$$P_{Q1} = \frac{2 \times V_{Q1} \times I_{Q1}}{\pi} \quad (23)$$

Angle Sense

V_{AC} is a dual input for both the PFC multiplier and the angle decoder. The resistor divider (R26+R29, R32) should be sized according to the desired angle detect voltage V_{DET}. A general rule of thumb is to set V_{DET} = V_{IN}/5 and choose R26+R29 between 1MΩ and 2MΩ to limit power dissipation.

$$R32 = \frac{356\,mV \times (R26 + R29)}{V_{DET} - 356\,mV} \quad (24)$$

Filters

The filters (FLT1, FLT2) are chosen to provide the desired dimming transition response (how the light changes during dimmer movement). The filter frequency should be set between 2Hz and 10Hz for best operation (2Hz has a fade feeling, 10Hz is very snappy). The capacitors (C17, C18) can both be set to 1µF for all designs and given the filter frequencies, the resistors (R24, R25) are calculated:

$$R24 = \frac{1}{2 \times \pi \times f_{FLT2} \times C17}$$
$$R25 = \frac{1}{2 \times \pi \times f_{FLT1} \times C18} \quad (25)$$

Opto-Isolator

A standard low cost opto-isolator (can be the same kind that is used for feedback of the output voltage) is used to transfer the dimming command from DIM to the secondary. It needs to be driven with at least 1-2mA of current to obtain full 70:1 contrast ratio (more current creates faster edges). The output of the opto-isolator should be clamped to just above the DIM input threshold of the secondary driver. This is accomplished with a 1.8V Zener clamp (D22) at the EN pin of the LM3409 on the evaluation boards.

Relevant Definitions

$I_{IN\text{-}MIN\text{-}REG}$ – Regulated Minimum Input Current

$I_{HOLD\text{-}MAX}$ – Maximum Hold Current

V_{DET} – Rectified AC Angle Detect Voltage

f_{FLT1} – FLT1 frequency

f_{FLT2} – FLT2 frequency

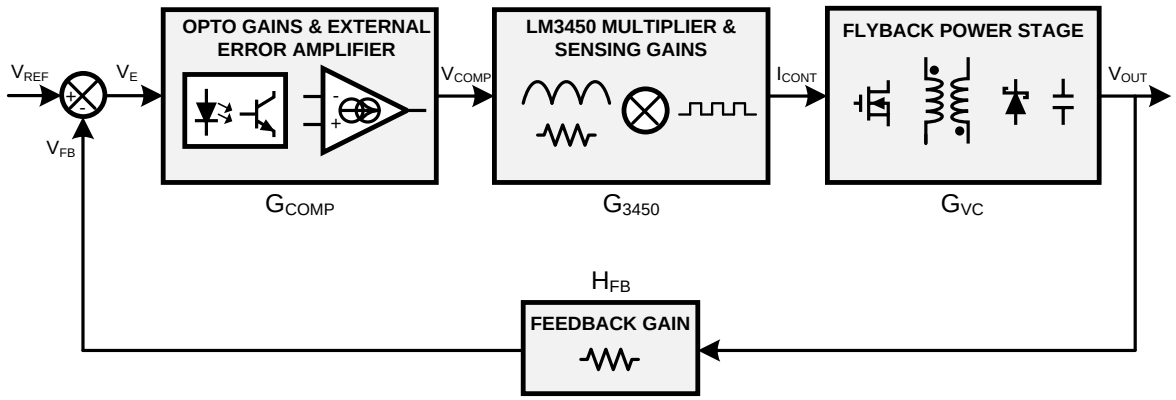


Figure 15. Control Loop Block Diagram

8.7 Voltage Control Loop

The CRM topology requires a narrow bandwidth voltage control loop to regulate the output voltage. This loop needs to be compensated to maintain stability over the desired operating range. The flyback topology is isolated, therefore the LM3450 internal error amplifier is bypassed and an external secondary side error amplifier is used instead. The control loop shown in Figure 15 is comprised of the converter control-to-output transfer function, the compensator transfer function, and all of the other gains in the loop.

The output voltage is sensed with a resistor divider (R81, R72):

$$R81 = \frac{1.24V \times R72}{V_{OUT} - 1.24V} \tag{26}$$

The converter control-to-output transfer function can be approximated as a single pole system:

$$G_{VC}(s) = G_{C0} \times \frac{1}{\left(1 + \frac{s}{\omega_{P1}}\right)}$$

$$\omega_{P1} = \frac{P_{OUT-MAX}}{V_{OUT}^{2} \times C11}$$

$$G_{C0} = \frac{V_{OUT}}{I_{P-PK}} \tag{27}$$

The feedback gain (H_{FB}) is unity due to the control implementation and the LM3450 device and external gains are defined:

$$G_{3450} = \frac{5k\Omega \times CTR \times K_V \times 0.55\frac{1}{V} \times V_{IN-PK}}{(R30 \,||\, R31) \times R70}$$

$$K_V = \frac{R32}{R32 + (R26 + R29)} \tag{28}$$

A standard PI compensator is used on the secondary to stabilize the system. The error amplifier is implemented with an LMV431 and a series resistor (R77) and capacitor (C35) in the feedback path as shown in Figure 16. The output of the LMV431 is tied to the cathode of the opto photo-diode. A resistor (R70 = 2kΩ) from the anode of the photodiode to the bias rail provides the current path and ultimately the output voltage swing of the secondary error amplifier. The primary side of the opto is connected directly to COMP. With the 5kΩ internal pull-up resistor, the maximum current through the primary side of the opto will be 1mA. A higher frequency roll-off pole is placed on the primary in the form of a capacitor (C24) from COMP to GND. The resistor divided flyback output voltage is regulated to the 1.24V LMV431 internal reference. Note the additional soft-start circuit using C34, D13, and D14.

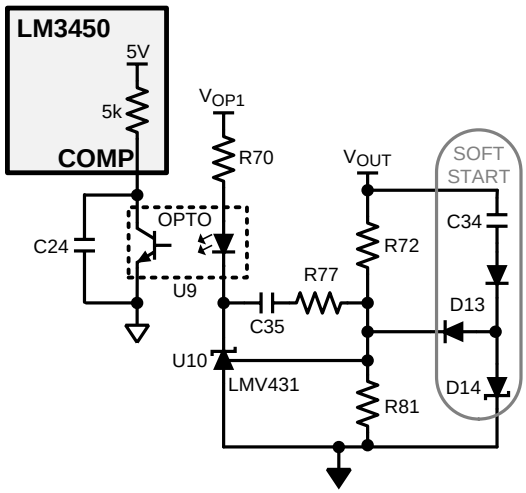


Figure 16. Secondary Error Amplifier Circuit

The compensator transfer function is defined:

$$G_{COMP}(s) = \frac{\left(1+\frac{s}{\omega_{Z1}}\right)}{\left(\frac{s}{\omega_{P2}}\right) x \left(1+\frac{s}{\omega_{P3}}\right)} \quad (29)$$

Where the secondary compensator pole is defined:

$$\omega_{P2} = \frac{1}{R72 \, x \, C35} \quad (30)$$

And the compensator zero is defined:

$$\omega_{Z1} = \frac{1}{R77 \, x \, C35} \quad (31)$$

And the primary roll-off pole is defined:

$$\omega_{P3} = \frac{1}{5 \, k\Omega \, x \, C24} \quad (32)$$

The resulting control loop gain is

$$T(s) = G_{COMP}(s) \, x \, G_{3450} \, x \, G_{VC}(s) \, x \, H_{FB} \quad (33)$$

The compensator design for this system can be complicated; however with some useful assumptions, it can be made simple. Looking at the total DC gain ($G_{3450}xG_{C0}xH_{FB}$), the following can be made relatively constant over all designs:

- R70 = 2kΩ, the 5kΩ internal pull-up, and the 0.55 multiplier gain.
- The opto CTR, though variable over temperature, given a fixed supply rail and a fixed R70 value.

In several cases, the product of two DC gain terms can also be identified as relatively constant over all designs if all of the previous LM3450 design methodology is observed:

- V_{INPK} and K_V are almost exactly inversely proportional (given the V_{DET} specification method).
- I_{P-PK} and R30||R31 are closely inversely proportional (given the I_{LIM} specification method).

Given these relationships and following the complete LM3450 design method, the DC gain should only vary largely with change in output voltage (directly proportional).

The output pole of the converter on the other hand follows these basic relationships:

- $P_{OUT-MAX}$ and C11 are exactly directly proportional given a fixed output ripple specification, therefore there is no relative change to ω_{P1}.
- V_{OUT} is exactly inversely proportional to ω_{P1} given a fixed output ripple specification.

With the opposing conditions of the output pole moving inversely proportional to V_{OUT} and the DC gain moving proportional to V_{OUT}, the net result gives a very consistent uncompensated loop gain. Because of this, a fixed compensator can be used. During prototyping, If stability becomes a concern, the R77 value can be incresed or decreased slightly to provide more phase margin and better stability. In general the compensator calculated in the Design Calculations section is sized to provide around 40° phase margin at a crossover frequency of 40Hz. This is a fairly high bandwidth for a PFC converter which will cause there to be some 120Hz ripple on COMP. This will decrease PF but improve transient response which is very helpful in phase dimmable applications.

Relevant Definitions

$G_{VC}(s)$ – Converter Control-to-Output Transfer Function

G_{CO} – Converter Control-to-Output DC Gain

G_{3450} – LM3450 and External Gains

$G_{COMP}(s)$ – Compensator Transfer Function

H_{FB} – Feedback Gain

ω_{P1} – Converter Output Pole

ω_{P2} – Compensator Secondary Integrator Pole

ω_{Z1} – Compensator Secondary Zero

ω_{P3} – Compensator Primary HF Pole

T(s) – Total Loop Gain

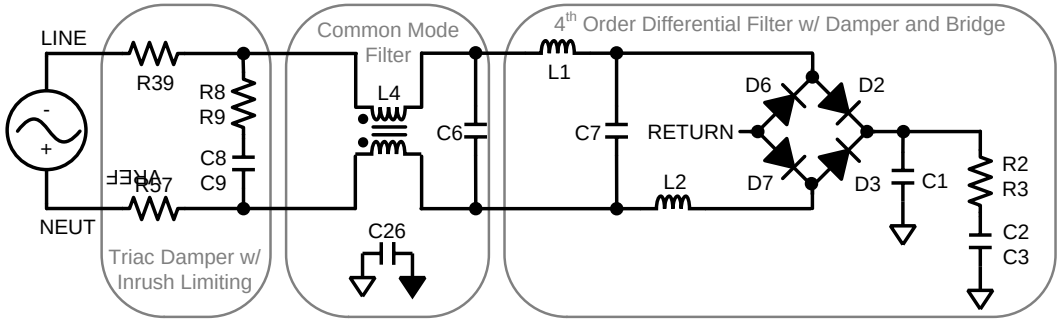


Figure 17. Input EMI Filter

8.8 Input Filter

Background

Since the LM3450 is used for AC to DC systems, electromagnetic interference (EMI) filtering is critical to pass the necessary standards for both conducted and radiated EMI. This filter will vary depending on the output power, the switching frequencies, and the layout of the PCB. There are two major components to EMI: differential noise and common-mode noise. Differential noise is typically represented in the EMI spectrum below approximately 500kHz while common-mode noise shows up at higher frequencies.

Conducted

Figure 17 shows a typical filter used with an LM3450 design. To conform to conducted standards, a fourth order filter (C1, L2, C7, L1) is implemented using shielded inductors and X rated AC capacitors. This, if sized properly can provide ample attenuation of the switching frequency and lower order harmonics contributing to differential noise. For common-mode noise, a common mode choke (L4) and a capacitor (C6) can be used to filter higher frequency content. A Y rated AC capacitor (C26) from the primary ground to the secondary ground is also critical for reduction of common mode noise. This combination of filters, along with any necessary damping (R2, R3, C2, C3), can easily provide a passing conducted EMI signature.

Radiated

Conforming to radiated EMI standards is much more difficult and is completely dependent on the entire system including the enclosure. C26 will also greatly help reduce radiated EMI; however, reduction of dV/dt on switching edges and PCB layout iterations are frequently necessary as well. Consult available literature and/or an EMI specialist for help with this. It can be a daunting task.

Interaction with Dimmers

In general, input filters and forward phase dimmers do not work well together. The triac needs a minimum amount of holding current to function. The converter itself is demanding a certain amount of current from the input to provide to its output. With no filter, the difference of the necessary hold current and the converter current is provided by the LM3450 dynamic hold circuit during a sampling interval. Unfortunately, the actual dimmer current is not being monitored; instead a filtered version is being measured. In reality, the input filter is providing or taking current depending upon the dV/dt of the capacitors. The discrepancy between the measured input current at ISEN and the actual input current through the triac is the worst at the highest dV/dt of the input filter capacitors. The best way to deal with this problem is to minimize filter capacitance and increase the regulated hold current until there is enough current to satisfy the dimmer and filter simultaneously.

8.9 Inrush Limiting, Damping and Clamping

Clamp

Figure 19 shows a large ringing (V_{RING}) on the Q3 drain due to the leakage inductance of the transformer and output capacitance of Q3. A clamp circuit is necessary to prevent damage to Q3 from excessive voltage. The evaluation boards use a transil (TVS) clamp, shown in Figure 18

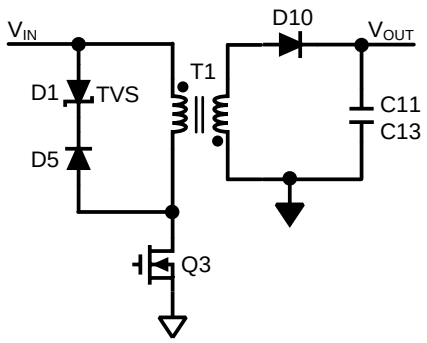


Figure 18. Transil Clamp

When Q3 is on and the drain voltage is low, the blocking diode (D5) is reverse biased and the clamp is inactive. When the MosFET is turned off, the drain voltage rises past the nominal voltage (reflected voltage plus the input voltage). If it reaches the TVS clamp voltage + the input voltage, the clamp prevents any further rise. The TVS diode (D1) voltage is set to prevent the MosFET from exceeding its maximum rating:

$$V_{TVS-D1} \leq \frac{3}{2} \times V_R \tag{34}$$

This clamp method is fairly efficient and very simple compared to other commonly used methods. Note that if the the ringing is large enough that the clamp activates, the ringing energy is radiated at higher frequencies. Depending on PCB layout, EMI filtering method, and other application specific items, the transil clamp can present problems conforming to radiated EMI standards. If the transil clamp becomes problematic, there are many other clamp options easily found in a basic literature search.

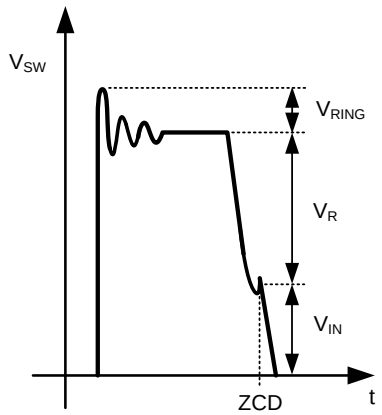


Figure 19. Switch Node Ringing

Inrush

With a forward phase dimmer, a very steep rising edge causes a large inrush current every cycle as shown in Figure 20. Series resistance (R39, R57) can be placed between the filter and the triac to limit the effect of this current on the converter and to provide some of the necessary holding current at the same time. This will, of course, degrade efficiency but some inrush protection is always necessary in any AC system due to startup. The size of R39 and R57 are best found experimentally as they provide attenuation for the whole system.

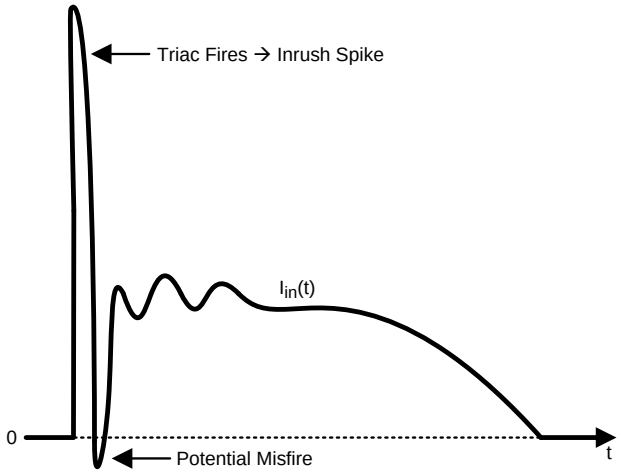


Figure 20. Inrush Current Spike

Damper

The inrush spike also excites a resonance between the input filter of the triac and the input filter of the converter. The associated interaction can cause the current to ring negative, as shown in Figure 20, thereby shutting off the triac. The triac damper (R8, R9, C8, C9), shown in Figure 17, is placed between the dimmer and the EMI filter to absorb some of the ringing energy and reduce the potential for misfires. The damper is also best sized experimentally due to the large variance in triac input filters.

8.10 Transient Performance

Startup

When using the LM3450 with a phase dimmer, startup can be very disruptive. Any time the dimmer is turned on (via a separate switch or some state where the dimmer has been previously disconnected from its load), the LM3450 will attempt to bring the system to regulation. Because phase dimmers can be turned on and off quickly, the system capacitances may or may not be fully discharged, this can lead to a large variance in startup conditions. The best way to control startup transients is to softstart the dimming command. This can be accomplished by placing a diode (D19), capacitor (C27) and resistor (R50) off the V_{ADJ} pin as shown in Figure 21. D19 should have a very low forward voltage and C27 should be between 10µF and 47µF. R50 is placed across the capacitor to help discharge the capacitor when the LM3450 is shut-off.

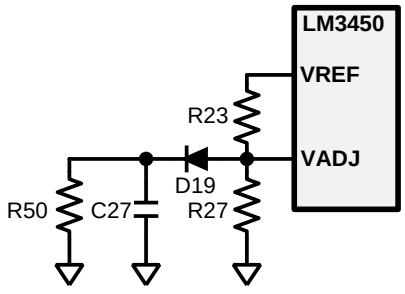


Figure 21. DIM Soft-start Circuit

Fast Dim Down

During quick phase dimmer movement, the effective line transient can cause problems with any phase dimmer. This is because a quick line transient is followed by a slow load transient. This problem only really surfaces with a quick decreasing line transient of fairly large magnitude (aka forcing the dimmer from high to low quickly).

Effectively, the input energy is reduced immediately, but the request for decreased output energy is delayed. Since the output is potentially demanding more energy than the input can produce instantaneously, the control loop will attempt to re-regulate by providing as much energy as possible to the output.

With a large enough transient, the output will sag causing a potential change in output current if the LM3409 goes into dropout. Given the added delay of sampling inherent to the LM3450 controller, a flutter or bobble of light can be magnified This will only happen during the transient, so designers probably won't care for many applications.

To mitigate this problem in high end applications, a circuit is shown in Figure 22 (NOT shown in *Simplified Evaluation Board Schematic* but exists on evaluation boards) to feed-forward the average line voltage to the LM3450 and force a quick sample period. This method takes the rectified AC and scales and filters it to a DC voltage with some resistors and capacitors (R20, R21, R52, R53, C14, C15). The dV/dt edge of this signal is AC coupled to a PFET (Q4) gate to create a 10's of ms pulse. The signal is then inverted, ac coupled again, and sent to the NFET (Q5) gate. This creates a small reset pulse on V_{ADJ}.

Pulling V_{ADJ} low for over 10µs will reset the sampling block and force the quickest possible sample. At the same time, FLT1 will immediately be set to minimum and the fastest filters will be enabled.

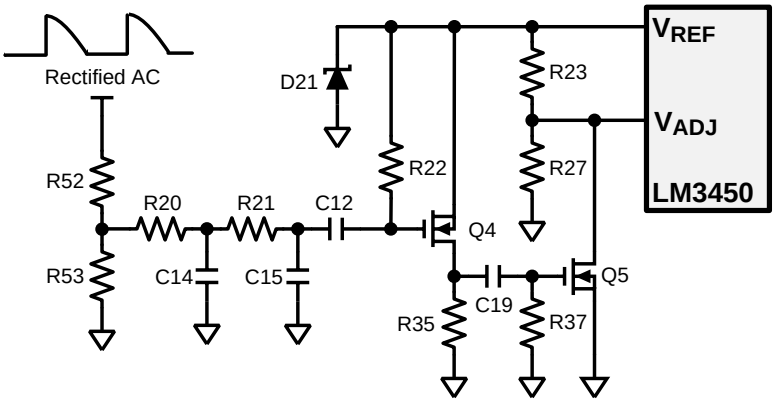


Figure 22. Line Feed-forward Circuit

9 Design Calculations - 120V, 15W

The following is a step-by-step procedure with calculations for the 120V 15W evaluation board. The 230V calculations can be done in the same manner. Many components are identical between both boards for simplicity, therefore some components on the 120V board are over-sized.

9.1 Specifications

f_L – 60Hz

f_{SW-MIN}– 40kHz

V_{IN} – 120V_{AC}

V_{IN-MIN} – 85V_{AC}

V_{IN-MAX} – 135V_{AC}

I_{LED} – 350mA

Δv_{OUT} = 1V

Δv_{IN-PK} = 35V

$I_{P-PK-LIM}$ = 1.65A

$V_{T-DES-MAX}$ = 400V

$P_{OUT-MAX}$ = 15W

$D_{@IIN-MAX-PK}$ = 0.6

V_{OUT} = 50V

9.2 Preliminary Calculations

Maximum peak input voltage:

$$V_{IN-PK-MAX} = 135V \times \sqrt{2} = 191V \quad (35)$$

Minimum peak input voltage:

$$V_{IN-PK-MIN} = 85V \times \sqrt{2} = 120V \quad (36)$$

Maximum average input current:

$$I_{IN-MAX} = \frac{15W}{0.9 \times 0.85 \times 85V} = 231mA \quad (37)$$

Maximum peak input current:

$$I_{IN-PK-MAX} = 231mA \times \sqrt{2} = 327mA \quad (38)$$

Maximum peak primary current:

$$I_{P-PK-MAX} = \frac{2 \times 327mA}{0.5} = 1.31A \quad (39)$$

9.3 Main Switching MOSFET

Maximum drain-to-source voltage:

$$V_{T-MAX} = 191V + (1.5 \times 100V) = 341V \quad (40)$$

Maximum peak MosFET current:

$$I_{T-PK-MAX} = 1.31A \quad (41)$$

Maximum RMS MosFET current:

$$I_{T-RMS-MAX} = 1.31A \times \sqrt{\frac{0.5}{3}} = 543mA \quad (42)$$

Maximum power dissipation:

$$P_{T-MAX} = 543mA^2 \times 1\Omega = 294mW \quad (43)$$

Resulting component choice:

$$\boxed{Q3 \rightarrow 400V, 2A, DPAK} \quad (44)$$

9.4 Re-circulating DIODE

Maximum reverse blocking voltage:

$$V_{RD-MAX} = 50V + \left(\frac{191V}{2}\right) = 145V \quad (45)$$

Maximum peak diode current:

$$I_{D-PK-MAX} = 1.31A \times 2 = 2.62A \quad (46)$$

Maximum average diode current:

$$I_{D-MAX} = 327\,mA \times 2 = 654\,mA \quad (47)$$

Maximum power dissipation:

$$P_{D-MAX} = 654\,mA \times 1V = 654\,mW \quad (48)$$

Resulting component choice:

$$\boxed{D10 \rightarrow 200V, 1A, SMB} \quad (49)$$

9.5 Current Sense

Sense resistor:

$$R30 \,||\, R31 = \frac{1.5V}{1.65A} = 0.9\Omega \quad (50)$$

Power dissipation:

$$P_{R30||R31} = 543\,mA^2 \times 0.9\Omega = 265\,mW \quad (51)$$

Resulting component choice:

$$\boxed{R30 \,||\, R31 \rightarrow 1\Omega, 0.25W \,||\, 10\Omega, 0.25W} \quad (52)$$

9.6 Input Capacitance

Minimum capacitance:

$$C1 = \frac{1\,mH \times 1.31A^2}{\left(120V + \frac{60V}{2}\right)^2 - \left(120V - \frac{60V}{2}\right)^2} = 119\,nF \quad (53)$$

Voltage rating:

$$V_{C1} = 191V \times 2 = 382V \quad (54)$$

Resulting component choice:

$$\boxed{C1 \rightarrow 100\,nF, 400V} \quad (55)$$

9.7 Output Capacitance

Minimum capacitance:

$$C11 = \frac{15W}{2 \times \pi \times 60\,Hz \times 50V \times 2V} = 400\,\mu F \quad (56)$$

Voltage rating:

$$V_{C11} = 50V \times 1.25 = 62.5V \quad (57)$$

Resulting component choice:

$$\boxed{C11 \rightarrow 470\,\mu F, 63V} \quad (58)$$

9.8 Transformer

Maximum acceptable reflected voltage:

$$V_{R-MAX} = \frac{2}{3} x (400V - 191V) = 140V \quad (59)$$

Primary to secondary turns ratio:

$$n < \frac{140V}{50V} = 2.8 \rightarrow 2 \quad (60)$$

Actual reflected voltage:

$$V_R = 2 x 50V = 100V \quad (61)$$

Primary to auxiliary turns ratio:

$$n_A < \frac{50V}{12.5V} = 4 \quad (62)$$

Transformer primary inductance:

$$L_{P-MIN} = \frac{(0.5)^2 x 85V}{2 x 40kHz x 327mA} = 812\mu H$$
$$L_P \rightarrow 1mH \quad (63)$$

Number of primary turns:

$$N_P = \sqrt{\frac{1mH}{160\frac{nH}{turns^2}}} = 80 turns \quad (64)$$

Number of secondary turns:

$$N_S = \frac{80 turns}{2} = 40 turns \quad (65)$$

Number of auxiliary turns:

$$N_A = \frac{40 turns}{4} = 10 turns \quad (66)$$

Maximum flux density:

$$B_{MAX} = \frac{1mH x 1.31A}{80 x 52 mm^2} = 314 mT \quad (67)$$

Resulting component choice:

$$\boxed{\begin{array}{l} N_P \rightarrow 80 turns \\ N_S \rightarrow 40 turns \\ N_A \rightarrow 10 turns \end{array}} \quad (68)$$

9.9 Transil Clamp

TVS clamp voltage:

$$V_{TVS-D1} \leq \frac{3}{2} x 100V = 150V \quad (69)$$

Resulting component choice:

$$\boxed{D1 \rightarrow 150V\ TVS} \quad (70)$$

9.10 Dynamic Hold

ISEN sense resistance:

$$R34 \,||\, R36 = \frac{200\,mV}{70\,mA} = 2.86 \tag{71}$$

HOLD resistance:

$$R12 \,||\, R14 \,||\, R15 = \frac{12V - 30\Omega \times 90\,mA}{90\,mA} = 103\Omega \tag{72}$$

Resulting component choice:

$$\boxed{\begin{array}{l} R12 \,||\, R14 \,||\, R15 = 300\Omega \,||\, 300\Omega \,||\, 300\Omega \\ R34 \,||\, R36 = 5.62\Omega \,||\, 5.62\Omega \end{array}} \tag{73}$$

9.11 Decoder Input

Resistor divider:

$$R32 = \frac{356\,mV \times 1\,M\Omega}{25V - 356\,mV} = 14.4\,k\Omega \tag{74}$$

Resulting component choice:

$$\boxed{\begin{array}{l} R26 + R29 \rightarrow 1M\Omega \\ R32 \rightarrow 14\,k\Omega \end{array}} \tag{75}$$

9.12 Output Voltage Sense

Resistance:

$$R81 = \frac{1.24V \times 105\,k\Omega}{(50V - 1.24V)} = 2.67\,k\Omega \tag{76}$$

Resulting component choice:

$$\boxed{\begin{array}{l} R81 \rightarrow 2.67\,k\Omega \\ R72 \rightarrow 105\,k\Omega \end{array}} \tag{77}$$

9.13 Loop Compensation

Converter output pole:

$$\omega_{P1} = \frac{15W}{50V^2 \times 470\,\mu F} = 12.8\,\frac{rad}{sec} \tag{78}$$

Converter DC gain:

$$G_{C0} = \frac{50V}{1.31A} = 38\Omega \tag{79}$$

LM3450 and external sensing DC gain:

$$G_{3450} = \frac{5\,k\Omega \times 1 \times 0.014 \times 0.55\,\frac{1}{V} \times 191V}{0.9\Omega \times 2\,k\Omega} = 4.09S \tag{80}$$

Secondary compensator dominant pole:

$$\omega_{P2} = \frac{1}{105\,k\Omega \times 10\,\mu F} = 0.952\,\frac{rad}{sec} \tag{81}$$

Secondary compensator zero:

$$\omega_{P2} = \frac{1}{20\,k\Omega \times 10\,\mu F} = 5\,\frac{rad}{sec} \tag{82}$$

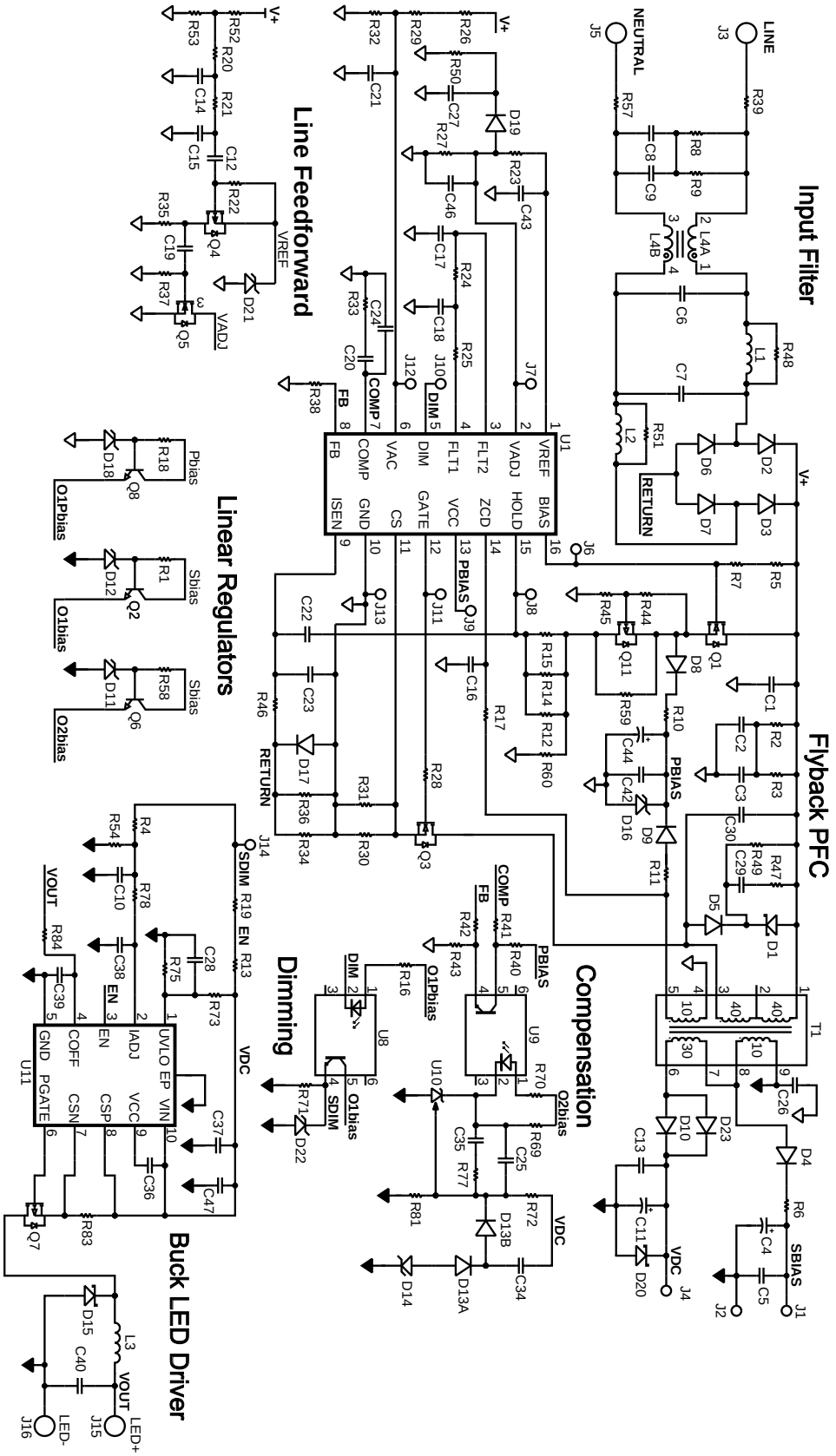
Primary roll-off pole:

$$\omega_{P3} = \frac{1}{5\,k\Omega \times 1\,\mu F} = 200\,\frac{rad}{sec} \tag{83}$$

Resulting component choice:

$$\boxed{\begin{array}{l} C35 \rightarrow 10\,\mu F \\ C24 \rightarrow 1\,\mu F \\ R77 \rightarrow 20\,k\Omega \end{array}} \tag{84}$$

10 Complete Evaluation Board Schematic



11 120V Bill of Materials

Table 1. 120V Bill of Materials

Reference Designator	Part Value	Manufacturer	Part Number
C1	CAP MPY 0.1µF 400V RAD	EPCOS	B32612A4104J008
C2, C8, C9	CAP CER 0.22µF 250V 1210	MURATA	GRM32DR72E224KW01L
C3	CAP CER 0.1µF 250V 1210	MURATA	GRM32DR72E104KW01L
C4, C44	CAP ELEC 100µF 50V RAD	NICHICON	UHE1H101MPD
C5, C23, C37, C42	CAP CER 0.10µF 50V 0603	MURATA	GRM188R71H104KA93D
C6	CAP MPY 33nF 250VAC X1 RAD	EPCOS	B32912A4733M
C7	CAP MPY 47nF 250VAC X1 RAD	EPCOS	B32912A3333M
C11	CAP ELEC 470µF 63V RAD	NICHICON	UPW1J471MHD3
C12, C14, C15	CAP CER 1µF 50V 1206	TDK	C3216X7R1H105K
C13, C34	CAP CER 1µF 100V 1206	TDK	C3216X7R2A105M
C17, C18, C24, C36	CAP CER 1µF 6.3V 0603	MURATA	GRM188R71C105KA12D
C19, C22	CAP CER 0.22µF 16V 0603	TDK	C1608X7R1C224K
C21, C43, C46	CAP CER 10nF 25V 0603	MURATA	GRM188R71E103KA01D
C26	CAP CER 4.7nF 500VAC Y1 RAD	EPCOS	VY1472M63Y5UQ63V0
C27	CAP CER 47µF 6.3V 0805	TAIYO YUDEN	JMK212BJ476MG-T
C35	CAP CER 10µF 16V 1206	MURATA	GRM31CR71C106KAC7L
C38	CAP CER 2.2µF 6.3V 0603	TDK	C1608X5R0J225M
C39	CAP CER 470pF 100V 0603	TDK	C1608C0G2A471J
C47	CAP CER 4.7µF 100V 2220	TDK	C5750X7R2A475K
D1	DIODE TVS 150V 600W UNI SMB	LITTLEFUSE	SMBJ150A
D2, D3, D6, D7	DIODE GEN PURPOSE 1000V 1A SMA	COMCHIP	CGRA4007-G
D4, D9	DIODE ULTRAFAST 100V 0.2A SOT-23	FAIRCHILD	MMBD914
D5	DIODE ULTRAFAST 600V 1A SMA	FAIRCHILD	ES1J
D8, D10	DIODE ULTRAFAST 200V 1A SMA	FAIRCHILD	ES1D
D11, D12, D18	DIODE ZENER 10V 500mW SOD-123	FAIRCHILD	MMSZ5240B
D13	DIODE ULTRAFAST 70V 0.2A SOT-23	FAIRCHILD	BAV99
D14	DIODE ZENER 3.3V 500mW SOD-123	ON-SEMI	MMSZ3V3T1G
D15	DIODE SCHOTTKY 60V 2A SMB	ON-SEMI	SS26T3G
D16	DIODE ZENER 24V 3W SMA	MICRO-SEMI	SMAJ5934B-TP
D17	DIODE SCHOTTKY 20V 3A SMA	FAIRCHILD	ES2AA-13-F
D19	DIODE SCHOTTKY 20V 0.5A SOT-23	NXP SEMI	PMEG2005ET,215
D21	DIODE ZENER 3V 500MW SOD-123	ON-SEMI	MMSZ4683T1G
D22	DIODE ZENER 1.8V 500MW SOD-123	ON-SEMI	MMSZ4678T1G
J3, J5, J15, J16	TERMINAL TURRET DOUBLE TH	KEYSTONE	1502-2
L1, L2	IND SHIELD 1mH 0.46A SMT	COILCRAFT	MSS1038-105KL
L3	IND SHIELD 470µH 1.06A SMT	COILCRAFT	MSS1260-474KLB
L4	IND LINE FILTER 6mH 0.3A 11M	PANASONIC	ELF-11M030E
Q1	MOSFET N-CH 800V 3A DPAK	ST MICRO	STD3NK80ZT4
Q2, Q6, Q8	TRANS NPN 40V 0.6A SOT-23	FAIRCHILD	MMBT4401
Q3	MOSFET N-CH 600V 4.4A DPAK	INFINEON	IPD60R950C6
Q4	MOSFET P-CH 20V 3.7A SOT-23	VISHAY	SI2323DS
Q5	MOSFET N-CH 60V 260MA SOT-23	ON-SEMI	2N7002ET1G
Q7	MOSFET P-CH 70V 5.7A DPAK	ZETEX	ZXMP7A17K
R1, R18, R58	RES 10kΩ 1% 0.1W 0603	VISHAY	CRCW060310K0FKEA
R2, R3	RES 820Ω 5% 1W 2512	VISHAY	CRCW2512820RJNEG
R5, R7	RES 200kΩ 1% 0.25W 1206	VISHAY	CRCW1206200KFKEA

Table 1. 120V Bill of Materials (continued)

R6	RES 0Ω 5% 0.25W 1206	VISHAY	CRCW12060000Z0EA
R8, R9	RES 680Ω 5% 1W 2512	VISHAY	CRCW2512680RJNEG
R10	RES 20Ω 1% 0.25W 1206	VISHAY	CRCW120620R0FKEA
R11, R30	RES 10Ω 1% 0.25W 1206	VISHAY	CRCW120610R0FKEA
R12, R14, R15	RES 301Ω 1% 0.25W 1206	VISHAY	CRCW1206301RFKEA
R16	RES 6.04kΩ 1% 0.125W 0805	VISHAY	CRCW08056K04FKEA
R17, R27, R50	RES 100kΩ 1% 0.1W 0603	VISHAY	CRCW0603100KFKEA
R19, R41, R43, R46, R59, R73	RES 0Ω 5% 0.1W 0603	VISHAY	CRCW06030000Z0EA
R20	RES 5.36kΩ 1% 0.25W 1206	VISHAY	CRCW12065K36FKEA
R21	RES 5.36kΩ 1% 0.1W 0603	VISHAY	CRCW06035K36FKEA
R22, R35, R37	RES 30.1kΩ 1% 0.1W 0603	VISHAY	CRCW060330K1FKEA
R23	RES 3.01kΩ 1% 0.1W 0603	VISHAY	CRCW06033K01FKEA
R24, R25	RES 75.0kΩ 1% 0.1W 0603	VISHAY	CRCW060375K0FKEA
R26, R29, R53	RES 499kΩ 1% 0.25% 1206	VISHAY	CRCW1206499KFKEA
R28	RES 10Ω 5% 0.125W 0805	VISHAY	CRCW080510R0JNEA
R31	RES 1.00Ω 1% 0.33W 1210	VISHAY	CRCW12101R00FNEA
R32	RES 14.0kΩ 1% 0.1W 0603	VISHAY	CRCW060314K0FKEA
R34, R36	RES 5.62Ω 1% 0.25W 1206	VISHAY	CRCW12065R62FNEA
R38	RES 5.11kΩ 1% 0.1W 0603	VISHAY	CRCW06035K11FKEA
R39, R57	RES 10Ω 10% 2W FILM	WELWYN	EMC2-10R0
R48, R51	RES 20.0kΩ 1% 0.25W 1206	VISHAY	CRCW120620K0FKEA
R52	RES 1.00MΩ 1% 0.25W 1206	VISHAY	CRCW12061M00FKEA
R60	RES 2.49kΩ 1% 0.125W 0805	VISHAY	CRCW08052K49FKEA
R69, R77	RES 20.0kΩ 1% 0.1W 0603	VISHAY	CRCW060320K0FKEA
R70	RES 2.00kΩ 1% 0.125W 0805	VISHAY	CRCW08052K00FKEA
R71	RES 10.0kΩ 1% 0.125W 0805	VISHAY	CRCW080510K0FKEA
R72	RES 105kΩ 1% 0.125W 0805	VISHAY	CRCW0805105KFKEA
R81	RES 2.67kΩ 1% 0.1W 0603	VISHAY	CRCW06032K67FKEA
R83	RES .62Ω 1% 0.5 2010 SMD	ROHM	MCR50JZHFLR620
R84	RES 80.6kΩ 1% 0.1W 0603	VISHAY	CRCW060380K6FKEA
T1	XFORMER 120V 15W OUTPUT 50V	WURTH	750813550
U1	IC PFC CONT 16-TSSOP	TI	LM3450
U8, U9	OPTO-ISOLATOR SMD	LITE ON	CNY17F-3S
U10	IC SHUNT REG SOT-23	TI	LMV431A
U11	IC LED DRIVR 10-MSOP-PowerPAD™	TI	LM3409HV
Any not specified	Do not populate		

12 230V Bill of Materials

Table 2. 230V Bill of Materials

Reference Designator	Part Value	Manufacturer	Part Number
C1	CAP MPY 0.1µF 400V RAD	EPCOS	B32612A4104J008
C2, C3, C8, C9	CAP CER 68nF 250V 1210	MURATA	GRM32QR72E683KW01L
C4, C44	CAP ELEC 100µF 50V RAD	NICHICON	UHE1H101MPD
C5, C23, C37, C42	CAP CER 0.10µF 50V 0603	MURATA	GRM188R71H104KA93D
C6	CAP MPY 33nF 250VAC X1 RAD	EPCOS	B32912A4733M
C7	CAP MPY 47nF 250VAC X1 RAD	EPCOS	B32912A3333M
C11	CAP ELEC 470µF 63V RAD	NICHICON	UPW1J471MHD3
C12, C14, C15	CAP CER 1µF 50V 1206	TDK	C3216X7R1H105K
C13, C34	CAP CER 1µF 100V 1206	TDK	C3216X7R2A105M
C17, C18, C24, C36	CAP CER 1µF 6.3V 0603	MURATA	GRM188R71C105KA12D
C19, C22	CAP CER 0.22µF 16V 0603	TDK	C1608X7R1C224K
C21, C43, C46	CAP CER 10nF 25V 0603	MURATA	GRM188R71E103KA01D
C26	CAP CER 4.7nF 500VAC Y1 RAD	EPCOS	VY1472M63Y5UQ63V0
C27	CAP CER 47µF 6.3V 0805	TAIYO YUDEN	JMK212BJ476MG-T
C35	CAP CER 10µF 16V 1206	MURATA	GRM31CR71C106KAC7L
C38	CAP CER 2.2µF 6.3V 0603	TDK	C1608X5R0J225M
C39	CAP CER 470pF 100V 0603	TDK	C1608C0G2A471J
C47	CAP CER 4.7µF 100V 2220	TDK	C5750X7R2A475K
D1	DIODE TVS 220V 600W UNI SMB	LITTLEFUSE	SMBJ220A
D2, D3, D6, D7	DIODE GEN PURPOSE 1000V 1A SMA	COMCHIP	CGRA4007-G
D4, D9	DIODE ULTRAFAST 100V 0.2A SOT-23	FAIRCHILD	MMBD914
D5	DIODE ULTRAFAST 600V 1A SMA	FAIRCHILD	ES1J
D8	DIODE ULTRAFAST 200V 1A SMA	FAIRCHILD	ES1D
D10	DIODE ULTRAFAST 300V 1A SMA	FAIRCHILD	ES1F
D11, D12, D18	DIODE ZENER 10V 500mW SOD-123	FAIRCHILD	MMSZ5240B
D13	DIODE ULTRAFAST 70V 0.2A SOT-23	FAIRCHILD	BAV99
D14	DIODE ZENER 3.3V 500mW SOD-123	ON-SEMI	MMSZ3V3T1G
D15	DIODE SCHOTTKY 60V 2A SMB	ON-SEMI	SS26T3G
D16	DIODE ZENER 24V 3W SMA	MICRO-SEMI	SMAJ5934B-TP
D17	DIODE SCHOTTKY 20V 3A SMA	FAIRCHILD	ES2AA-13-F
D19	DIODE SCHOTTKY 20V 0.5A SOT-23	NXP SEMI	PMEG2005ET,215
D21	DIODE ZENER 3V 500MW SOD-123	ON-SEMI	MMSZ4683T1G
D22	DIODE ZENER 1.8V 500MW SOD-123	ON-SEMI	MMSZ4678T1G
J3, J5, J15, J16	TERMINAL TURRET DOUBLE TH	KEYSTONE	1502-2
L1, L2	IND SHIELD 1mH 0.46A SMT	COILCRAFT	MSS1038-105KL
L3	IND SHIELD 470µH 1.06A SMT	COILCRAFT	MSS1260-474KLB
L4	IND LINE FILTER 6mH 0.3A 11M	PANASONIC	ELF-11M030E
Q1, Q3	MOSFET N-CH 800V 3A DPAK	ST MICRO	STD3NK80ZT4
Q2, Q6, Q8	TRANS NPN 40V 0.6A SOT-23	FAIRCHILD	MMBT4401
Q4	MOSFET P-CH 20V 3.7A SOT-23	VISHAY	SI2323DS
Q5	MOSFET N-CH 60V 260MA SOT-23	ON-SEMI	2N7002ET1G
Q7	MOSFET P-CH 70V 5.7A DPAK	ZETEX	ZXMP7A17K
R1, R18, R58, R77	RES 10kΩ 1% 0.1W 0603	VISHAY	CRCW060310K0FKEA
R2, R3	RES 3.3kΩ 5% 1W 2512	VISHAY	CRCW25123K30JNEG
R5, R7	RES 475kΩ 1% 0.25W 1206	VISHAY	CRCW1206475KFKEA
R6	RES 0Ω 5% 0.25W 1206	VISHAY	CRCW12060000Z0EA

Table 2. 230V Bill of Materials (continued)

R8, R9	RES 1kΩ 5% 1W 2512	VISHAY	CRCW25121K00JNEG
R10	RES 20Ω 1% 0.25W 1206	VISHAY	CRCW120620R0FKEA
R11, R30	RES 10Ω 1% 0.25W 1206	VISHAY	CRCW120610R0FKEA
R12, R14, R15	RES 301Ω 1% 0.25W 1206	VISHAY	CRCW1206301RFKEA
R16	RES 6.04kΩ 1% 0.125W 0805	VISHAY	CRCW08056K04FKEA
R17, R27, R50	RES 100kΩ 1% 0.1W 0603	VISHAY	CRCW0603100KFKEA
R19, R41, R43, R46, R59, R73	RES 0Ω 5% 0.1W 0603	VISHAY	CRCW06030000Z0EA
R20	RES 5.36kΩ 1% 0.25W 1206	VISHAY	CRCW12065K36FKEA
R21	RES 5.36kΩ 1% 0.1W 0603	VISHAY	CRCW06035K36FKEA
R22, R35, R37	RES 30.1kΩ 1% 0.1W 0603	VISHAY	CRCW060330K1FKEA
R23, R32	RES 15kΩ 1% 0.1W 0603	VISHAY	CRCW060315K0FKEA
R24, R25	RES 75.0kΩ 1% 0.1W 0603	VISHAY	CRCW060375K0FKEA
R26, R29, R52	RES 1.00MΩ 1% 0.25W 1206	VISHAY	CRCW12061M00FKEA
R28	RES 10Ω 5% 0.125W 0805	VISHAY	CRCW080510R0JNEA
R31	RES 1.00Ω 1% 0.33W 1210	VISHAY	CRCW12101R00FNEA
R34, R36	RES 5.62Ω 1% 0.25W 1206	VISHAY	CRCW12065R62FNEA
R38	RES 5.11kΩ 1% 0.1W 0603	VISHAY	CRCW06035K11FKEA
R39, R57	RES 27Ω 10% 2W FILM	WELWYN	EMC2-27R0
R48, R51	RES 20.0kΩ 1% 0.25W 1206	VISHAY	CRCW120620K0FKEA
R53	RES 249kΩ 1% 0.25W 1206	VISHAY	CRCW1206249KFKEA
R60	RES 4.99kΩ 1% 0.125W 0805	VISHAY	CRCW08054K99FKEA
R69	RES 20.0kΩ 1% 0.1W 0603	VISHAY	CRCW060320K0FKEA
R70	RES 2.00kΩ 1% 0.125W 0805	VISHAY	CRCW08052K00FKEA
R71	RES 10.0kΩ 1% 0.125W 0805	VISHAY	CRCW080510K0FKEA
R72	RES 105kΩ 1% 0.125W 0805	VISHAY	CRCW0805105KFKEA
R81	RES 2.67kΩ 1% 0.1W 0603	VISHAY	CRCW06032K67FKEA
R83	RES .62Ω 1% 0.5 2010 SMD	ROHM	MCR50JZHFLR620
R84	RES 80.6kΩ 1% 0.1W 0603	VISHAY	CRCW060380K6FKEA
T1	XFORMER 120V 15W OUTPUT 50V	WURTH	750813550
U1	IC PFC CONT 16-TSSOP	TI	LM3450
U8, U9	OPTO-ISOLATOR SMD	LITE ON	CNY17F-3S
U10	IC SHUNT REG SOT-23	TI	LMV431A
U11	IC LED DRIVR 10-MSOP-PowerPAD	TI	LM3409HV
Any not specified	Do not populate		

13 PCB Layout

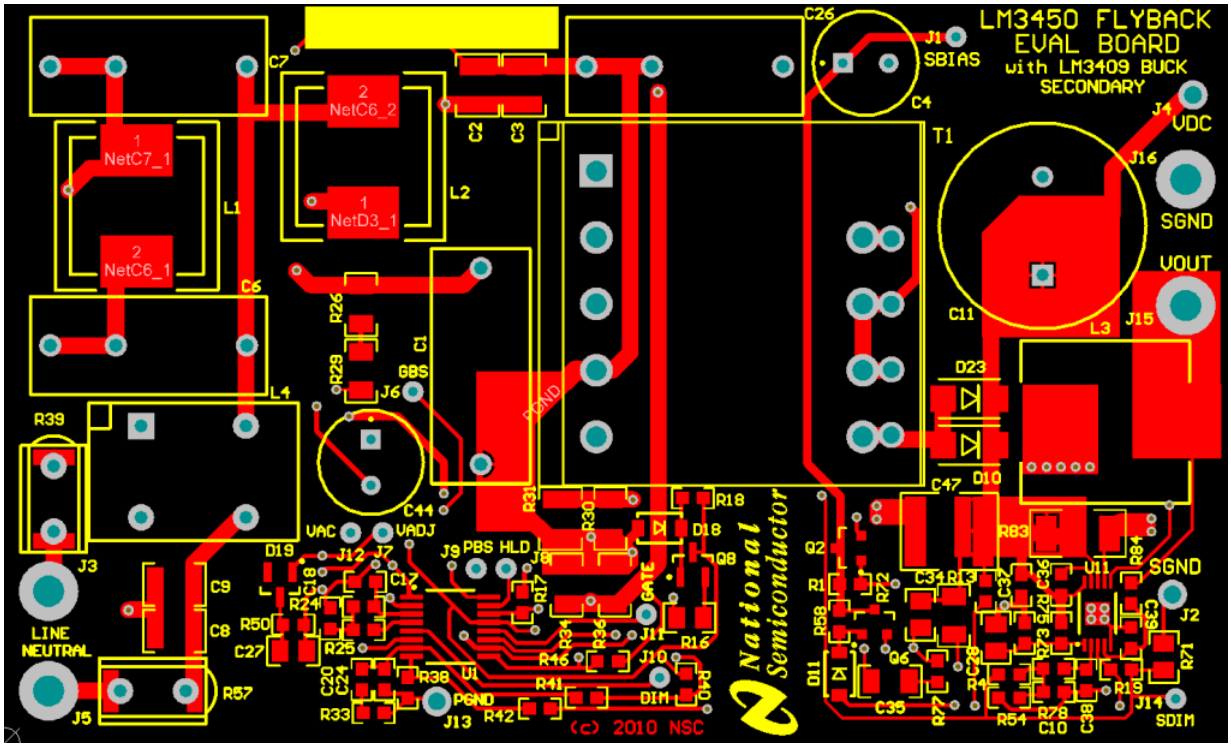


Figure 23. Top Copper and Silkscreen

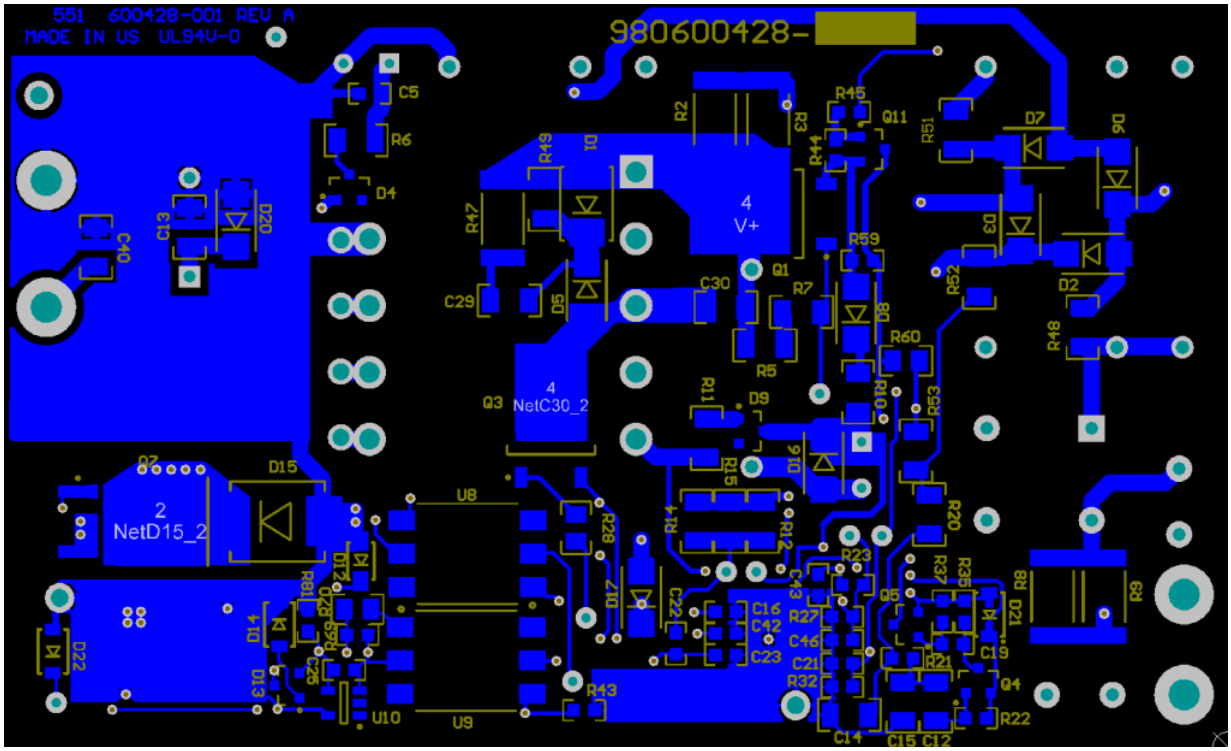


Figure 24. Bottom Copper and Silkscreen

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