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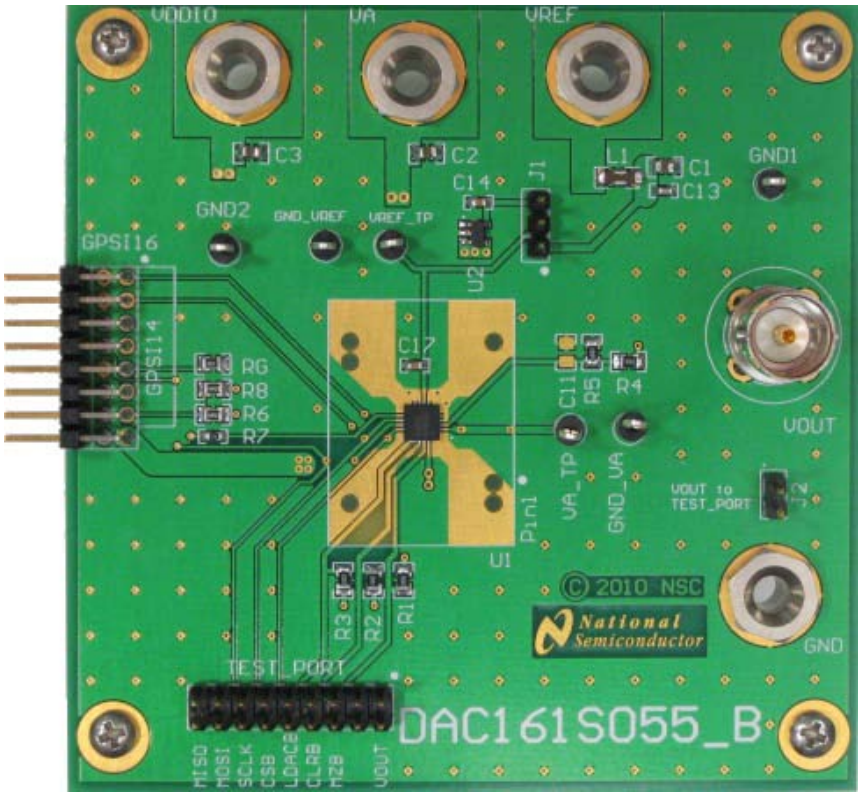
Evaluation Board User's Guide

DAC161S055 16-Bit, Low Glitch, Buffered Voltage-Output Digital to Analog Converter



1. Introduction

The DAC161S055 Evaluation Board Design Kit (consisting of the DAC161S055 Evaluation Board, this User's Guide and the optional SPUSI2 board from National Semiconductor) is intended to ease evaluation and design-in of the National Semiconductor DAC161S055 16-bit Digital to Analog Converter.

The evaluation board can be used in either the 'Stand-Alone mode' or the 'Computer mode'. In the 'Stand-Alone mode', the user can interface to the part using the on board TEST_PORT with external pattern generators and other suitable test equipment or with a ribbon cable attached to their microprocessor's evaluation board.

In the 'Computer mode', data can be sent to the DAC161S055 using the SPUSI2 board and the TinyI2CSPI software. The SPUSI2 board can be purchased, and the TinyI2CSPI software downloaded for free, at http://www.national.com/analog/webench/sensors/spusi2 . The TinyI2CSPI software operates under Microsoft Windows and allows the user to send and receive individual SPI transactions. The TinyI2CSPI software therefore will be useful for applications where you want to set an output value and observe that value.

2. Board Assembly

The DAC161S055 evaluation board comes fully assembled and ready for use. Refer to the Bill of Materials for a description of components, to Figure 1 for major component placement, and to the schematic at the end of this document.

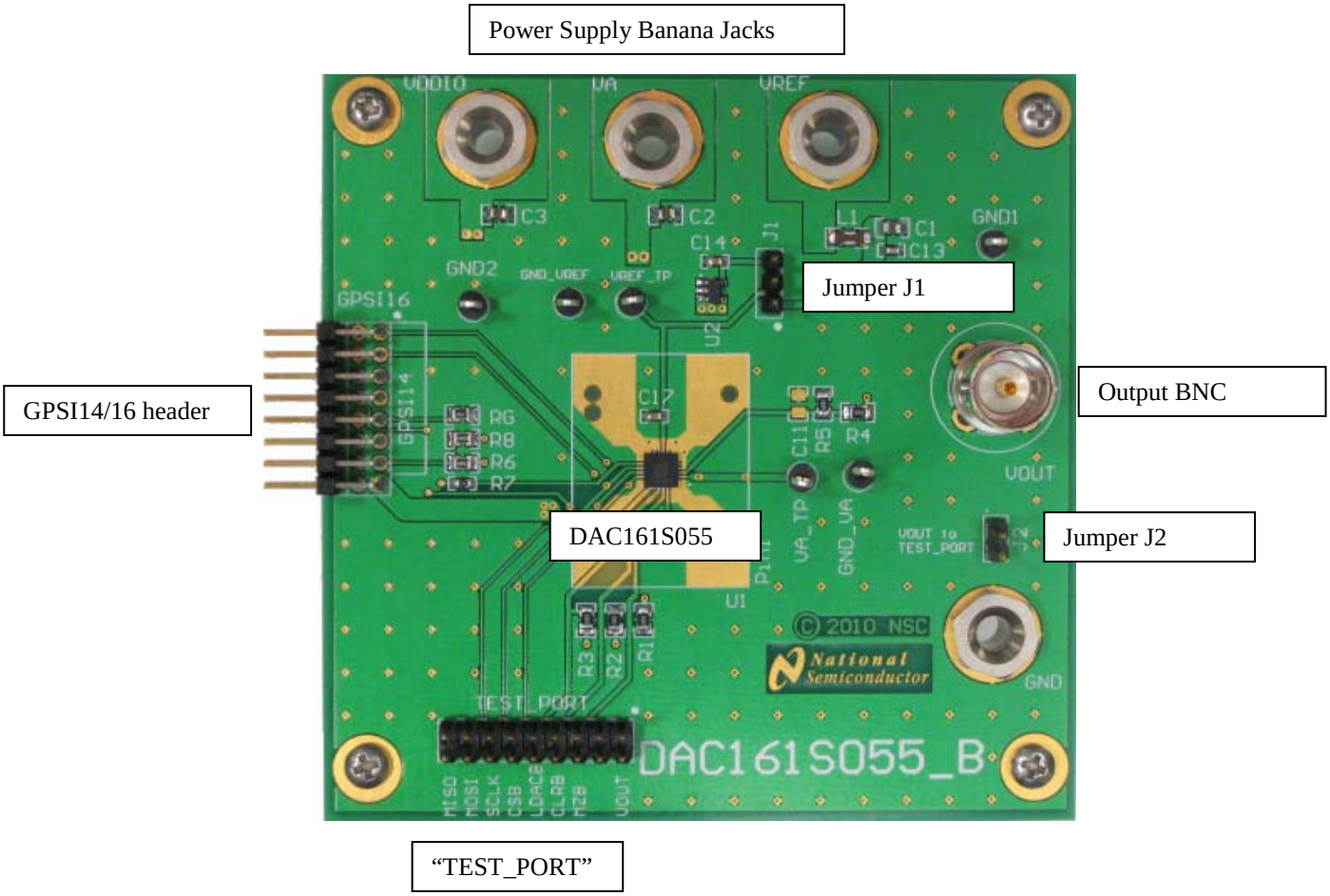


Figure 1: Location of major components

VREF_TP, GND_VREF	VREF test point and ground. Located above the DAC161S055
VA_TP, GND_VA	VA external supply and ground. Located between the part and the Vout BNC

Table 1: Test Points on the DAC161S055 Evaluation Board

GPSI16/GPSI14	16 pin dual row right angle male header. Connect 14 pin to SPUSI board. The 16 pin are for forward compatibility.
TEST_PORT	18 pin dual row male header. Allows access to SPI signals, Vout, and on board control signals. Allows for grounding of control signals (LDACB, MZB, CLRB) using a jumper.

Table 2: Connectors on the DAC161S055 Evaluation Board

J1	Selects reference source for VREF – either external or on board LM4120-4.1.
J2	Connects Vout to the TEST_PORT.

Table 3: Jumpers

3. Quick Start

The fastest way to start using the DAC161S055 evaluation board is to use it in Computer Mode with the SPUSI2 board and the TinyI2CSPI software.

3.1 Computer Mode

You will need a power supply for VA and a power supply for VDDIO. If you choose to use an external reference, you will also need a power supply VREF.

- For using the external VREF from the banana jack, connect pin 1 to pin 2 on jumper J1.
- To use the onboard LM4120-4.1 regulator, connect pin 3 to pin 2 on jumper J1
- Determine if you want to start up at zero or mid scale for the DAC output. If zero, connect pins 5 (gnd) and 6 (MZB) on the TEST_PORT header.
- Determine if you would like to have the DAC update every time you write data to it (instead of having to write data and then write an update command). If so, short pins 9 and 10 (gnd and LDACB) on the TEST_PORT header.
- Connect the SPUSI2 board to the DAC161S055 evaluation board. Ensure that you line up the SPUSI2 board with the GPSI14 pins as shown on the board (see Figure 2). Note that one set of pins will not match the header.
- Connect the power (VA and VDDIO, optionally VREF) to the board and turn on the supplies.
- Connect the SPUSI2 board to your computer via the USB cable.

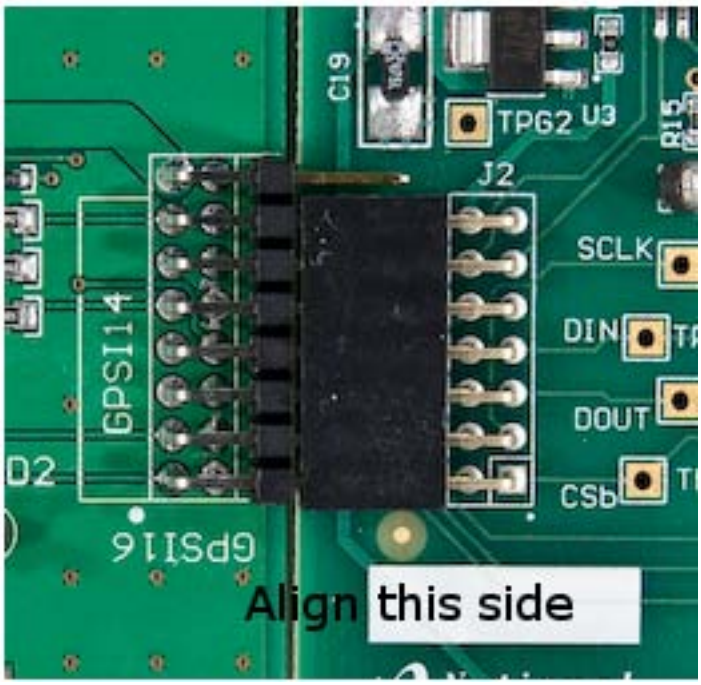


Figure 2: DAC161S055 Eval board connected to SPUSI board.

- Start the TinyI2CSPI software on your computer.
- Once the program has started, select "Add SPI" to get an SPI interface window.
- The settings needed to communicate with the DAC161S055 are
    - CS=1
    - CKPOL=0
    - CKPHA=0
    - Bits=24
- Type the command (in HEX) that you wish to send to the DAC161S055 into the MOSI field. See Figure 3 for some example commands. Pressing "Execute" will send the command to the DAC.
- The MISO field will update once "Execute" is pressed. It will be '00 0000' for the first execution. It will be the last command for each subsequent execution as long as a clear command has not been sent.
- The DAC output will be available at the Vout BNC after executing a command that updates the output.
- Go to http://www.national.com/analog/webench/sensors/spusi2#tinyi2cspi to download the TinyI2CSPI personality file for this board.

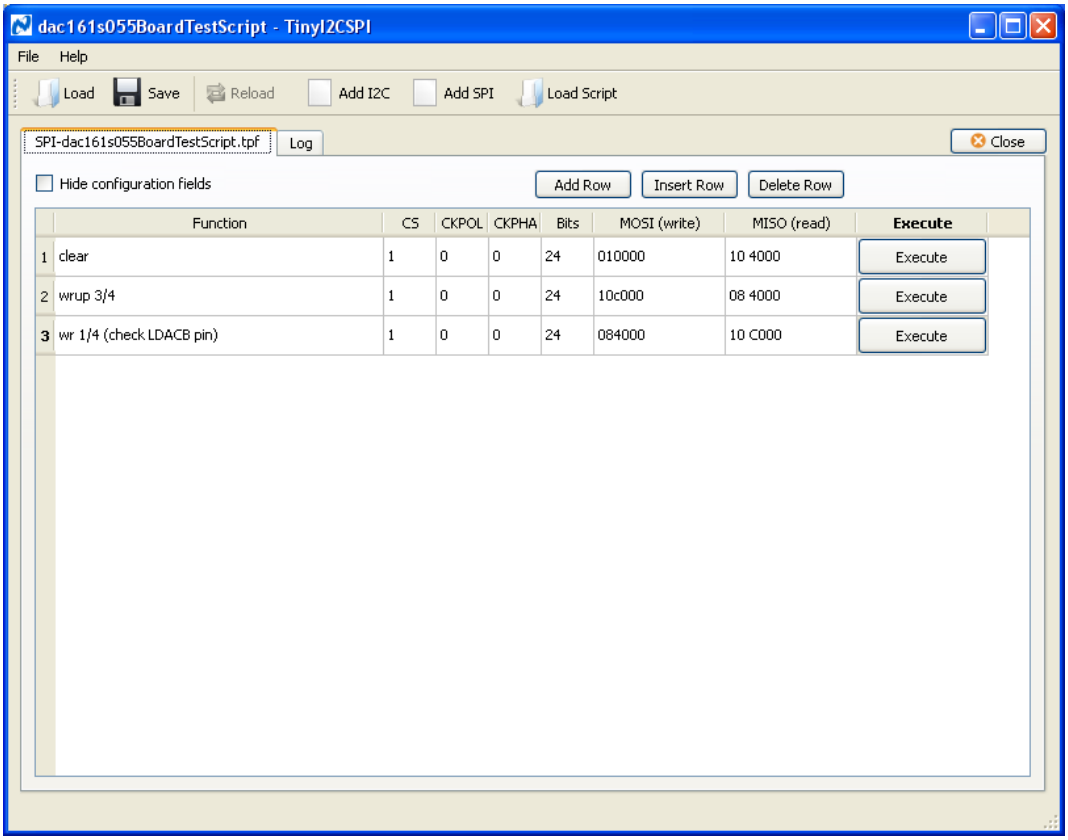


Figure 3: Example commands in TinyI2CSPI interface

4. Functional Description

4.1 DAC Reference Circuitry

This evaluation board includes two options to source the voltage reference, VREF. The options are selecting the fixed, on board +4.096V voltage reference (LM4120-4.1) to source VREF or using the external banana jack to source VREF. To select the +4.1V reference, short pins 2 & 3 of J1. To select the external reference, short pins 1 & 2 of J1. J1 can be driven by a power supply set between +2.7 V and +5.25 V.

4.2 SPI Interface

The DAC161S055 requires three SPI input pins. It has one output pin. The input pins are Serial Clock (SCLK), Chip Select Bar (CSB), and data in or Master Out Slave In (MOSI). The user must provide input signals for SCLK, CSB and MOSI. The user can optionally use the data out or Master In Slave Out (MISO) pin to use the DAC161S055 in a Daisy Chain configuration as described in the data sheet.

4.2.1 Serial Clock (SCLK, CSB, MISO, MOSI)

These signals are provided by the SPUSI2 board in Computer Mode. In Stand Alone Mode, these signals must be provided by the user either on the TEST_PORT or the GPSI 14/16 header. The signal levels are TTL and CMOS compatible. The voltage expected is set by the value of VDDIO that is applied to the board.

4.3 Other I/O

The DAC161S055 requires three other digital I/O pins: LDACB, CLRB and MZB.

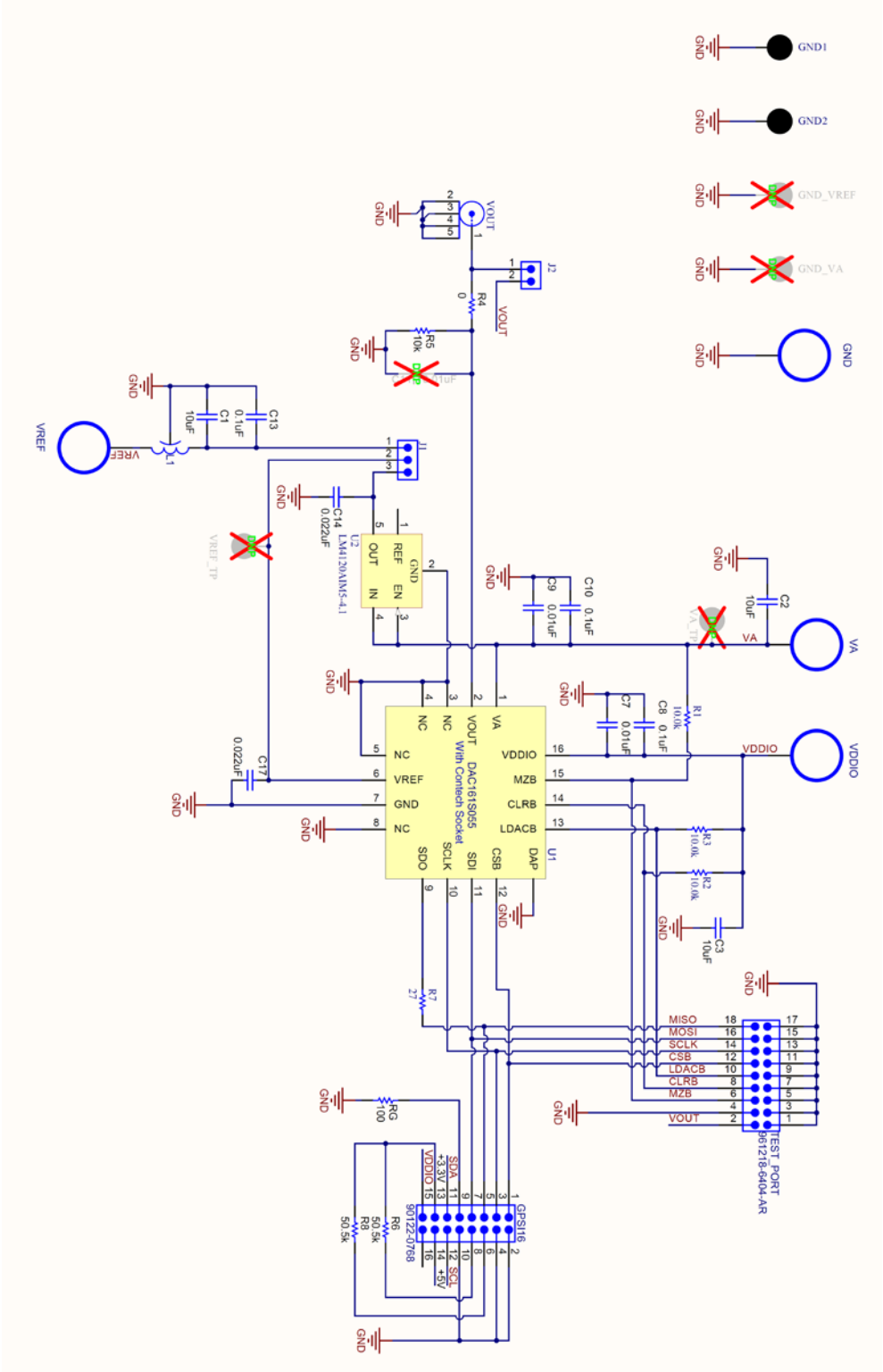
4.3.1 Load DAC (LDACB) and Clear (CLRB)

These two signals must be provided by the user. In computer mode, you can set the levels by either leaving the pin on the TEST_PORT unconnected, in which case it floats high, or by shorting the pin to the ground pin on the header using a jumper. The signal level for CSB is TTL and CMOS compatible. The voltage expected is set by the value of VDDIO that is applied to the board.

4.3.2 Mid Scale or Zero Output (MZB)

The MZB pin must be provide by the user. In computer mode, the level can be set by leaving the pin floating (for a high) or shorting it to ground on the TEST_PORT header using a jumper. The signal level for MISO is TTL and CMOS compatible. Unlike all the other pins, the voltage expected is set by the value of VA that is applied to the board so that the output is set when the VA supply comes up.

5. Hardware Schematic


GND1
GND2
GND_VREF
GND_VA
GND
VOUT
J2
R4
0
R5
10k
C1
10uF
C13
0.1uF
VREF
J1
C14
0.022uF
U2
LM4120AIM5-4.1
C9
0.01uF
C10
0.1uF
C2
10uF
VA
C7
0.01uF
C8
0.1uF
R1
10.0k
VDDIO
C17
0.022uF
U1
DAC161S055
With Comtech Socket
NC
VOUT
VA
VREF
GND
VDDIO
MZB
CLRB
LDACB
SCLK
SDI
CSB
SDO
DAP
R3
10.0k
R2
10.0k
C3
10uF
R7
27
MISO
MOSI
SCLK
CSB
LDACB
CLRB
MZB
VOUT
TEST_PORT
96118-6404-AR
RG
100
R6
50.5k
R8
50.5k
90122-0768
GPSI16
SDA
+3.3V
VDDIO
SCL
+5V

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6. DAC161S055 Evaluation Board Bill of Materials

Item	Designator	Value	Description	Manufacturer	PartNumber	Quantity
1	AA1		Printed Circuit Board	TBD		1
2	C1, C2, C3	10uF	Ceramic, X5R, 10V, 10%	Kemet	C0805C106K8PACTU	3
3	C7, C9	0.01uF	Ceramic, X7R, 50V, 10%	Kemet	C0805C103K5RACTU	2
4	C8, C10, C13	0.1uF	Ceramic, X7R, 16V, 10%	Kemet	C0603C104K4RACTU	3
5	C14, C17	0.022uF	Ceramic, X7R, 16V, 10%	Kemet	C0603C223K4RACTU	2
6	GND, VA, VDDIO, VREF		Uninsulated Standard .175 Female Banana Jack Panel Mount	Emerson Network Power Connectivity Solutions	108-0740-001	4
7	GND1, GND2	Black	Test Point, TH, Multipurpose, Black	Keystone Electronics	5011	2
8	GPSI16		2x8 CONN HEADER 16POS .100" R/A GOLD	Molex	90122-0768	1
9	J1		CONN 1X3 HEADER 100mil pitch	3M	961103-6404-AR	1
10	J2		CONN 1X2 HEADER 100mil pitch	3M	961102-6404-AR	1
11	L1		FILTER LC HIGH FREQ .2UF 1806	Murata	NFM41PC204F1H3L	1
12	R1, R2, R3	10.0k	1%, 0.125W	Vishay-Dale	CRCW080510K0FKEA	3
13	R4	0	RES, 0 ohm, 5%, 0.125W, 0805	Vishay-Dale	CRCW08050000Z0EA	1
14	R5	10k	RES, 10k ohm, 5%, 0.125W, 0805	Vishay-Dale	CRCW080510K0JNEA	1
15	R6, R8	49.9k	RES, 49.9k ohm, 1%, 0.125W, 0805	Panasonic	ERJ-6ENF4992V	2
16	R7	27	5%, 0.1W	Vishay-Dale	CRCW060327R0JNEA	1
17	RG	100	RES, 100 ohm, 5%, 0.125W, 0805	Panasonic	ERJ-6GEYJ101V	1
18	TEST_PORT		2x9 CONN HEADER 18POS .100"	3M	961218-6404-AR	1
19	U1		Precision 16-bit, Low Glitch, Buffered Voltage-Output DAC	National Semiconductor	DAC161S055	1
20	U2		Precision Micropower Low Dropout Voltage Reference	National Semiconductor	LM4120AIM5-4.1	1
21	VOUT		Connector, TH, 75 Ohm BNC	Amphenol Connex	31-5329-72RFX	1

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