Current Mode PWM Controller for Forward and Flyback Applications

NCP1252

The NCP1252 controller offers everything needed to build cost−effective and reliable ac−dc switching supplies dedicated to ATX power supplies. Thanks to the use of an internally fixed timer, NCP1252 detects an output overload without relying on the auxiliary Vcc. A Brown−Out input offers protection against low input voltages and improves the converter safety. Finally a SOIC−8 package saves PCB space and represents a solution of choice in cost sensitive project.

Features

- Peak Current Mode Control
- Adjustable Switching Frequency up to 500 kHz
- Jittering Frequency ±5% of the Switching Frequency
- Latched Primary Over Current Protection with 10 ms Fixed Delay
- Delay Extended to 150 ms in E Version
- Delayed Operation Upon Start−up via an Internal Fixed Timer (A, B and C versions only)
- Adjustable Soft−start Timer
- Auto−recovery Brown−Out Detection
- UC384X−like UVLO Thresholds
- Vcc Range from 9 V to 28 V with Auto−recovery UVLO
- Internal 160 ns Leading Edge Blanking
- Adjustable Internal Ramp Compensation
- +500 mA / –800 mA Source / Sink Capability
- Maximum 50% Duty Cycle: A Version
- Maximum 80% Duty Cycle: B Version
- Maximum 65% Duty Cycle: C Version
- Maximum 47.5% Duty Cycle: D & E Versions
- Ready for Updated No Load Regulation Specifications
- SOIC−8 and PDIP−8 Packages
- These are Pb−Free Devices

Typical Applications

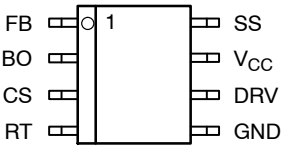
- Power Supplies for PC Silver Boxes, Games Adapter...
- Flyback and Forward Converter

OFFLINE CONTROLLER

SOIC−8
CASE 751
SUFFIX D

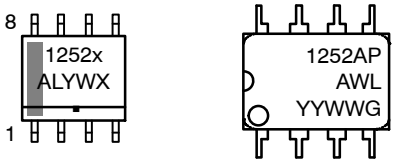
PDIP−8
CASE 626
SUFFIX P

PIN CONNECTIONS



(Top View)

MARKING DIAGRAMS



x	= A, B, C, D or E
A	= Assembly Location
L, WL	= Wafer Lot
Y, YY	= Year
W, WW	= Work Week
▪ or G	= Pb−Free Package

ORDERING INFORMATION

See detailed ordering and shipping information on page 18 of this data sheet.

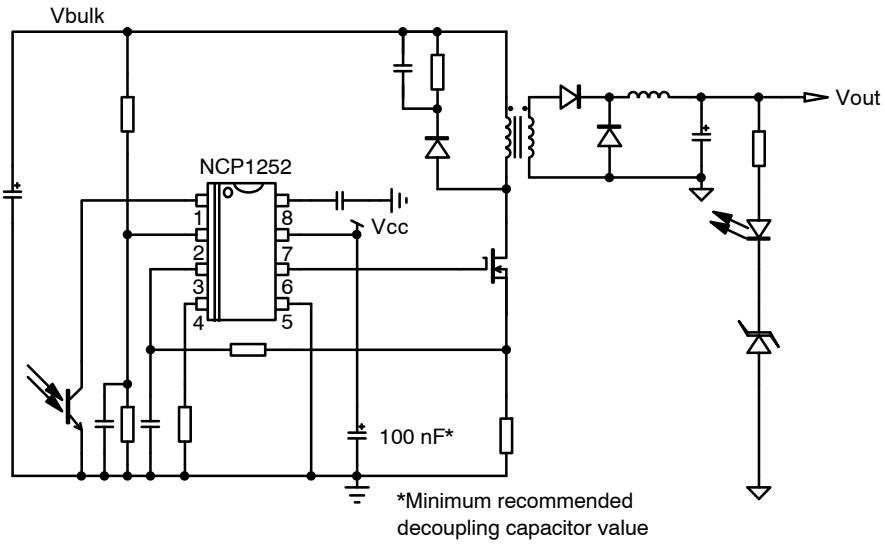


Figure 1. Typical Application

Table 1. PIN FUNCTIONS

Pin No.	Pin Name	Function	Pin Description
1	FB	Feedback	This pin directly connects to an optocoupler collector.
2	BO	Brown−out input	This pin monitors the input voltage image to offer a Brown−out protection.
3	CS	Current sense	Monitors the primary current and allows the selection of the ramp compensation amplitude.
4	R_T	Timing element	A resistor connected to ground fixes the switching frequency.
5	GND	−	The controller ground pin.
6	Drv	Driver	This pin connects to the MOSFET gate
7	V_{CC}	V_{CC}	This pin accepts voltage range from 8 V up to 28 V
8	SSTART	Soft−start	A capacitor connected to ground selects the soft−start duration. The soft start is grounded during the delay timer

Table 2. MAXIMUM RATINGS TABLE (Notes 1 and 2)

Symbol	Rating	Value	Unit
V_{CC}	Power Supply voltage, Vcc pin, transient voltage: 10 ms with I_{Vcc} < 20 mA	30	V
V_{CC}	Power Supply voltage, Vcc pin, continuous voltage	28	V
I_{Vcc}	Maximum current injected into pin 7	20	mA
V_{DRV}	Maximum voltage on DRV pin	−0.3 to V_{CC}	V
	Maximum voltage on low power pins (except pin 6, 7)	−0.3 to 10	V
$R_{\theta JA\ -\ PDIP8}$	Thermal Resistance Junction−to−Air − PDIP8	131	°C/W
$R_{\theta JA\ -\ SOIC8}$	Thermal Resistance Junction−to−Air − SOIC8	169	°C/W
$T_{J(MAX)}$	Maximum Junction Temperature	150	°C
T_{STG}	Storage Temperature Range	−60 to +150	°C
ESD_{HBM}	ESD Capability, HBM model	1.8	kV
ESD_{MM}	ESD Capability, Machine Model	200	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. This device series contains ESD protection and exceeds the following tests: Human Body Model 1800 V per JEDEC Standard JESD22−A114E. Machine Model Method 200 V per JEDEC Standard JESD22−A115A.
2. This device contains latch−up protection and exceeds 100 mA per JEDEC Standard JESD78.

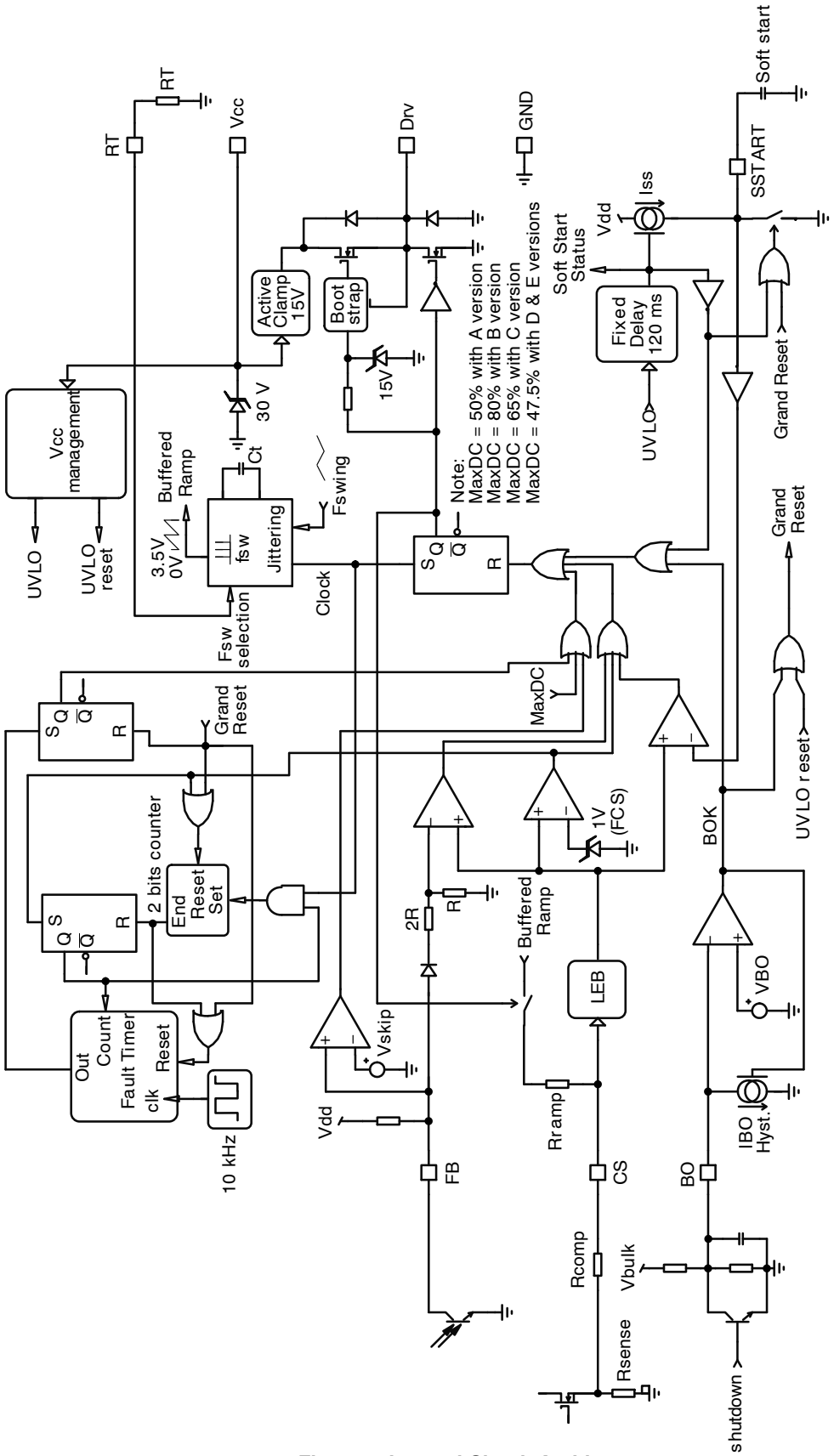


Figure 2. Internal Circuit Architecture

Table 3. ELECTRICAL CHARATERISTICS

(V_{CC} = 15 V, R_T = 43 kΩ, C_{DRV} = 1 nF. For typical values T_J = 25°C, for min/max values T_J = −25°C to +125°C, unless otherwise noted)

Characteristics	Test Condition	Symbol	Min	Typ	Max	Unit
SUPPLY SECTION AND V_{CC} MANAGEMENT						
Startup threshold at which driving pulses are authorized	V_{CC} increasing A, B, C versions D & E versions	$V_{CC(on)}$	 9.4 13.1	 10 14	 10.6 14.9	V
Minimum Operating voltage at which driving pulses are stopped	V_{CC} decreasing	$V_{CC(off)}$	8.4	9	9.6	V
Hysteresis between $V_{CC(on)}$ and $V_{CC(min)}$	A, B and C versions D & E versions	$V_{CC(HYS)}$	0.9 4.5	1.0 5.0	– –	V
Start−up current, controller disabled	V_{CC} < $V_{CC(on)}$ & V_{CC} increasing from zero	I_{CC1}	–	–	100	μA
Internal IC consumption, controller switching	F_{sw} =100 kHz, DRV = open	I_{CC2}	0.5	1.4	2.2	mA
Internal IC consumption, controller switching	F_{sw} =100 kHz, C_{DRV} = 1 nF	I_{CC3}	2.0	2.7	3.5	mA
CURRENT COMPARATOR						
Current Sense Voltage Threshold		V_{ILIM}	0.92	1	1.08	V
Leading Edge Blanking Duration		t_{LEB}	–	160	–	ns
Input Bias Current	(Note 3)	I_{bias}	–	0.02	–	μA
Propagation delay	From CS detected to gate turned off	t_{ILIM}	–	70	150	ns
Internal Ramp Compensation Voltage level	@ 25°C (Note 4)	V_{ramp}	3.15	3.5	3.85	V
Internal Ramp Compensation resistance to CS pin	@ 25°C (Note 4)	R_{ramp}	–	26.5	–	kΩ
INTERNAL OSCILLATOR						
Oscillator Frequency	R_T = 43 kΩ & DRV pin = 47 kΩ	f_{OSC}	92	100	108	kHz
Oscillator Frequency	R_T = 8.5 kΩ & DRV pin = 47 kΩ	f_{OSC}	425	500	550	kHz
Frequency Modulation in percentage of f_{OSC}	(Note 3)	f_{jitter}	–	±5	–	%
Frequency modulation Period	(Note 3)	T_{swing}	–	3.33	–	ms
Maximum operating frequency	(Note 3)	f_{MAX}	500	–	–	kHz
Maximum duty−cycle − A version		DC_{maxA}	45.6	48	49.6	%
Maximum duty−cycle − B version		DC_{maxB}	76	80	84	%
Maximum duty−cycle − C version		DC_{maxC}	61	65	69	%
Maximum duty−cycle − D & E versions		DC_{maxD}	44.2	45.6	47.2	%
FEEDBACK SECTION						
Internal voltage division from FB to CS setpoint		FB_{div}	–	3	–	–
Internal pull−up resistor		$R_{pull-up}$	–	3.5	–	kΩ
FB pin maximum current	FB pin = GND	I_{FB}	1.5	–	–	mA
Internal feedback impedance from FB to GND		Z_{FB}	–	40	–	kΩ
Open loop feedback voltage	FB pin = open	V_{FBOL}	–	6.0	–	V
Internal Diode forward voltage	(Note 3)	V_f	–	0.75	–	V
DRIVE OUTPUT						
DRV Source resistance		R_{SRC}	–	10	30	Ω
DRV Sink resistance		R_{SINK}	–	6	19	Ω

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Guaranteed by design
4. V_{ramp}, R_{ramp} Guaranteed by design

Table 3. ELECTRICAL CHARATERISTICS

(V_{CC} = 15 V, R_T = 43 kΩ, C_{DRV} = 1 nF. For typical values T_J = 25°C, for min/max values T_J = −25°C to +125°C, unless otherwise noted)

Characteristics	Test Condition	Symbol	Min	Typ	Max	Unit
DRIVE OUTPUT						
Output voltage rise−time	V_{CC} = 15 V, C_{DRV} = 1 nF, 10 to 90%	t_r	−	26	−	ns
Output voltage fall−time	V_{CC} = 15 V, C_{DRV} = 1 nF, 90 to 10%	t_f	−	22	−	ns
Clamping voltage (maximum gate voltage)	V_{CC} = 25 V R_{DRV} = 47 kΩ, C_{DRV} = 1 nF	V_{CL}	−	15	18	V
High−state voltage drop	V_{CC} = $V_{CC(min)}$ + 100 mV, R_{DRV} = 47 kΩ, C_{DRV} = 1 nF	$V_{DRV(clamp)}$	−	50	500	mV
CYCLE SKIP						
Skip cycle level		V_{skip}	0.2	0.3	0.4	V
Skip threshold Reset		$V_{skip(reset)}$	−	V_{skip}+ $V_{skip(HYS)}$	−	V
Skip threshold Hysteresis		$V_{skip(HYS)}$	−	25	−	mV
SOFT START						
Soft−start charge current	SS pin = GND	I_{SS}	8.8	10	11	μA
Soft start completion voltage threshold		V_{SS}	3.5	4.0	4.5	V
Internal delay before starting the Soft start when $V_{CC(on)}$ is reached	For A, B and C versions only − No delay for D & E versions	SS_{delay}	100	120	155	ms
PROTECTION						
Current sense fault voltage level triggering the timer		F_{CS}	0.9	1	1.1	V
Timer delay before latching a fault (overload or short circuit) − A/B/C/D versions	When CS pin > F_{CS}	T_{fault}	10	15	20	ms
Timer delay before latching a fault (overload or short circuit) − E version	When CS pin > F_{CS}	T_{fault}	120	155	200	ms
Brown−out voltage		V_{BO}	0.974	1	1.026	V
Internal current source generating the Brown−out hysteresis	−5°C ≤ T_J ≤ +125°C −25°C ≤ T_J ≤ +125°C	I_{BO}	8.8 8.6	10 10	11.2 11.2	μA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Guaranteed by design
4. V_{ramp}, R_{ramp} Guaranteed by design

Table 4. SELECTION TABLE

NCP1252	Start−up Delay	Duty Ratio Max	VCC Start (Typ.)	Fault Timer (Typ.)	Fault
A	Yes	50%	10 V	15 ms	Latched
B	Yes	80%	10 V	15 ms	Latched
C	Yes	65%	10 V	15 ms	Latched
D	No	47.5%	14 V	15 ms	Latched
E	No	47.5%	14 V	150 ms	Latched

TYPICAL CHARACTERISTICS

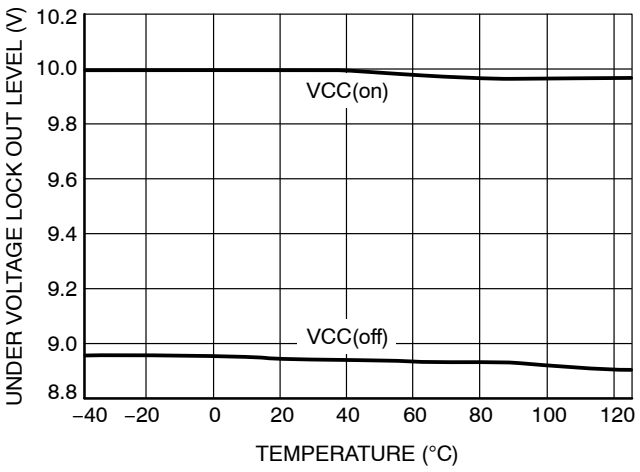


Figure 3. Supply Voltage Threshold vs. Junction Temperature (A, B and C Versions)

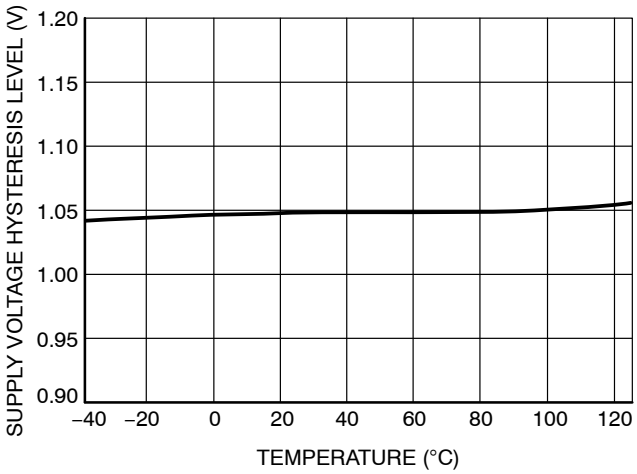


Figure 4. Supply Voltage Hysteresis vs. Junction Temperature (A, B and C Versions)

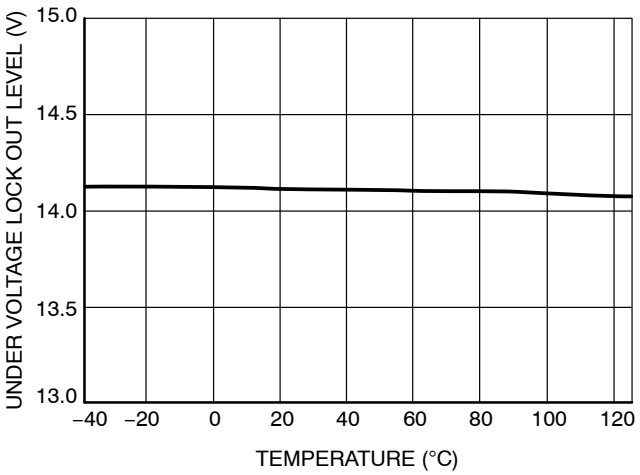


Figure 5. Supply Voltage $V_{CC(ON)}$ Threshold vs. Junction Temperature (D Version)

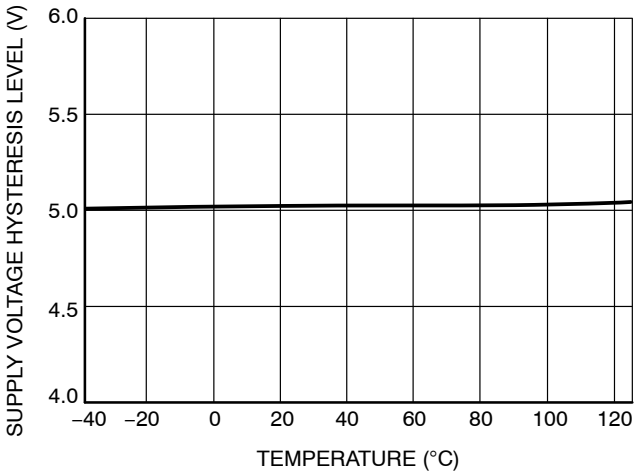


Figure 6. Supply Voltage Hysteresis vs. Junction Temperature (D Version)

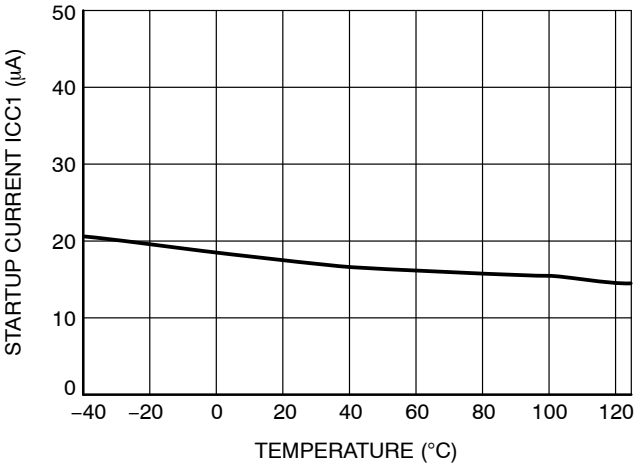


Figure 7. Start−up Current (I_{CC1}) vs. Junction Temperature

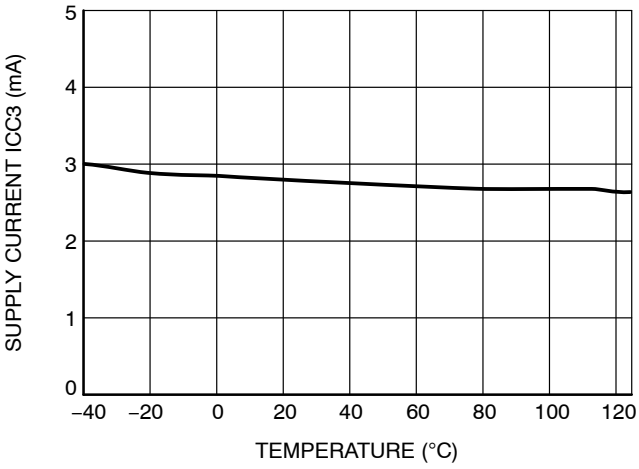


Figure 8. Supply Current (I_{CC3}) vs. Junction Temperature

TYPICAL CHARACTERISTICS

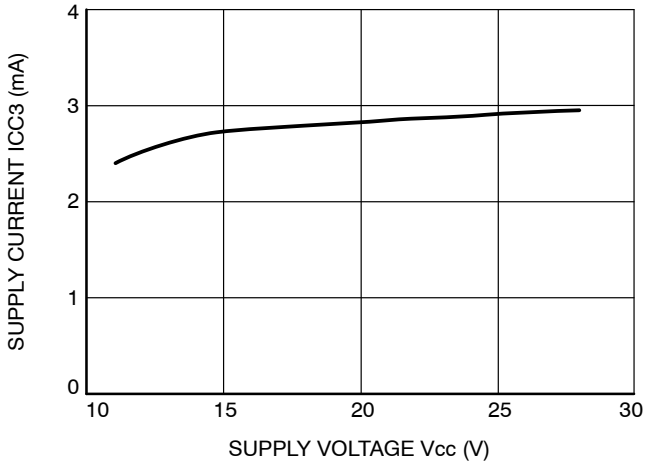


Figure 9. Supply Current (I_{CC3}) vs. Supply Voltage

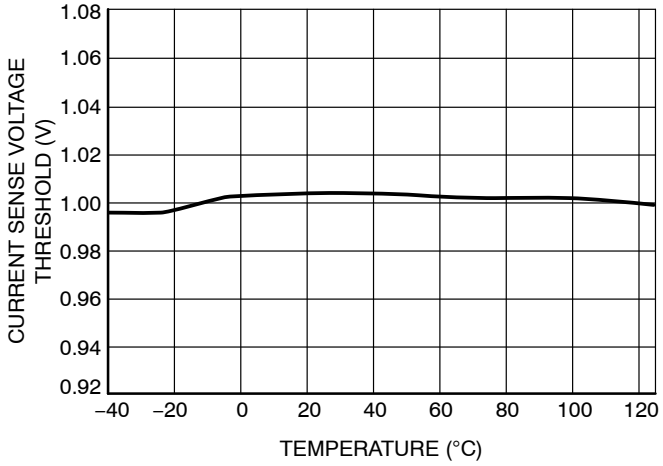


Figure 10. Current Sense Voltage Threshold vs. Junction Temperature

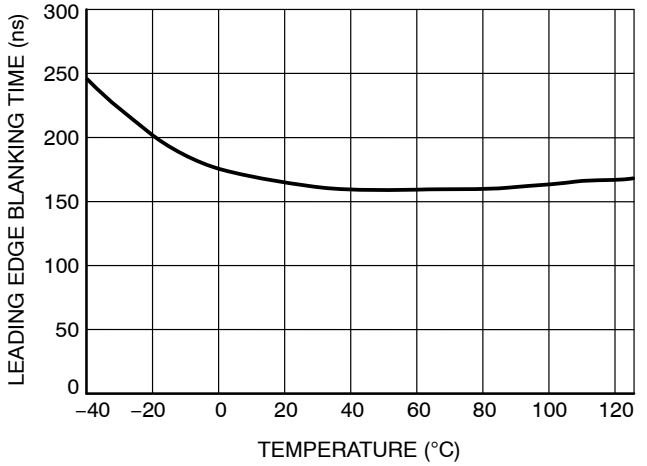


Figure 11. Leading Edge Blanking Time vs. Junction Temperature

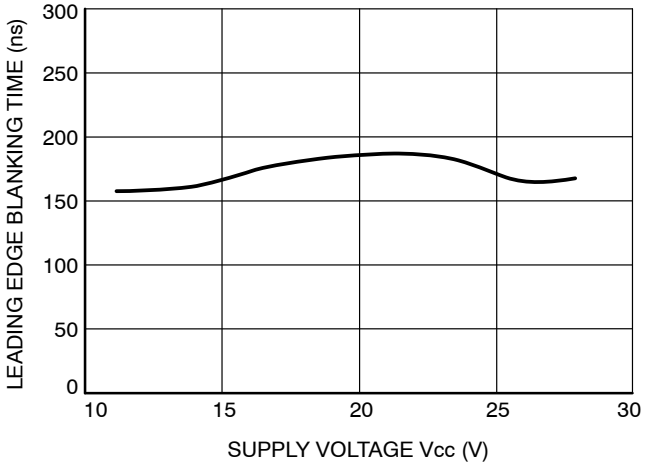


Figure 12. Leading Edge Blanking Time vs. Supply Voltage

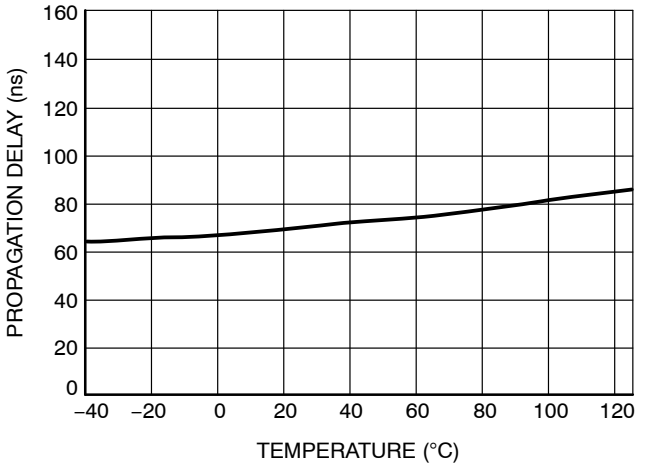


Figure 13. Propagation Delay from CS to DRV vs. Junction Temperature

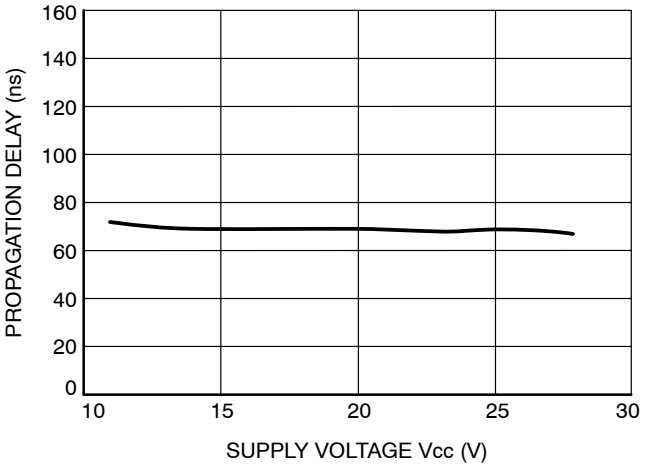


Figure 14. Propagation Delay from CS to DRV vs. Supply Voltage

TYPICAL CHARACTERISTICS

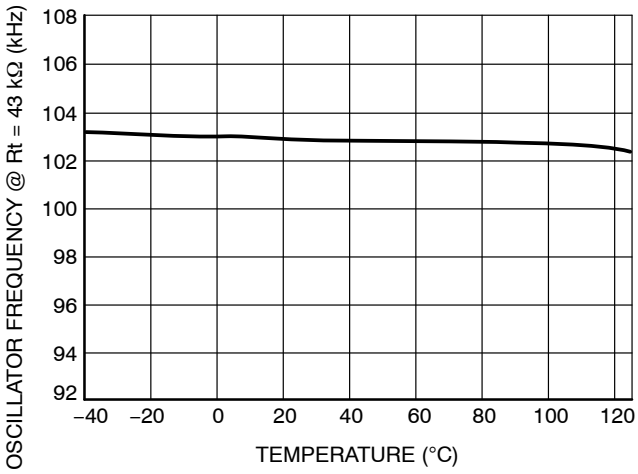


Figure 15. Oscillator Frequency vs. Junction Temperature

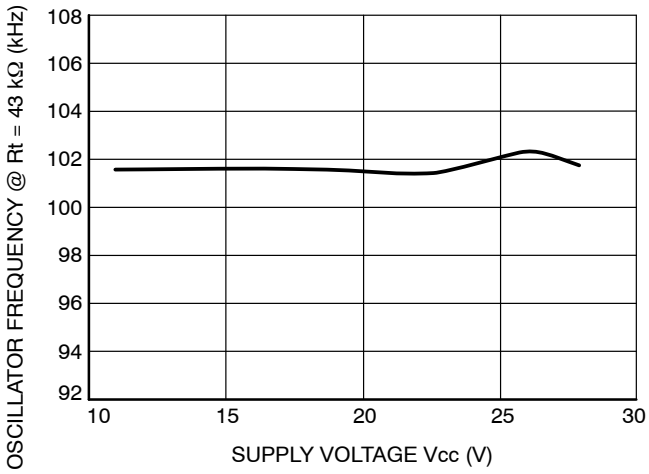


Figure 16. Oscillator Frequency vs. Supply Voltage

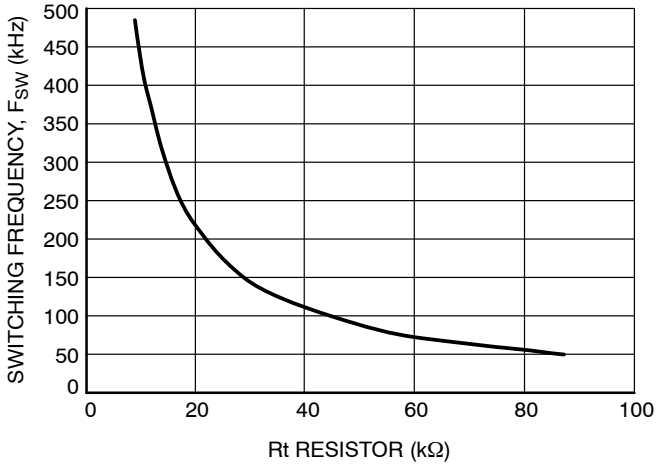


Figure 17. Oscillator Frequency vs. Oscillator Resistor

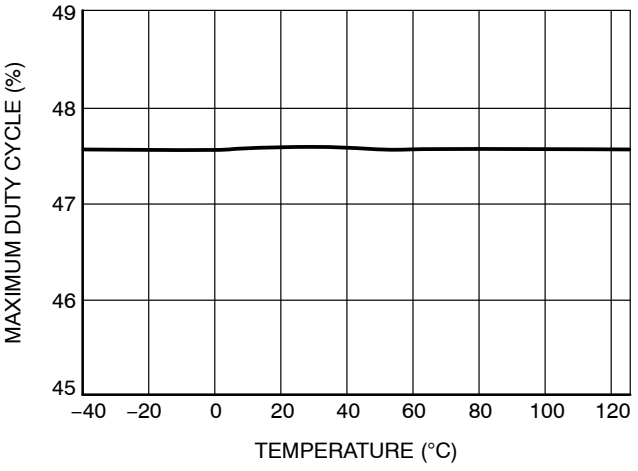


Figure 18. Maximum Duty−cycle, A Version vs. Junction Temperature

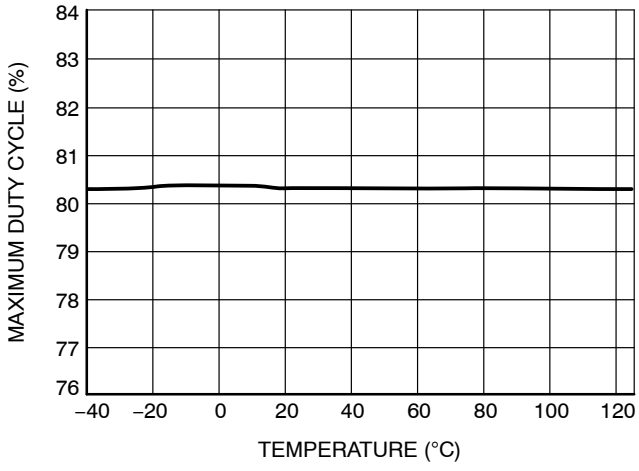


Figure 19. Maximum Duty−cycle, B Version vs. Junction Temperature

TYPICAL CHARACTERISTICS

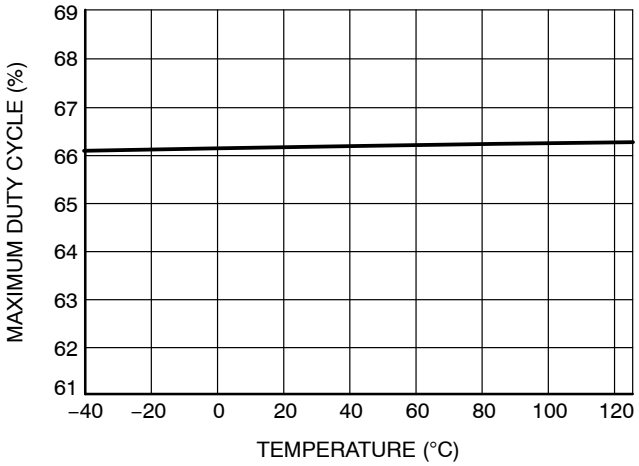


Figure 20. Maximum Duty−cycle, C Version vs. Junction Temperature

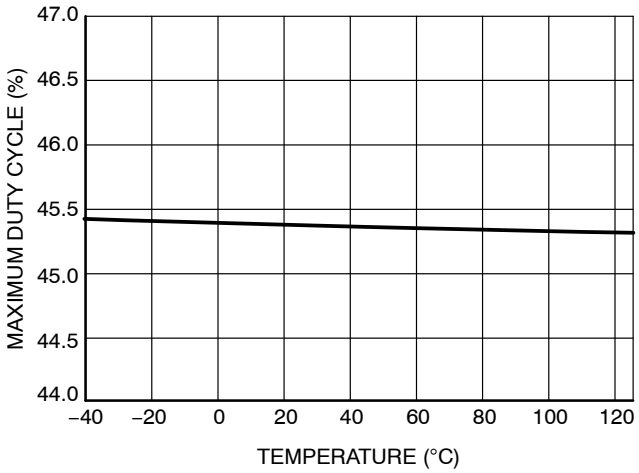


Figure 21. Maximum Duty−cycle, D Version vs. Junction Temperature

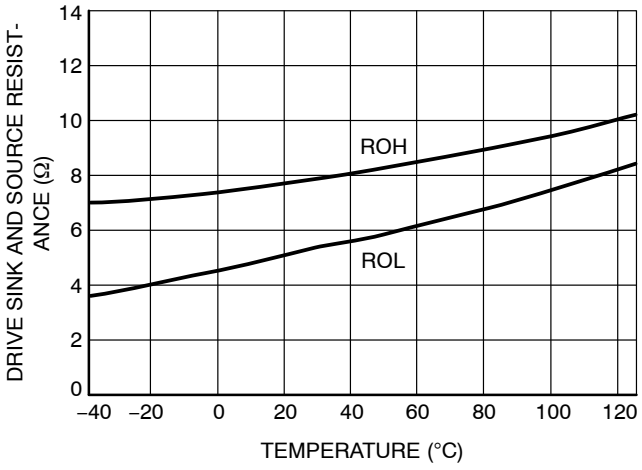


Figure 22. Drive Sink and Source Resistances vs. Junction Temperature

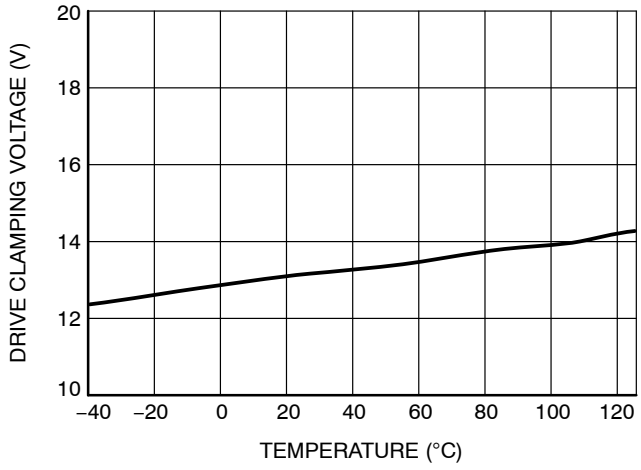


Figure 23. Drive Clamping Voltage vs. Junction Temperature

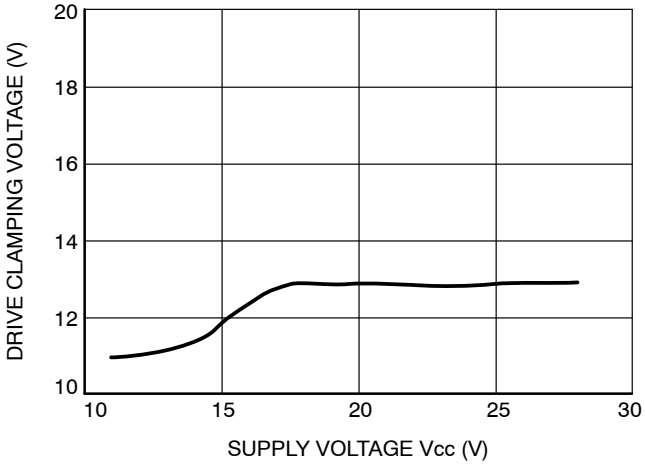


Figure 24. Drive Clamping Voltage vs. Supply Voltage

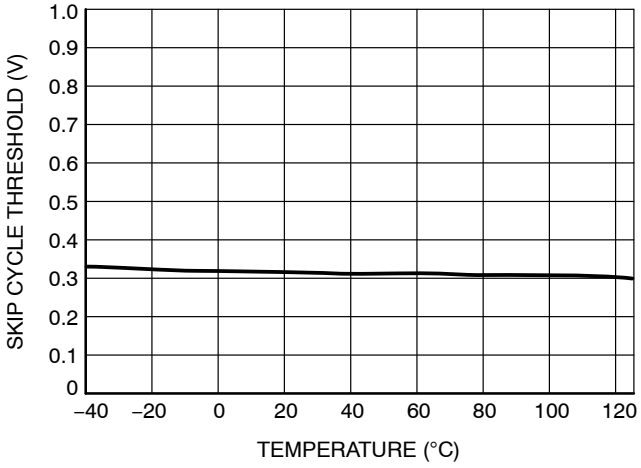


Figure 25. Skip Cycle Threshold vs. Junction Temperature

TYPICAL CHARACTERISTICS

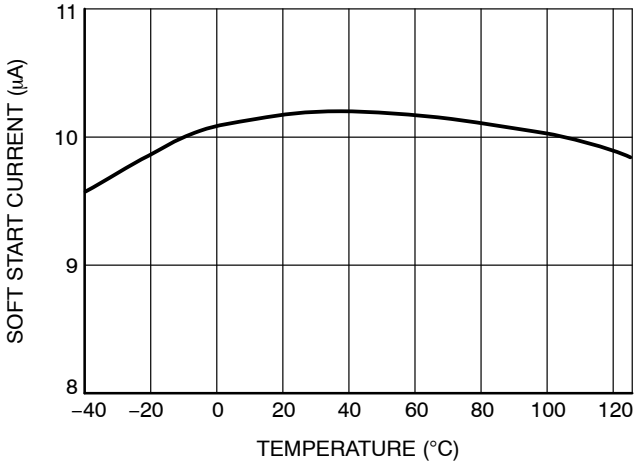


Figure 26. Soft Start Current vs. Junction Temperature

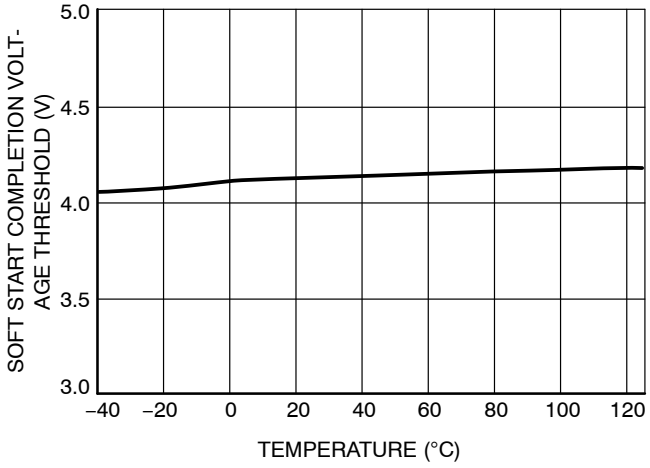


Figure 27. Soft Start Completion Voltage Threshold vs. Junction Temperature

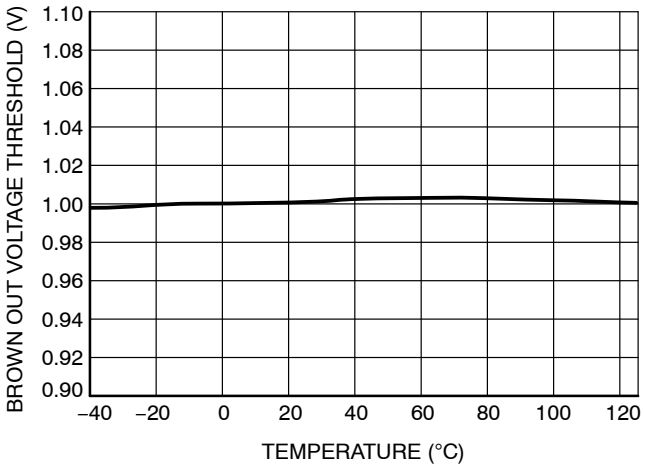


Figure 28. Brown Out Voltage Threshold vs. Junction Temperature

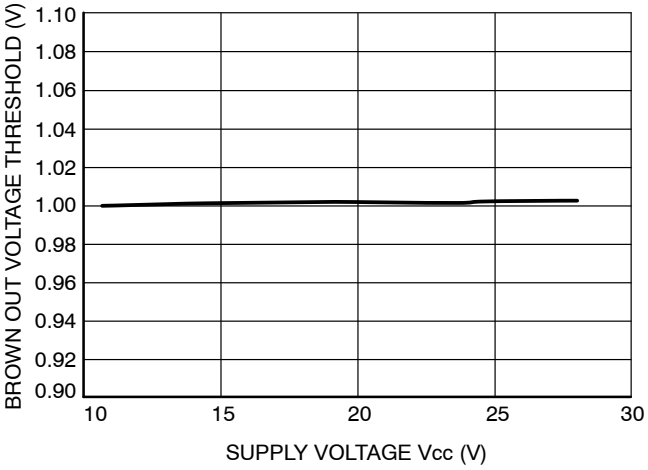


Figure 29. Brown Out Voltage Threshold vs. Supply Voltage

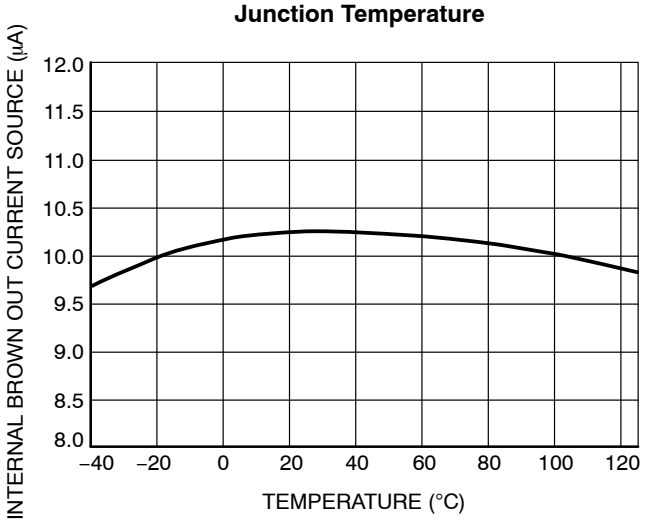


Figure 30. Internal Brown Out Current Source vs. Junction Temperature

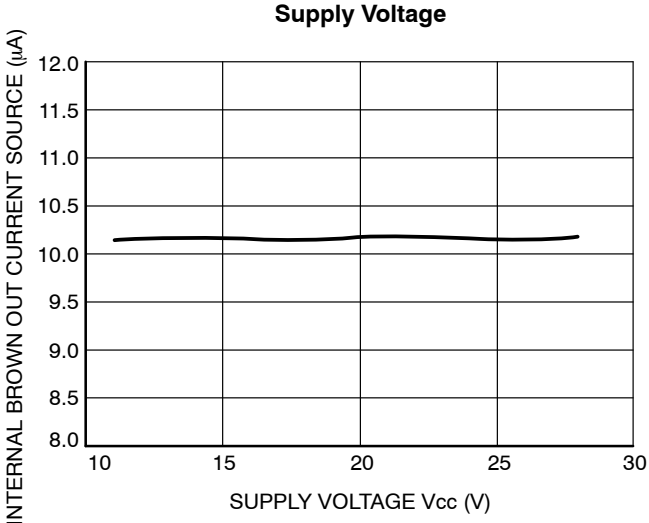


Figure 31. Internal Brown Out Current Source vs. Supply Voltage

APPLICATION INFORMATION

Introduction

The NCP1252 hosts a high−performance current−mode controller specifically developed to drive power supplies designed for the ATX and the adapter market:

- **Current Mode operation:** implementing peak current−mode control topology, the circuit offers UC384X−like features to build rugged power supplies.
- **Adjustable switching frequency:** a resistor to ground precisely sets the switching frequency between 50 kHz and a maximum of 500 kHz. There is no synchronization capability.
- **Internal frequency jittering:** Frequency jittering softens the EMI signature by spreading out peak energy within a band ±5% from the center frequency.
- **Wide Vcc excursion:** the controller allows operation up to 28 V continuously and accepts transient voltage up to 30 V during 10 ms with I_{VCC} < 20 mA
- **Gate drive clamping:** a lot of power MOSFETs do not allow their driving voltage to exceed 20 V. The controller includes a low−loss clamping voltage which prevents the gate from going beyond 15 V typical.
- **Low startup−current:** reaching a low no−load standby power represents a difficult exercise when the controller requires an external, lossy, resistor connected to the bulk capacitor. The start−up current is guaranteed to be less than 100 μA maximum, helping the designer to reach a low standby power level.
- **Short−circuit protection:** by monitoring the CS pin voltage when it exceeds 1 V (maximum peak current), the controller detects a fault and starts an internal digital timer. On the condition that the digital timer elapses, the controller will permanently latch−off. This allows accurate overload or short−circuit detection which is not dependant on the auxiliary winding. Reset occurs when: a) a BO reset is sensed, b) V_{CC} is cycled down to $V_{CC(min)}$ level. If the short circuit or the fault disappear before the fault timer ends, the fault timer is reset only if the CS pin voltage level is below 1 V at least during 3 switching frequency periods. This delay before resetting the fault timer prevents any false or missing fault or over load detection.
- **Adjustable soft−start:** the soft−start is activated upon a start−up sequence (V_{CC} going−up and crossing $V_{CC(on)}$) after a minimum internal time delay of 120 ms (SS_{delay}). But also when the brown−out pin is reset without in that case timer delay. This internal time delay gives extra time to the PFC to be sure that the output PFC voltage is in regulation. The soft start pin is grounded until the internal delay is ended. Please note that SS_{delay} is present only for A, B and C versions.
- **Shutdown:** if an external transistor brings the BO pin down, the controller is shut down, but all internal biasing circuits are alive. When the pin is released, a new soft−start sequence takes place.
- **Brown−Out protection:** BO pin permanently monitors a fraction of the input voltage. When this image is below the V_{BO} threshold, the circuit stays off and does not switch. As soon the voltage image comes back within safe limits, the pulses are re−started via a start−up sequence including soft−start. The hysteresis is implemented via a current source connected to the BO pin; this current source sinks a current (I_{BO}) from the pin to the ground. As the current source status depends on the brown−out comparator, it can easily be used for hysteresis purposes. A transistor pulling down the BO pin to ground will shut−off the controller. Upon release, a new soft−start sequence takes place.
- **Internal ramp compensation:** a simple resistor connected from the CS pin to the sense resistor allows the designer to inject ramp compensation inside his design.
- **Skip cycle feature:** When the power supply loads are decreasing to a low level, the duty cycle also decreases to the minimum value the controller can offer. If the output loads disappear, the converter runs at the minimum duty cycle fixed by the propagation delay and driving blocks. It often delivers too much energy to the secondary side and it trips the voltage supervisor. To avoid this problem, the FB is allowed to impose the min t_{ON} down to ~ V_f and it further decreases down to V_{skip}, zero duty cycle is imposed. This mode helps to ensure no−load outputs conditions as requested by recently updated ATX specifications. Please note that the converter first goes to min t_{ON} before going to zero duty cycle: normal operation is thus not disturbed. The following figure illustrates the different mode of operation versus the FB pin level.

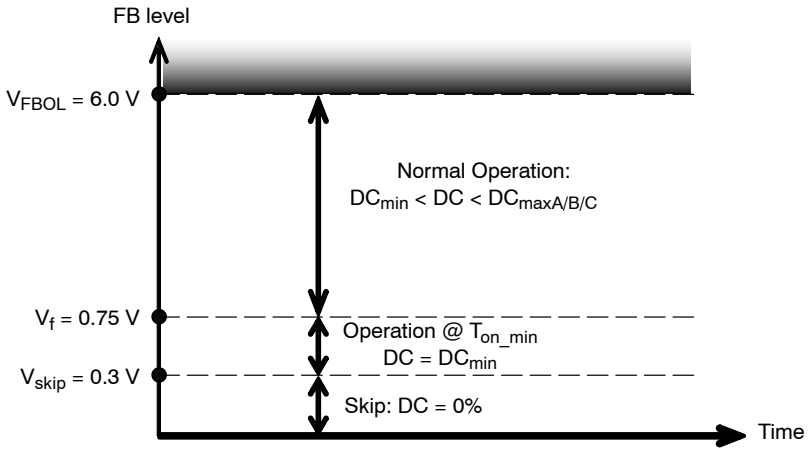


Figure 32. Mode of Operation versus the FB Pin Level

Startup Sequence:

The startup sequence is activated when Vcc pin reaches $V_{CC(on)}$ level. Once the startup sequence has been activated the internal delay timer (SS_{delay}) runs (except D version). Only when the internal delay elapses the soft start can be allowed if the BO pin level is above V_{BO} level. If the BO pin threshold is reached or as soon as this level will be reached the soft start is allowed. When the soft start is allowed the SS pin is released from the ground and the current source connected to this pin sources its current to the external capacitor connected on SS pin. The voltage variation of the SS pin divided by 4 gives the same peak current variation on the CS pin.

The following figures illustrate the different startup cases.

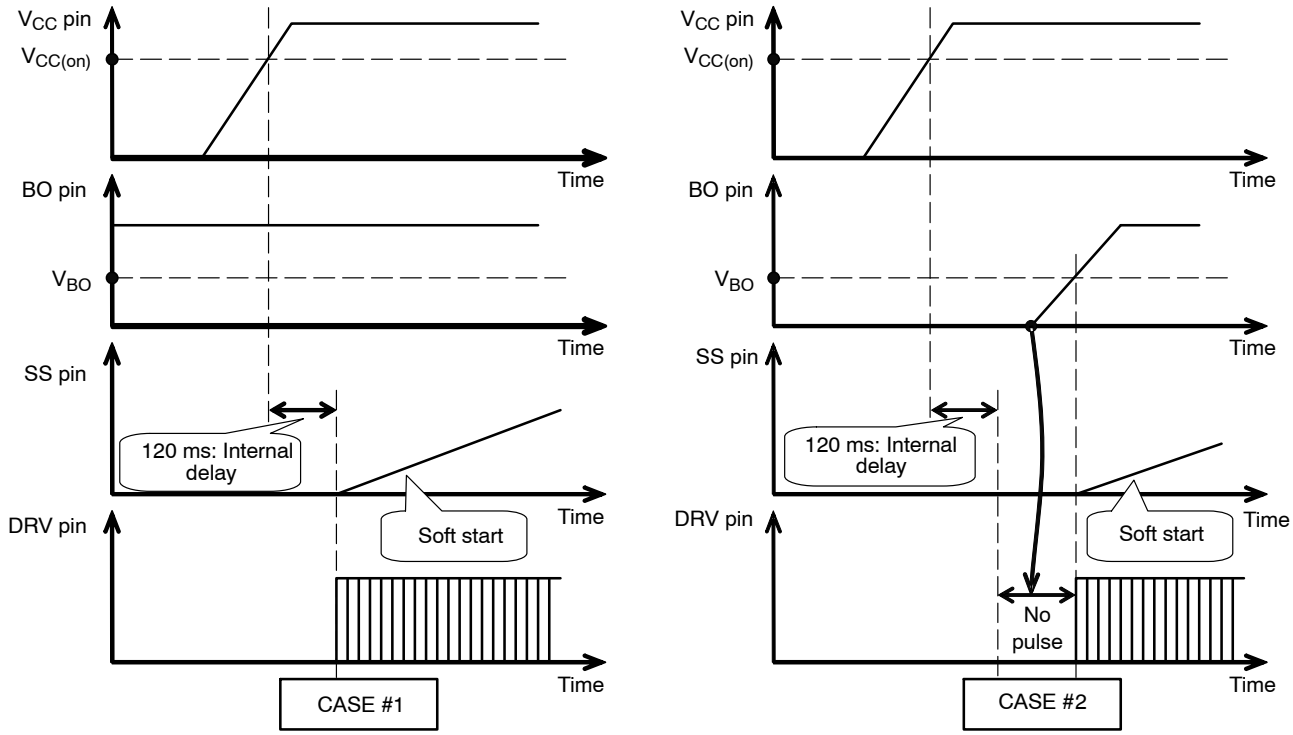


Figure 33. Different Startup Sequence Case #1 & #2 – (For A, B and C versions)

With the Case #1, when the V_{CC} pin reaches the $V_{CC(on)}$ level, the internal timer starts. As the BO pin level is above the V_{BO} threshold at the end of the internal delay, a soft start sequence is started.

With the Case #2, at the end of the internal delay, the BO pin level is below the V_{BO} threshold thus the soft start sequence can not start. A new soft start sequence will start only when the BO pin reaches the V_{BO} threshold.

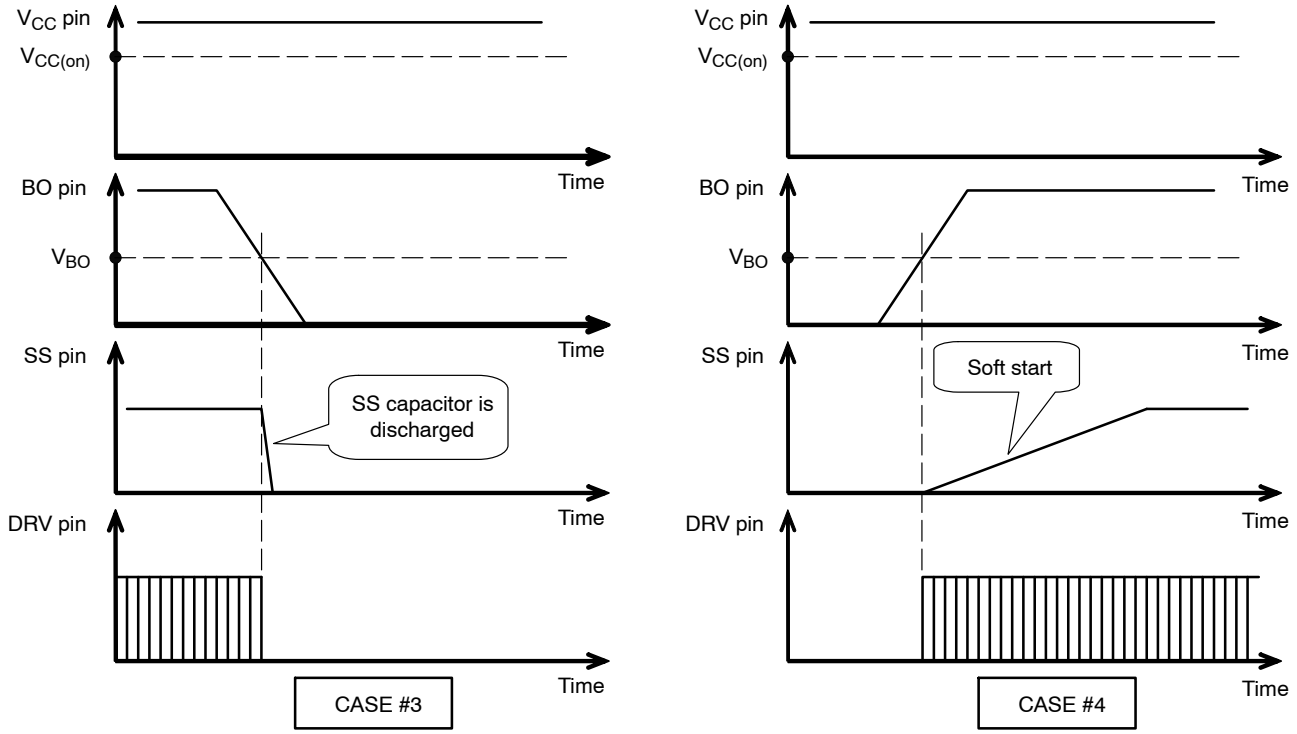


Figure 34. Controller Shuts Down with the Brown Out Pin

When the BO pin is grounded, the controller is shut down and the SS pin is internally grounded in order to discharge the soft start capacitor connected to this pin (Case #3). If the BO pin is released, when its level reaches the V_{BO} level a new soft start sequence happens.

Soft Start:

As illustrated by the following figure, the rising voltage on the SS pin voltage divided by 4 controls the peak current sensed on the CS pin. Thus as soon as the CS pin voltage becomes higher than the SS pin voltage divided by 4 the driver latch is reset.

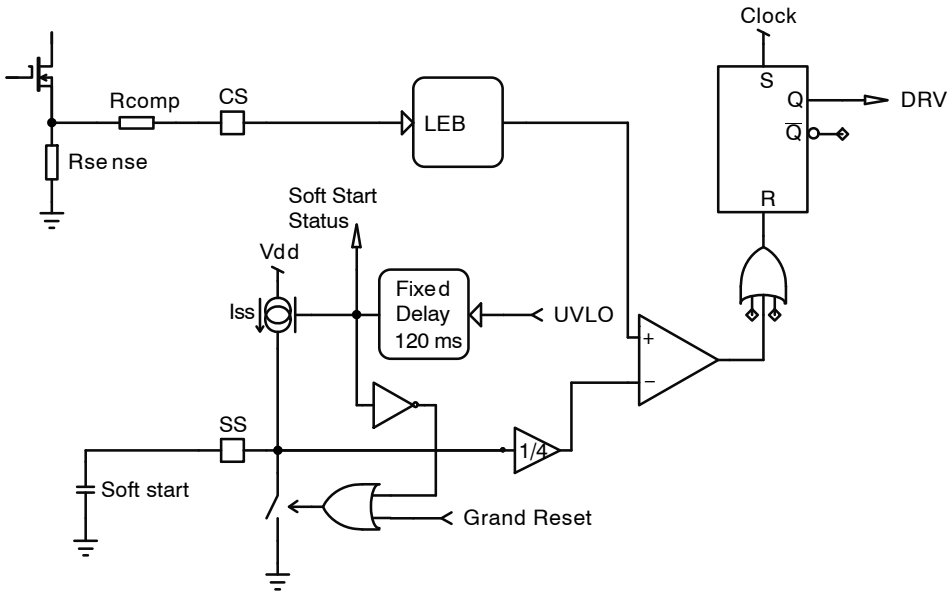


Figure 35. Soft Start Principle

The following figure illustrates a soft start sequence.

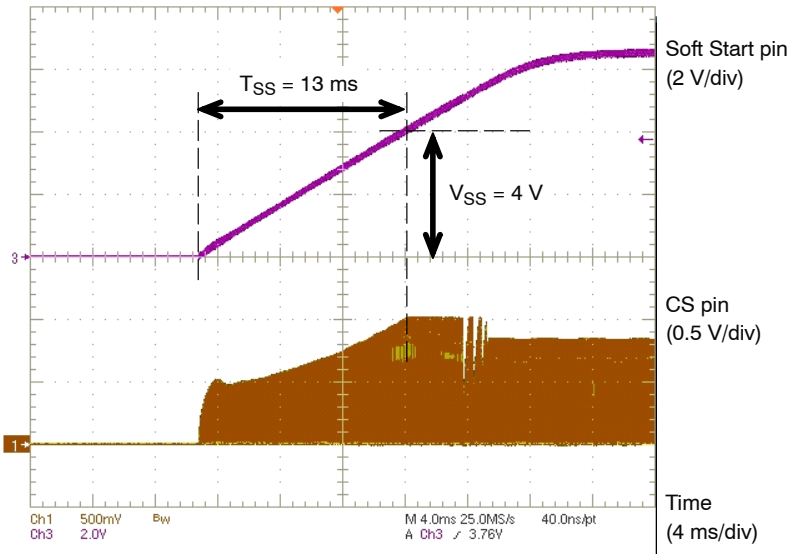


Figure 36. Soft Start Example

Brown−Out Protection

By monitoring the level on BO pin, the controller protects the forward converter against low input voltage conditions. When the BO pin level falls below the V_{BO} level, the controllers stops pulsing until the input level goes back to normal and resumes the operation via a new soft start sequence.

The brown−out comparator features a fixed voltage reference level (V_{BO}). The hysteresis is implemented by using the internal current connected between the BO pin and the ground when the BO pin is below the internal voltage reference (V_{BO}).

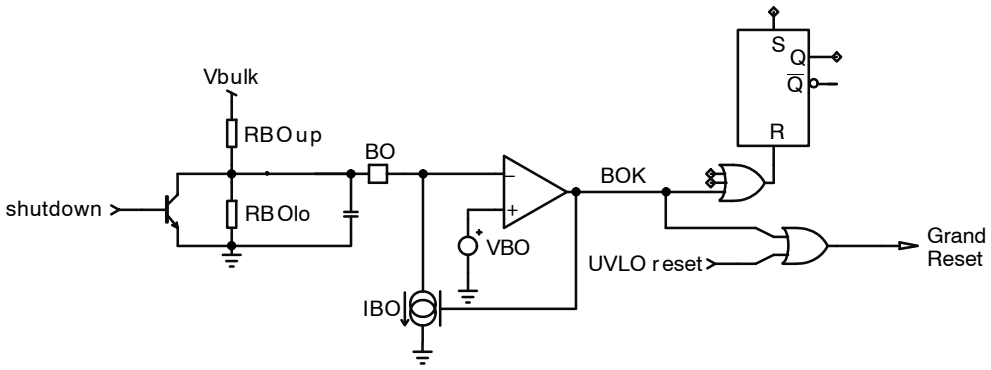


Figure 37. BO Pin Setup

The following equations show how to calculate the resistors for BO pin.

First of all, select the bulk voltage value at which the controller must start switching (V_{bulkon}) and the bulk voltage for shutdown ($V_{bulkoff}$) the controller.

Where:

- V_{bulkon} = 370 V
- $V_{bulkoff}$ = 350 V
- V_{BO} = 1 V
- I_{BO} = 10 μA

When BO pin voltage is below V_{BO} (internal voltage reference), the internal current source (I_{BO}) is activated. The following equation can be written:

$$V_{bulkON} = R_{BOup}\left(I_{BO} + \frac{V_{BO}}{R_{BOlo}}\right) + V_{BO} \qquad \text{(eq. 1)}$$

When BO pin voltage is higher than V_{BO}, the internal current source is now disabled. The following equation can be written:

$$V_{BO} = \frac{V_{bulkoff} R_{BOlo}}{R_{BOlo} + R_{BOup}} \qquad \text{(eq. 2)}$$

From Equation 2 it can be extracted the R_{BOup}:

$$R_{BOup} = \left(\frac{V_{bulkoff} - V_{BO}}{V_{BO}}\right) R_{BOlo} \qquad \text{(eq. 3)}$$

Equation 3 is substituted in Equation 1 and solved for R_{BOlo}, yields:

$$R_{BOlo} = \frac{V_{BO}}{I_{BO}}\left(\frac{V_{bulkon} - V_{BO}}{V_{bulkoff} - V_{BO}} - 1\right) \quad \text{(eq. 4)}$$

R_{BOup} can be also written independently of R_{BOlo} by substituting Equation 4 into Equation 3 as follow:

$$R_{BOup} = \frac{V_{bulkon} - V_{bulkoff}}{I_{BO}} \quad \text{(eq. 5)}$$

From Equation 4 and Equation 5, the resistor divider value can be calculated:

$$R_{BOlo} = \frac{1}{10\ \mu}\left(\frac{370 - 1}{350 - 1} - 1\right) = 5731\ \Omega$$

$$R_{BOup} = \frac{370 - 350}{10\ \mu} = 2.0\ M\Omega$$

Short Circuit or Over Load Protection:

A short circuit or an overload situation is detected when the CS pin level reaching its maximum level at 1 V. In that case the fault status is stored in the latch and allows the digital timer count. If the digital timer ends then the fault is latched and the controller permanently stops the pulses on the driver pin.

If the fault is gone before ending the digital timer, the timer is reset only after 3 switching controller periods without fault detection (or when the CS pin < 1 V during at least 3 switching periods).

If the fault is latched the controller can be reset if a BO reset is sensed or if V_{CC} is cycled down to $V_{CC(off)}$. The fault timer is typically set to 15 ms for A/B/C and D versions but is extended to 150 ms for the E version.

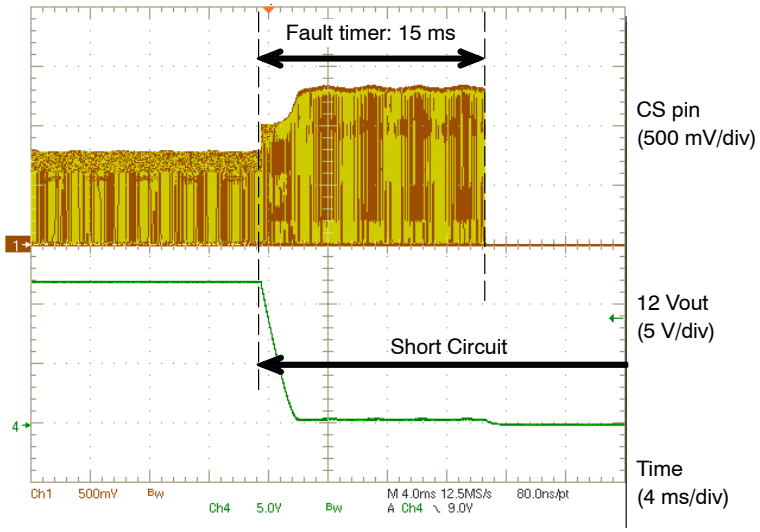


Figure 38. Short Circuit Detection Example

Shut Down

There is one possibility to shut down the controller; this possibility consists of grounding the BO pin as illustrated in Figure 37.

Slope Compensation

Slope compensation is a known mean to cure subharmonic oscillations. These oscillations take place at half of the switching frequency and occur only during Continuous Conduction Mode (CCM) with a duty−cycle close to and above 50%. To lower the current loop gain, one usually injects between 50 and 100% of the inductor downslope. Figure 39 depicts how internally the ramp is generated:

The compensation is derived from the oscillator via a buffer. A switch placed between the buffered internal oscillator ramp and R_{ramp} disconnects the compensation ramp during the OFF time DRV signal.

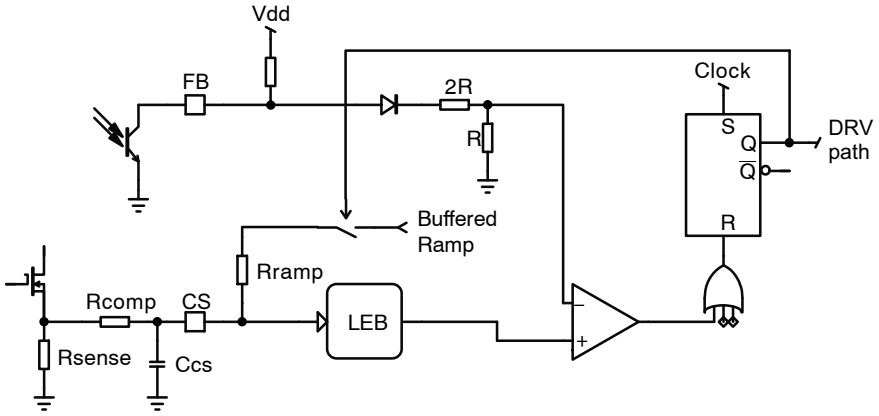


Figure 39. Ramp Compensation Setup

In the NCP1252, the internal ramp swings with a slope of:

$$S_{int} = \frac{V_{ramp}}{DC_{max}} F_{SW} \qquad \text{(eq. 6)}$$

In a forward application the secondary−side downslope viewed on a primary side requires a projection over the sense resistor R_{sense}. Thus:

$$S_{sense} = \frac{(V_{out} + V_f)}{L_{out}} \frac{N_s}{N_p} R_{sense} \qquad \text{(eq. 7)}$$

where:

- V_{out} is output voltage level
- V_f the freewheel diode forward drop
- L_{out}, the secondary inductor value
- N_s/N_p the transformer turn ratio
- R_{sense}: the sense resistor on the primary side

Assuming the selected amount of ramp compensation to be applied is δ_{comp}, then we must calculate the division ratio to scale down S_{int} accordingly:

$$Ratio = \frac{R_{sense}\delta_{comp}}{S_{int}} \qquad \text{(eq. 8)}$$

A few line of algebra determined Rcomp:

$$R_{comp} = R_{ramp} \frac{Ratio}{1 - Ratio} \qquad \text{(eq. 9)}$$

The previous ramp compensation calculation does not take into account the natural primary ramp created by the transformer magnetizing inductance. In some case illustrated here after the power supply does not need additional ramp compensation due to the high level of the natural primary ramp.

The natural primary ramp is extracted from the following formula:

$$S_{natural} = \frac{V_{bulk}}{L_{mag}} R_{sense} \qquad \text{(eq. 10)}$$

Then the natural ramp compensation will be:

$$\delta_{natural\_comp} = \frac{S_{natural}}{S_{sense}} \qquad \text{(eq. 11)}$$

If the natural ramp compensation ($\delta_{natural\_comp}$) is higher than the ramp compensation needed (δ_{comp}), the power supply does not need additional ramp compensation. If not, only the difference (δ_{comp}−$\delta_{natural\_comp}$) should be used to calculate the accurate compensation value.

Thus the new division ratio is:

$$\text{if} \quad \delta_{natural\_comp} < \delta_{comp} \Rightarrow Ratio = \frac{S_{sense}(\delta_{comp} - \delta_{natural\_comp})}{S_{int}} \qquad \text{(eq. 12)}$$

Then R_{comp} can be calculated with the same equation used when the natural ramp is neglected (Equation 9).

Ramp Compensation Design Example:

2 switch−Forward Power supply specification:

- Regulated output: 12 V
- L_{out} = 27 μH
- V_f = 0.7 V (drop voltage on the regulated output)
- Current sense resistor : 0.75 Ω
- Switching frequency : 125 kHz
- V_{bulk} = 350 V, minimum input voltage at which the power supply works.
- Duty cycle max: DC_{max} = 84%
- V_{ramp} = 3.5 V, Internal ramp level.
- R_{ramp} = 26.5 kΩ, Internal pull−up resistance
- Targeted ramp compensation level: 100%
- Transformer specification:
  - L_{mag} = 13 mH
  - N_s/N_p = 0.085

Internal ramp compensation level

$$S_{int} = \frac{V_{ramp}}{DC_{max}} F_{sw} \Rightarrow S_{int} = \frac{3.5}{0.84} 125\ kHz = 520\ mV / \mu s$$

Secondary−side downslope projected over the sense resistor is:

$$S_{sense} = \frac{(V_{out} + V_f)}{L_{out}} \frac{N_s}{N_p} R_{sense} \Rightarrow S_{sense} = \frac{(12 + 0.7)}{27 \cdot 10^{-6}} 0.085 \times 0.75 = 29.99\ mV / \mu s$$

Natural primary ramp:

$$S_{natural} = \frac{V_{bulk}}{L_{mag}} R_{sense} \Rightarrow S_{natural} = \frac{350}{13 \cdot 10^{-3}} 0.75 = 20.19\ mV / \mu s$$

Thus the natural ramp compensation is:

$$\delta_{natural\_comp} = \frac{S_{natural}}{S_{sense}} \Rightarrow \delta_{natural\_comp} = \frac{20.19}{29.99} = 67.3\%$$

Here the natural ramp compensation is lower than the desired ramp compensation, so an external compensation should be added to prevent sub−harmonics oscillation.

$$Ratio = \frac{S_{sense}(\delta_{comp} - \delta_{natural\_comp})}{S_{int}} \Rightarrow Ratio = \frac{29.99 \cdot (1.00 - 0.67)}{520} = 0.019$$

We can know calculate external resistor (R_{comp}) to reach the correct compensation level.

$$R_{comp} = R_{ramp} \frac{Ratio}{1 - Ratio} \Rightarrow R_{comp} = 26.5 \cdot 10^3 \frac{0.019}{1 - 0.019} = 509\ \Omega$$

Thus with R_{comp} = 510 Ω, 100% compensation ramp is applied on the CS pin.

The following example illustrates a power supply where the natural ramp offers enough ramp compensation to avoid external ramp compensation.

2 switch−Forward Power supply specification:

- Regulated output: 12 V
- L_{out} = 27 μH
- V_f = 0.7 V (drop voltage on the regulated output)
- Current sense resistor: 0.75 Ω
- Switching frequency: 125 kHz
- V_{bulk} = 350 V, minimum input voltage at which the power supply works.
- Duty cycle max: DC_{max} = 84%
- V_{ramp} = 3.5 V, Internal ramp level.
- R_{ramp} = 26.5 kΩ, Internal pull−up resistance
- Targeted ramp compensation level: 100%
- Transformer specification:
  - **L_{mag} = 7 mH**
  - N_s/N_p = 0.085

Secondary−side downslope projected over the sense resistor is:

$$S_{sense} = \frac{(V_{out} + V_f)}{L_{out}} \frac{N_s}{N_p} R_{sense} \Rightarrow S_{sense} = \frac{(12 + 0.7)}{27 \cdot 10^{-6}} 0.085 \times 0.75 = 29.99\ mV / \mu s$$

The natural primary ramp is:

$$S_{natural} = \frac{V_{bulk}}{L_{mag}} R_{sense} \Rightarrow S_{natural} = \frac{350}{7 \cdot 10^{-3}} 0.75 = 37.5\ mV / \mu s$$

And the natural ramp compensation will be:

$$\delta_{natural\_comp} = \frac{S_{natural}}{S_{sense}} \Rightarrow \delta_{natural\_comp} = \frac{37.5}{29.99} = 125\%$$

So in that case the natural ramp compensation due to the magnetizing inductance of the transformer will be enough to prevent any sub−harmonics oscillation in case of duty cycle above 50%.

Table 5. ORDERING INFORMATION

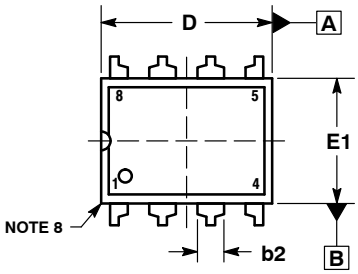
Device	Version	Marking	Shipping†
NCP1252APG	A	1252AP	50 Units / Rail
NCP1252ADR2G	A	1252A	2500 / Tape & Reel
NCP1252BDR2G	B	1252B	2500 / Tape & Reel
NCP1252CDR2G	C	1252C	2500 / Tape & Reel
NCP1252DDR2G	D	1252D	2500 / Tape & Reel
NCP1252EDR2G	E	1252E	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

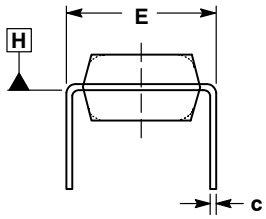
SCALE 1:1

PDIP–8
CASE 626–05
ISSUE P

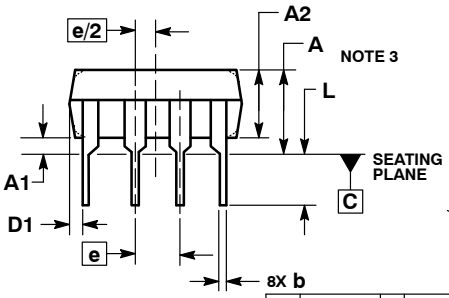
DATE 22 APR 2015



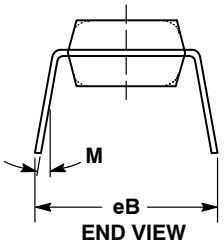
TOP VIEW



END VIEW
WITH LEADS CONSTRAINED
NOTE 5



SIDE VIEW



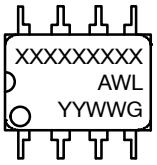
END VIEW
NOTE 6

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSIONS A, A1 AND L ARE MEASURED WITH THE PACKAGE SEATED IN JEDEC SEATING PLANE GAUGE GS–3.
4. DIMENSIONS D, D1 AND E1 DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS ARE NOT TO EXCEED 0.10 INCH.
5. DIMENSION E IS MEASURED AT A POINT 0.015 BELOW DATUM PLANE H WITH THE LEADS CONSTRAINED PERPENDICULAR TO DATUM C.
6. DIMENSION eB IS MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
7. DATUM PLANE H IS COINCIDENT WITH THE BOTTOM OF THE LEADS, WHERE THE LEADS EXIT THE BODY.
8. PACKAGE CONTOUR IS OPTIONAL (ROUNDED OR SQUARE CORNERS).

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	----	0.210	---	5.33
A1	0.015	----	0.38	---
A2	0.115	0.195	2.92	4.95
b	0.014	0.022	0.35	0.56
b2	0.060 TYP		1.52 TYP	
C	0.008	0.014	0.20	0.36
D	0.355	0.400	9.02	10.16
D1	0.005	----	0.13	---
E	0.300	0.325	7.62	8.26
E1	0.240	0.280	6.10	7.11
e	0.100 BSC		2.54 BSC	
eB	----	0.430	---	10.92
L	0.115	0.150	2.92	3.81
M	----	10°	---	10°

STYLE 1:
PIN 1. AC IN
2. DC + IN
3. DC – IN
4. AC IN
5. GROUND
6. OUTPUT
7. AUXILIARY
8. V_{CC}

GENERIC
MARKING DIAGRAM*



XXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb–Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb–Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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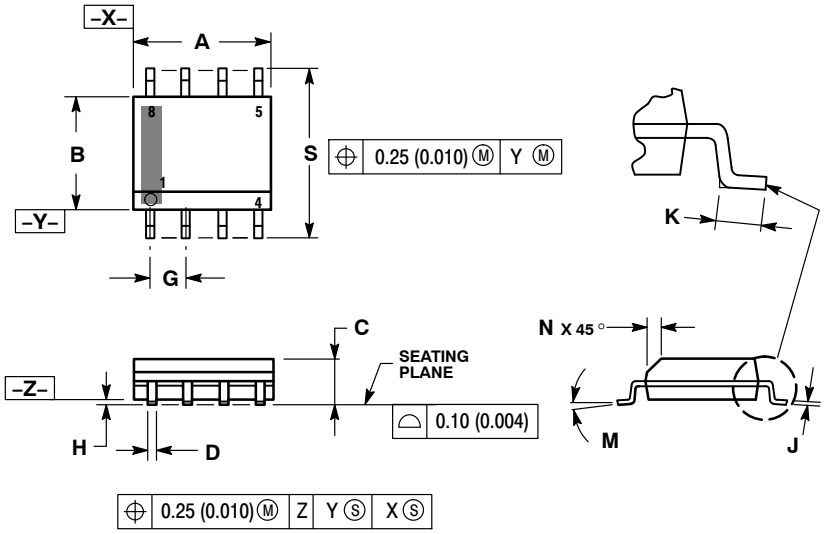
DESCRIPTION:	**PDIP–8**	**PAGE 1 OF 1**

SCALE 1:1

SOIC−8 NB
CASE 751−07
ISSUE AK

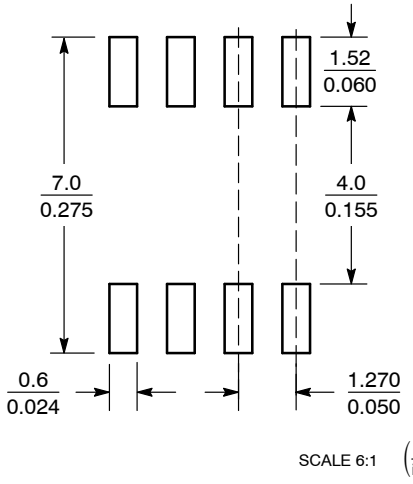
DATE 16 FEB 2011



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

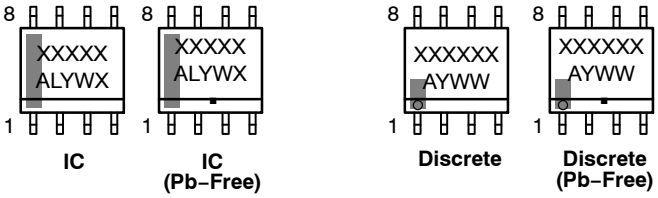
SOLDERING FOOTPRINT*



SCALE 6:1 (mm / inches)

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

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DESCRIPTION:	**SOIC−8 NB**		**PAGE 1 OF 2**

SOIC−8 NB
CASE 751−07
ISSUE AK

DATE 16 FEB 2011

STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. COLLECTOR
4. EMITTER
5. EMITTER
6. BASE
7. BASE
8. EMITTER

STYLE 2:
PIN 1. COLLECTOR, DIE, #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. BASE, #2
6. EMITTER, #2
7. BASE, #1
8. EMITTER, #1

STYLE 3:
PIN 1. DRAIN, DIE #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. GATE, #2
6. SOURCE, #2
7. GATE, #1
8. SOURCE, #1

STYLE 4:
PIN 1. ANODE
2. ANODE
3. ANODE
4. ANODE
5. ANODE
6. ANODE
7. ANODE
8. COMMON CATHODE

STYLE 5:
PIN 1. DRAIN
2. DRAIN
3. DRAIN
4. DRAIN
5. GATE
6. GATE
7. SOURCE
8. SOURCE

STYLE 6:
PIN 1. SOURCE
2. DRAIN
3. DRAIN
4. SOURCE
5. SOURCE
6. GATE
7. GATE
8. SOURCE

STYLE 7:
PIN 1. INPUT
2. EXTERNAL BYPASS
3. THIRD STAGE SOURCE
4. GROUND
5. DRAIN
6. GATE 3
7. SECOND STAGE Vd
8. FIRST STAGE Vd

STYLE 8:
PIN 1. COLLECTOR, DIE #1
2. BASE, #1
3. BASE, #2
4. COLLECTOR, #2
5. COLLECTOR, #2
6. EMITTER, #2
7. EMITTER, #1
8. COLLECTOR, #1

STYLE 9:
PIN 1. EMITTER, COMMON
2. COLLECTOR, DIE #1
3. COLLECTOR, DIE #2
4. EMITTER, COMMON
5. EMITTER, COMMON
6. BASE, DIE #2
7. BASE, DIE #1
8. EMITTER, COMMON

STYLE 10:
PIN 1. GROUND
2. BIAS 1
3. OUTPUT
4. GROUND
5. GROUND
6. BIAS 2
7. INPUT
8. GROUND

STYLE 11:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

STYLE 12:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 13:
PIN 1. N.C.
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 14:
PIN 1. N−SOURCE
2. N−GATE
3. P−SOURCE
4. P−GATE
5. P−DRAIN
6. P−DRAIN
7. N−DRAIN
8. N−DRAIN

STYLE 15:
PIN 1. ANODE 1
2. ANODE 1
3. ANODE 1
4. ANODE 1
5. CATHODE, COMMON
6. CATHODE, COMMON
7. CATHODE, COMMON
8. CATHODE, COMMON

STYLE 16:
PIN 1. EMITTER, DIE #1
2. BASE, DIE #1
3. EMITTER, DIE #2
4. BASE, DIE #2
5. COLLECTOR, DIE #2
6. COLLECTOR, DIE #2
7. COLLECTOR, DIE #1
8. COLLECTOR, DIE #1

STYLE 17:
PIN 1. VCC
2. V2OUT
3. V1OUT
4. TXE
5. RXE
6. VEE
7. GND
8. ACC

STYLE 18:
PIN 1. ANODE
2. ANODE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. CATHODE
8. CATHODE

STYLE 19:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. MIRROR 2
7. DRAIN 1
8. MIRROR 1

STYLE 20:
PIN 1. SOURCE (N)
2. GATE (N)
3. SOURCE (P)
4. GATE (P)
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 21:
PIN 1. CATHODE 1
2. CATHODE 2
3. CATHODE 3
4. CATHODE 4
5. CATHODE 5
6. COMMON ANODE
7. COMMON ANODE
8. CATHODE 6

STYLE 22:
PIN 1. I/O LINE 1
2. COMMON CATHODE/VCC
3. COMMON CATHODE/VCC
4. I/O LINE 3
5. COMMON ANODE/GND
6. I/O LINE 4
7. I/O LINE 5
8. COMMON ANODE/GND

STYLE 23:
PIN 1. LINE 1 IN
2. COMMON ANODE/GND
3. COMMON ANODE/GND
4. LINE 2 IN
5. LINE 2 OUT
6. COMMON ANODE/GND
7. COMMON ANODE/GND
8. LINE 1 OUT

STYLE 24:
PIN 1. BASE
2. EMITTER
3. COLLECTOR/ANODE
4. COLLECTOR/ANODE
5. CATHODE
6. CATHODE
7. COLLECTOR/ANODE
8. COLLECTOR/ANODE

STYLE 25:
PIN 1. VIN
2. N/C
3. REXT
4. GND
5. IOUT
6. IOUT
7. IOUT
8. IOUT

STYLE 26:
PIN 1. GND
2. dv/dt
3. ENABLE
4. ILIMIT
5. SOURCE
6. SOURCE
7. SOURCE
8. VCC

STYLE 27:
PIN 1. ILIMIT
2. OVLO
3. UVLO
4. INPUT+
5. SOURCE
6. SOURCE
7. SOURCE
8. DRAIN

STYLE 28:
PIN 1. SW_TO_GND
2. DASIC_OFF
3. DASIC_SW_DET
4. GND
5. V_MON
6. VBULK
7. VBULK
8. VIN

STYLE 29:
PIN 1. BASE, DIE #1
2. EMITTER, #1
3. BASE, #2
4. EMITTER, #2
5. COLLECTOR, #2
6. COLLECTOR, #2
7. COLLECTOR, #1
8. COLLECTOR, #1

STYLE 30:
PIN 1. DRAIN 1
2. DRAIN 1
3. GATE 2
4. SOURCE 2
5. SOURCE 1/DRAIN 2
6. SOURCE 1/DRAIN 2
7. SOURCE 1/DRAIN 2
8. GATE 1

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