# NCP1230 90 Watt, Universal Input Adapter Power Supply Evaluation Board User's Manual



# ON Semiconductor®

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# **EVAL BOARD USER'S MANUAL**

#### **General Description**

The NCP1230 implements a standard current mode control architecture. It's an ideal candidate for applications where a low parts count is a key parameter, particularly in low cost adapter power supplies. The NCP1230 combines a low standby power mode with an event management scheme that will disable a PFC circuit during Standby, thus reducing the no load power consumption. The 90 W Evaluation Board demonstrates the wide range of features found on the NCP1230 controller.

The NCP1230 has a PFC\_Vcc output pin which provides Vcc power for a PFC controller, or other circuitry. The PFC Vcc pin is enabled when the output of the power supply is up and in regulation. In the event that there is an output fault, the PFC\_Vcc pin is turned off, disabling the PFC controller, reducing the stress on the PFC semiconductors.

In addition to excellent no load power consumption, the NCP1230 provides an internal latching function that can be used for over voltage protection by pulling the CS pin above 3.0 V.

### **Features**

- Current−Mode Control
- Lossless Startup Circuit
- Operation Over the Universal Input Range
- Direct Connection to PFC Controller
- Low Standby
- Overvoltage Protection



**Figure 1. Evaluation Board Photo**

#### **Design Specification**

This Demo Board is configured as a two stage adapter power supply. The first stage operates off of the universal input, 85−265 Vac, 50−60 Hz, using the MC33260 Critical Conduction Mode controller, in the Boost Follower mode. The output voltage from the Boost Follower (when Vin is 85 Vac) is 200 V and as the input line increases to 230 Vac the output of the Boost Follower will ramp up to 400 Vdc. The second stage of the power supply features the NCP1230 driving a flyback power stage. The output of the second stage is 19 Vdc capable of 90 W of output power. It is fully self−contained and includes a bias supply that operates off of the Auxiliary winding of the transformer.

### **Table 1. EVALUATION BOARD SPECIFICATIONS**



#### **PFC**

The MC33260 is configured as a Boost Follower operating from the universal input line. The PFC section was designed to provide approximately 116 W of power.

$$
lpk = \frac{2 \cdot \sqrt{2} \cdot \text{Pin max}}{\text{Vac}}
$$

$$
lpk = \frac{2 \cdot \sqrt{2} \cdot 116}{85} = 3.86 \text{ A}
$$

The MC33260 is a Critical Conduction Mode controller; as a result the switching frequency is a function of the boost inductor and the timing capacitor. In this application the minimum operating frequency is 30 kHz.

$$
Lp = \frac{2 \cdot Tp \left(\frac{V \cdot o}{\sqrt{2}} - \sqrt{ac}\right) \cdot (\sqrt{ac})^2}{V o \cdot \sqrt{ac} \cdot lpk}
$$

$$
Lp = \frac{2 \cdot 33.33 \left(\frac{200}{\sqrt{2}} - 85\right) \cdot (85)^2}{200 \cdot 85 \cdot 3.86} = 414 \ \mu H
$$

The value used is 400  $\mu$ H.

Where:

$$
Tp = \frac{1}{\text{Freq min}} = \frac{1}{30} = 33.33 \text{ }\mu\text{ sec}
$$

Vomin =  $200$  Vdc ( $@$  85 Vac input)  $Vac = 85$  Vac

The oscillator timing capacitor is calculated by the following formula:

$$
CT = \frac{4 \text{ Vo}^2 \text{ Kosc} \text{ Lp Pin}}{\text{Ro}^2 \text{ Vpk}^2} - \text{Cint}
$$

$$
CT = \frac{4 \cdot 200^2 \cdot 6400 \cdot 400 \cdot 116}{2^2 \cdot 120^2} - 15 = 809 \text{ pF}
$$

Where:

 $Kosc = 6400$  $Ro = 2.0 M\Omega$  (feedback resistor) The CT value used is 820 pF

Refer to the ON Semiconductor website for Application Note AND8123/D for additional MC33260 application information, and the Excel based development tool DDTMC33260/D.

#### **Startup Circuit Description**

The High Voltage pin (pin 8) of the NCP1230 controller is connected directly to the high voltage DC bus. When the input power is turned on, an internal current source is turned on (typically 3.0 mA) charging up an external capacitor on the Vcc pin. When the Vcc capacitor is above VCCoff, the current source is turned off, and the controller delivers output drive pulses to an external MOSFET, Q1. The MOSFET, Q1, drives the primary of the transformer T1. The transformer has two additional windings, the auxiliary winding which provides power to the controller after the power supply is running, and the secondary winding which provided the 19 Vdc output power.

#### **Transformer**

The transformer primary inductance was selected so the current would be discontinuous under all operating conditions. As a result the total switching period, Ton + Toff, must be less than or equal to 1/frequency.

The following assumptions were used in the design process:

Dmax = 0.4 Duty Cycle

\nVdc bus = 200 Vdc input with Vin 85 Vac  
\nEfficiency = 0.80  
\nFreq = 65 kHz  
\nVo = 19 V  
\nVf = 0.7  
\nPo = 90 W  
\nPin = 
$$
\frac{Po}{\eta} = \frac{90}{0.8} = 112.5 W
$$
  
\nlavg =  $\frac{Pin}{Vin} = \frac{112.5}{200} = 0.566$   
\n $Lp = \frac{2 \cdot Pin}{\left(\frac{2 \cdot \text{lawg}}{\text{Dmax}}\right) \cdot \text{Freq}}$   
\n $Lp = \frac{2 \cdot 112.5}{\left(\frac{2 \cdot 0.566}{0.4}\right)^2 65} = 432 \, \mu H$ \n

 $\big($ 

In this application the primary inductance used is  $220 \mu H$ . This takes into consideration the transformer tolerances, and to minimize the transformer size. Once the primary inductance has been calculated, the next step is to determine the peak primary current.

$$
\text{Pin} = \frac{1}{2} \cdot \text{lpk}^2 \cdot \text{Lp} \cdot \text{f}
$$
\n
$$
\text{lpk} = \sqrt{\frac{\text{Pin} \cdot 2}{\text{Lp} \cdot \text{f}}}
$$
\n
$$
\text{lpk} = \sqrt{\frac{2 \cdot 112.5}{220 \cdot 65}} = 3.97 \text{ Apk}
$$

The following calculations are used to verify that the current will be Discontinuous under all operating conditions.

$$
Tp = Ton + Toff > \frac{1}{freq}
$$

$$
Ton = \frac{Lp \cdot lpk}{ Vin}
$$

$$
Toff = \frac{Ls \cdot lopk}{Vo + Vf}
$$

$$
Tp = \left(\frac{Lp \cdot lpk}{ Vin}\right) + \left(\frac{Ls \cdot lopk}{Vo + Vf}\right)
$$

Where:

$$
Ls = \frac{Lp}{n^2}
$$

n is the transformer turns ratio 6.77

$$
Tp = \frac{220 \cdot 3.97}{200} + \frac{4.8 \cdot 27.22}{19 + 0.7} = 10 \,\mu s
$$

With a primary inductance value of  $220 \mu H$ , Ton + Toff is less than the controller switching period. An Excel spreadsheet was designed using the above equation to help calculate the correct primary inductance value; visit the ON Semiconductor website for a copy of the spreadsheet.

One method for calculating the transformer turns ratio is to minimize the voltage stress of the MOSFET  $(V_{DS})$  due to the reflected output voltage.

### V<sub>DSmax</sub> = Vinmax + n · (Vo + Vf) + Vspike

In this application an 800 V MOSFET was selected. The goal, for safety purposes, is to limit  $V_{DSmax}$  at high line (including the Vspike) to 700 V. To limit the power dissipation in the snubber clamp (refer to the section in the Applications Note titled "Snubber".) Vspike is clamped at 167 V.

$$
n = \frac{VDSmax - Vinmax - Vspike}{Vo + Vf}
$$

$$
n = \frac{700 - 400 - 167}{19.7} = 6.77
$$

The NCP1230 requires that the controller Vcc be supplied through an auxiliary winding on the transformer. The nominal supply voltage for the controller is 13 Vdc.

$$
n_{\text{aux}} = \frac{\text{Vaux}(1 - \text{D} \text{max})}{\text{Vin} \cdot \text{D} \text{max}}
$$

$$
n_{\text{aux}} = \frac{13.7(1 - 0.4)}{200(0.4)} = 0.128
$$

The supply voltage to the controller may be higher than the calculated value because of the transformer leakage inductance. The leakage inductance spike on the auxiliary winding is averaged by the rectifier D2 and capacitor C5. Because of this, an 18 V Zener diode (D18 refer to the Demo Board Schematic Figure [10\)](#page-9-0) is connected from the Vcc pin to ground. To limit the current into the Zener diode a 200  $\Omega$ resistor is placed between C5 and the Vcc pin (R28).

ON Semiconductor recommends that the Vcc capacitor be at least  $47 \mu$ F to be sure that the Vcc supply voltage does not drop below Vccmin (7.6 V typical) during standby power mode and unusual fault conditions.

The transformer primary rms current is:

$$
Irms = Ipk \sqrt{\frac{Don}{3}} = 3.97 \sqrt{\frac{0.4}{3}} = 1.45 \text{ Arms}
$$

The transformer secondary rms current is:

$$
Irms\_sec = 1pk\_prim \cdot n \sqrt{\frac{1-D}{3}}
$$
  
= 3.97 \cdot 6.77  $\sqrt{\frac{0.6}{3}}$  = 12.02 Arms

The transformer for the Demo Board was manufactured by Cooper Electronics Technologies (www.cooperET.com) part number CTX22−16134. The designer should take precautions that under startup conditions, the transformer will not saturate at the low input ac line (85 Vac) and full load conditions. The above calculation assumed that the adapter was running and the PFC front end was enabled.

#### **Output Filter**

One of the disadvantages of a Flyback converter operating in the Discontinuous mode is there is a large ripple current

in the output capacitor(s). As a result you may be required to use multiple capacitors in parallel to handle the ripple current.

$$
I_{cap\_right} = \sqrt{10 \cdot 10^2 + 10^2}
$$
  
\n
$$
I_{cap\_right} = \sqrt{12.02^2 - 4.74^2} = 11.04 \text{ A}
$$
  
\n
$$
T_{on} = \frac{1}{frequency} \quad 0.4 = \frac{1}{65000} \quad 0.4 = 6.15 \text{ }\mu \text{ sec}
$$
  
\n
$$
C_{on} = \frac{\text{lorms} \cdot (T_{on})}{V_{in}} = \frac{1}{r_{in}}
$$

Where Vripple = 50 mV.

$$
Co = \frac{12.02 \cdot (15.38 - 9.23)}{0.05} = 1,478 \,\mu\text{F}
$$

In the 90 W Adapter design four 2200  $\mu$ F (8800  $\mu$ F total) capacitors (C2, C3, C14, and C15) were required in parallel to handle the ripple current.

A small LC filter has been added to the output of the power supply to help reduce the output ripple. The cut−off frequency for the filter is:

$$
fp = \frac{1}{2\pi\sqrt{LC}} = \frac{1}{2\pi\sqrt{2.2 \cdot 47}} = 15.6 \text{ kHz}
$$
  
L1 = 2.2 µH  
CS = 47 µF

#### **Output Rectifying Diode**

The rectifying diode was selected based upon on the peak inverse voltage and the diodes average forward current. The peak inverse voltage across the secondary of the transformer is:

$$
P_{IV} = \frac{V_{in}}{n} + V_{0}
$$

$$
P_{IV} = \frac{400}{6.77} + 19 = 78 V_{pk}
$$

The average current through the diode is:

$$
layg = \frac{Po}{Vo} = \frac{90}{19} = 4.74 A
$$

An MBR20100CT Schottky diode was selected; it is rated for a  $V_{RRM}$  of 100 V, with an average forward current of 10 A.

#### **Power Switch**

A MOSFET was selected as the power switching element. Several factors were used in selecting the MOSFET; current, voltage stress (VDS), and  $R_{DS(on)}$ .

The rms current through the primary of the transformer is the same as the current in the MOSFET, which is 1.45 Arms. The MOSFET selected is manufactured by Infineon, part number SPP11N80C3. It is rated for 800 VDS and 11 Arms, with an  $R_{DS(on)}$  of 0.45  $\Omega$ .

#### **Snubber**

The maximum voltage across the MOSFET is:

$$
Vpk = Vin_{max} + (Vo + Vf)n
$$
  

$$
Vpk = 400 + (19 + 0.7) 6.77 = 534 V
$$

This calculation neglects the voltage spike when the MOSFET turns off due to the transformer leakage inductance. The spike, due to the leakage inductance, must be clamped to a level below the MOSFETs' maximum VDS. To clamp the voltage spike a resistive, capacitive, diode clamp network was used to prevent the drain voltage from rising above Vin + (Vo + Vf) n + Vclamp. The desired clamp voltage is 700 V; this provides a safety margin of 100 V. The first step is to calculate the snubber resistor.

$$
\text{Rclamp} = \frac{2 \cdot \text{Vclamp} \cdot (\text{Vclamp} - \text{Vo} \cdot \text{n})}{\text{le} \cdot \text{lpk}^2 \cdot \text{Freq}}
$$
\n
$$
\text{Rclamp} = \frac{2 \cdot 700 \cdot (700 - (19.7 \cdot 6.77))}{7 \cdot 3.97^2 \cdot 65} = 110 \text{ k}\Omega
$$

Where:

 $Vo$  = the output voltage

 $Vf =$  the forward voltage drop across the output diode n is the transformer turns ratio 6.77

Ie is the transformer turns ratio of  $7 \mu H$ 

The power dissipation in the clamp resistor is:

$$
\text{PRclamp} = 0.5 \cdot \text{lpk}^2 \cdot \text{le} \cdot \text{Freq} \cdot \left( \frac{\text{Vclamp}}{\text{Vclamp} - (\text{Vo} \cdot \text{n})} \right)
$$
\n
$$
\text{PRclamp} = 0.5 \cdot 3.97^2 \cdot 7 \cdot 65 \cdot \left( \frac{700}{700 - (19.7 \cdot 6.77)} \right)
$$
\n
$$
= 4.4 \text{ W}
$$

The snubber capacitor can be calculated from the following equation. See Application Note AN1679/D for details of how the snubber equations were derived.

$$
C6 = \frac{Vclamp}{Vripple \cdot Freq \cdot Rclamp}
$$

$$
C6 = \frac{700}{20 \cdot 65 \cdot 110} = 0.005 \mu F
$$

After the initial snubber was calculated, the snubber values were tuned in the circuit to minimize ringing, and minimize the power dissipation. As a result the final circuit values are; Rclamp uses three 100 k $\Omega$  (33 k $\Omega$  equivalent), 2.0 W resistors used in parallel, and C6 is  $0.01 \mu$ F, 1000 V. Refer to Figure 2 for a scope waveform of the Drain to source voltage at full load and high line.



#### **Current Sense Resistor Selection**

The input to the current sense amplifier is clamped to 1.0 V (typical). The current sense resistor should be calculated at 125% of the full rated load to be sure that under all operating conditions the power supply will be able to deliver the full rated power.

Po = 90 · 1.25 = 112.5 W  
\nPin = 
$$
\frac{Po}{eff}
$$
 =  $\frac{112.5}{0.80}$  = 140.63 W  
\nlpk =  $\sqrt{\frac{2 \cdot 140.63}{220 \cdot 65}}$  = 4.43 Apk  
\nRs =  $\frac{1 V}{lpk}$  =  $\frac{1}{4.43}$  = 0.23 Ω

 $0.2 \Omega$  was used.

To reduce the power dissipation in the sense resistor, two  $0.4 \Omega$  resistors were used in parallel.

#### **Overvoltage Protection**

The NCP1230 has a fast comparator which only monitors the current sense pin during the power switch off time. If the voltage on the current sense pin rises above 3.0 V (typical), the NCP1230 will immediately stop the output drive pulses and latch−off the controller. The NCP1230 will stay in the Latch−Off mode until Vcc has dropped below 4.0 V.

This feature allows the user to implement several protection functions, for example, Overvoltage or Overtemperature Protection.

The Auxiliary winding of the Flyback transformer (T5) can be used for overvoltage protection because the voltage on the Auxiliary winding is proportional to the output voltage.

To implement Overvoltage Protection (OVP), a PNP transistor is used to bias up the current sense pin during the NCP1230 controller off time (refer to Figure 3). The base of the PNP transistor is driven by the NCP1230 drive output (pin 5), if the Auxiliary winding voltage increases above the Zener diode (D1) breakdown voltage, 13 V, current will flow through Q3 biasing up the voltage on the current sense pin. Using typical component values, if the voltage on the Auxiliary winding reaches 16.5 V (3.5 V above the nominal voltage) the NCP1230 will latch−off through the CS input (pin 3).

 $OVP$ threshold =  $Vz(D1) + VceQ3 + CSlatchoff$ 

$$
= 13 V + 0.5 V + 3.0 V = 16.5 V
$$

A 13 V Zener diode was selected to have the controller Latch−Off prior to having Vcc reach its maximum allowable voltage level, 18 V.



**Figure 3. Overvoltage Protection Circuit**

#### **Overtemperature Protection**

To implement Overtemperature Protection (OTP) shutdown, the Zener diode can be replaced by an NTC (refer to Figure 4), or an NTC can be placed in parallel with the Zener diode to have OVP and OTP protection. When an overtemperature condition occurs, the resistance of the NTC will decrease, allowing current to flow through the PNP transistor biasing up the Current Sense pin.



**Figure 4. Overtemperature Protection Circuit**

#### **Slope Compensation**

A Flyback converter operating in continuous conduction mode with a duty cycle greater than 50% requires slope compensation. In this application the power supply will always be operating in the discontinuous mode, so no slope compensation is required.

The resistor R21 and capacitor C24 form a low pass filter suppressing the leading edge of the current signal. Typically, the leading edge of the current will have a large spike due to the transformer leakage inductance. If the spike is not filtered, it can prematurely turn off the MOSFET. The NCP1230 does have a leading edge blanking circuit, but it is a good design practice to add an external filter. The time constant of the filter must be significantly higher than the highest expected operating frequency, but low enough to filter the spike.

#### **Output Control**

Feedback theory states that for the control loop to be stable there must be at least 45° of phase margin when the loop gain crosses cross zero dB. The following equations derive the Flyback converter transfer function while operating in the discontinuous continuous mode.

$$
Po = \frac{Vo^2}{Ro}
$$

Where:

Po is the maximum output power Vo is the output voltage Ro is the output resistance

$$
P = \frac{1}{2} \cdot lpk^2 \cdot Lp \cdot f
$$

Where:

I is the peak primary current Lp is the transformer primary inductance F is the switching frequency of the controller

$$
\frac{Vo^2}{Ro} = \frac{1}{2} \cdot 1pk^2 \cdot Lp \cdot f
$$

$$
\frac{Vo}{i} = \sqrt{\frac{Ro \cdot f \cdot Lp}{2}} \cdot n \cdot d
$$

$$
i = lp \cdot Rs = \frac{Vc}{3}
$$

Where:

Ip is the peak primary current

Rs is the current sense resistor

Vc is the control voltage

3, the feedback input voltage is divided down by a factor of three

Combining equations the open loop gain is:

$$
\frac{V_{0}}{i} = \sqrt{\frac{Ro \cdot Lp \cdot f}{2}} \cdot n \cdot d
$$

$$
i = lpk \cdot Rs = \frac{V_{C}}{3}
$$

$$
\mathsf{Vc} = 3 \cdot \mathsf{Rs} \cdot \mathsf{lpk}
$$

$$
\frac{V_0}{Vc} = \sqrt{\frac{Ro \cdot Lp \cdot f}{2}} \cdot n \cdot d \cdot lpk \cdot Rs \cdot 3
$$

With current mode control, there is pole associated with the output capacitor(s) and the load resistors. In this application there are four  $2200 \mu F$  capacitors in parallel:

$$
fp = \frac{1}{\pi \text{CoRo}} = \frac{1}{\pi \cdot 8800 \cdot 3.9} = 9.3 \text{ Hz}
$$

The secondary filter made up of L1 and C8 does not affect the control loop because we are sensing the output voltage before the LC network.

In addition to the pole, there is a zero associated with the output capacitor(s) and the capacitors esr. The esr of each capacitors is  $0.022 \Omega$  (from the data sheet).

$$
fz = \frac{1}{2\pi\text{Co} \cdot \text{esr}} = \frac{1}{6.28 \cdot 8800 \cdot \frac{0.022}{4}} = 3.3 \text{ kHz}
$$

A small 0.47 nF capacitor (C25) is connected from the feedback pin to ground to reduce the switching noise on the feedback pin. Care must be taken not to have too large a capacitor, or a low frequency pole may be created in the feedback loop.

#### **Output Voltage Regulation**

The output voltage regulation is achieved by using a TL431 on the secondary side of the transformer. The output voltage is sensed and divided down to the reference level of the TL431 (2.5 V typical) by the resistive divider network consisting of R4 and R10.

The TL431 requires a minimum of 1.0 mA of current for regulation:

Ropto(R22) = 
$$
\frac{Vo - Vfopto}{1 mA} = \frac{19 - 1}{1 mA} = 18 k
$$

In this application R22 was changed to 1.0  $k\Omega$  to minimize the stand by power consumption.

When the power supply is operating at no load, there may not be sufficient current through the optocoupler LED, so a resistor (R7) is placed in parallel. A 4.7 k $\Omega$  resistor was selected.

The optocoupler gain is:

$$
\frac{\Delta Vf}{\Delta Vc} = \frac{Rfb \cdot CTR}{Ropto} = \frac{20 \cdot 1.0}{1} = 20
$$

#### dBgain = 20log20 = 26 dB

CTR is the current transfer ratio of the opto and is nominally 1.0, but over time the CTR will degrade so analysis of the circuit with the CTR  $= 0.5$  is recommended.

Rfb is the internal pull−up resistor of the NCP1230 and it is a nominal 20  $k\Omega$ .

#### **Standby Power**

To minimize the standby power consumption, the output voltage sense resistor divider network was select to consume less than 10 mW.

Vref = Vo 
$$
\left(\frac{R10}{R10 + R4}\right)
$$
 = 19  $\left(\frac{7.4}{7.4 + 50}\right)$  = 2.5 V

The Standby power consumption is:

$$
P = \frac{Vo^2}{Rtotal} = \frac{19^2}{57400} = 6.3 \text{ mW}
$$

Standby power calculation:

$$
P_R22 = 12 * R22 = 12 ma \cdot 2 k = 2 mW
$$
  

$$
P_TL431 = (Vo - V_R22 - Vopto) \cdot 1 ma
$$
  

$$
= 17 V \cdot 1 ma = 17 mW
$$

#### **Control Loop**

Two methods were used to verify that the Demo Board loop was stable, the results are shown below. The first method was to use an Excel Spreadsheet (using the previously derived equations) which can be down loaded from the ON Semiconductor website (www.onsemi.com). The results from the Excel Spreadsheet are shown below. At full load and 200 Vdc (200 Vdc is the minimum voltage being supplied from the PFC) the loop gain crosses zero dB at approximately 1.2 kHz with approximately 100° of phase margin.

The second method was to model the NCP1230 Demo Board in PSPICE. The result can be seen in Figure [7.](#page-6-0) Because parasitic elements can be added to the PSPICE model, it was more accurate at high frequencies.

The results from the PSPICE model (at low frequencies) shows similar results, the loop gain crosses zero dB at approximately 1.2 kHz with about 90° of phase margin.



**Figure 5. Excel Spreadsheet Loop Gain**

<span id="page-6-0"></span>







**Figure 8. AC Frequency Response SPICE Model**

#### **Evaluation Board Test Procedure**





#### **Table 2. TEST EQUIPMENT**



#### **Test Setup**

- 1. Connect the ac source to the input terminals J4.
- 2. Connect a variable electronic load to the output terminals J2, the PWB is marked +, for the positive output, and − for the return.
- 3. Set the variable electronic load to 45 W.
- 4. Turn on the ac source and set it to 115 Vac at 60 Hz.
- 5. Verify that the NCP1230 provides 19 Vdc to the load.
- 6. Vary the load and input voltage. Verify that the output voltage is within the minimum and maximum values as shown in Table [4.](#page-8-0)
- 7. To verify total harmonic distortion (THD) first, shut off the ac power supply.
- 8. Connect the Voltec Precision Power Analyzer as shown in Figure 9.
- 9. Turn on the ac source to 115 Vac at 60 Hz and set the electronic load to 90 W. (Only measure the THD at full load).
- 10. Verify that the current Harmonics (THD) are less than the maximum vales in Table 5.
- 11. Verify that the PF is greater than the minimum values in Table 5.
- 12. Set the ac source output to 230 Vac at 60 Hz.
- 13. Verify that the current Harmonics (THD) are less than the maximum vales in Table 5.
- 14. Verify that the PF is greater than the minimum values in Table 5.
- 15. Set the ac source to 115 Vac, set the load to 0 Adc, and measure the standby power, refer to Table [5](#page-8-0) for the maximum acceptable input power.
- 16. Set the ac source to 230 Vac, and refer to Table [5](#page-8-0) for the maximum input power.

### **Table 3. EXPECTED VALUES FOR VARYING INPUT VOLTAGES AND LOADS**



Table 3 shows typical values, the initial set point (19.0 Vdc may vary).

## <span id="page-8-0"></span>**Table 4. REGULATION**



# **Table 5. STAND-BY POWER**



# **Table 6. POWER FACTOR AND THD**



<span id="page-9-0"></span>



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## **Table 7. Voltage Regulation and Efficiency**



### **Table 8. Power Factor and Distortion**



### **Table 9. Standby Power**



# **Table 10. Vendor Contact List**



# <span id="page-12-0"></span>**Table 11. NCP1230 EVALUATION BOARD BILL OF MATERIALS**



# **Table [11.](#page-12-0) NCP1230 EVALUATION BOARD BILL OF MATERIALS**



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