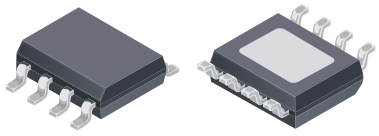
High-Voltage Stepdown Regulator

FEATURES AND BENEFITS

- Wide input voltage range: 8 to 50 V
- Integrated low $R_{DS(on)}$ DMOS switch
- 2 A continuous output current
- Adjustable fixed off-time
- Highly efficient
- Adjustable output: 0.8 to 24 V
- Small package with exposed thermal pad

PACKAGE:

8-pin SOIC with exposed thermal pad (suffix LJ)



Not to scale

DESCRIPTION

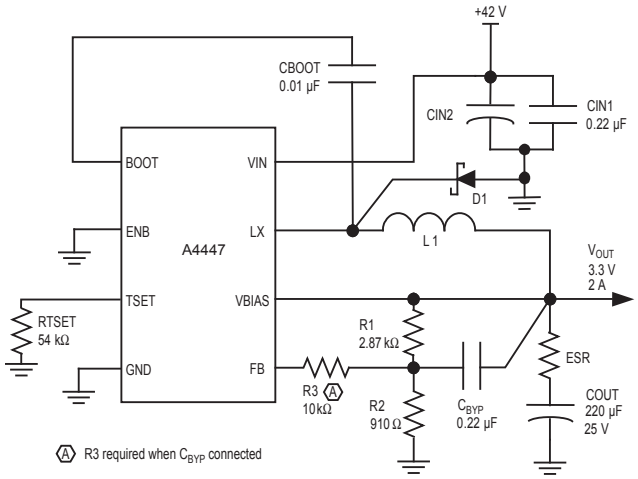
The A4447 is a 2 A, high efficiency general-purpose buck regulator designed for a wide variety of applications. The output voltage is adjustable from 0.8 to 24 V, based on a resistor divider and the 0.8 V ±2% reference. External components include an external clamping diode, inductor, and filter capacitor. The off-time is determined by an external resistor to ground. It operates in both continuous and discontinuous modes to maintain light load regulation. An internal blanking circuit is used to filter out transients due to the reverse recovery of the external clamp diode. Typical blanking time is 200 ns.

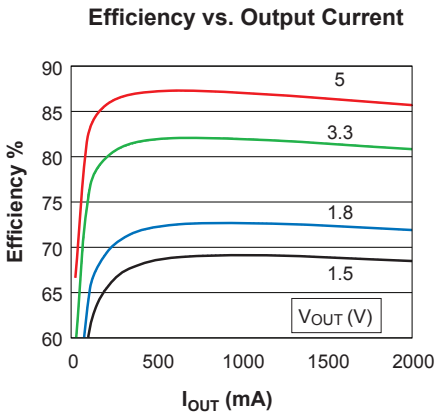
This new device is ideal for various end products including applications with 8 to 50 V input voltage range and require up to 2 A output current, such as uninterruptible power supplies, point of sale (POS) applications, and industrial applications with 24 or 36 V bus.

Applications include:

- Printer power supplies
- Office automation equipment
- POS thermal, laser, photo, and inkjet printers
- Tape drives
- Industrial applications

Typical Application





Data is for reference only. Efficiency data from circuit shown in left panel.

SELECTION GUIDE

Part Number	Packing	Package
A4447SLJTR-T	13-in. reel, 3000 pieces/reel	LJ package, SOIC surface mount with exposed thermal pad; leadframe plating 100% matte tin.

ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Conditions	Min.	Typ.	Max.	Units
VIN Supply Voltage	V_{IN}		–	–	50	V
VBIAS Input Voltage	V_{BIAS}		–0.3	–	7	V
SW Switching Voltage	V_S		–1	–	–	V
ENB Input Voltage Range	V_{ENB}		–0.3	–	7	V
Operating Ambient Temperature Range	T_A		–20	–	85	°C
Junction Temperature	T_J(max)		–	–	150	°C
Storage Temperature	T_{stg}		–55	–	150	°C

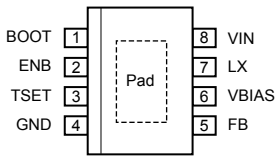
*Output current rating may be limited by duty cycle, ambient temperature, and heat sinking. Under any set of conditions, do not exceed the specified current ratings, or a junction temperature, T_J, of 150°C.

THERMAL CHARACTERISTICS*: May require derating at maximum conditions; see application section for optimization

Characteristic	Symbol	Test Conditions*	Value	Unit
Package Thermal Resistance (Junction to Ambient)	$R_{\theta JA}$	On 4-layer PCB based on JEDEC standard	35	°C/W
		On 2-layer generic test PCB with 0.8 in.^{2} of copper area each side	62	°C/W
Package Thermal Resistance (Junction to Pad)	$R_{\theta JP}$		2	°C/W

*Additional thermal information available on the Allegro™ website.

Pinout Diagram



Terminal List Table

Number	Name	Description
1	BOOT	Gate drive boost node
2	ENB	On/off control; logic input
3	TSET	Off-time setting
4	GND	Ground
5	FB	Feedback for adjustable regulator
6	VBIAS	Bias supply input
7	LX	Buck switching node
8	VIN	Supply input

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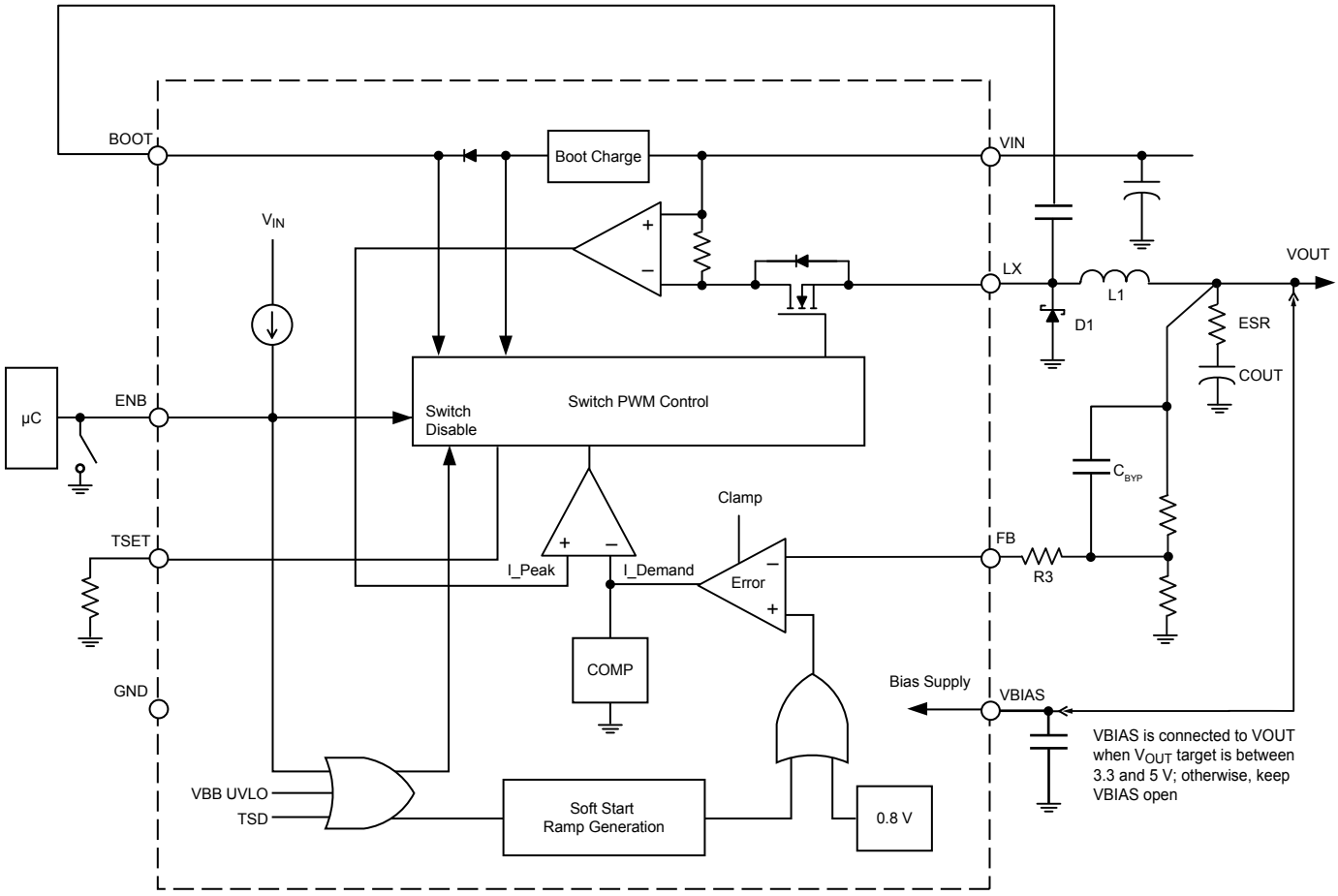
FUNCTIONAL BLOCK DIAGRAM



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ELECTRICAL CHARACTERISTICS [1][2]: Valid at T_A = 25°C, V_{IN} = 8 to 50 V (unless noted otherwise)

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Units
VIN Quiescent Current [3]	$I_{VIN(Q)}$	V_{ENB} = LOW, I_{OUT} = 0 mA, V_{IN} = 42 V, V_{BIAS} = V_{OUT}	–	0.90	1.35	mA
		V_{ENB} = LOW, I_{OUT} = 0 mA, V_{IN} = 42 V, V_{BIAS} < 3 V	–	4.4	6.35	mA
		V_{ENB} = HIGH	–	–	100	µA
VBIAS Input Current	I_{BIAS}	V_{BIAS} = V_{OUT}	–	3.5	5	mA
Buck Switch On Resistance	$R_{DS(on)}$	T_A = 25°C, I_{OUT} = 2 A	–	450	–	mΩ
		T_A = 125°C, I_{OUT} = 2 A	–	650	–	mΩ
Fixed Off-Time Proportion	t_{off}	Based on calculated value	–15	–	15	%
Feedback Voltage	V_{FB}		0.784	0.8	0.816	V
Output Voltage Regulation	V_{OUT}	I_{OUT} = 0 mA to 2 A	–3	–	3	%
Feedback Input Bias Current	I_{FB}		–400	–100	100	nA
Soft Start Time	t_{ss}		5	10	15	ms
Buck Switch Current Limit	I_{CL}	V_{FB} > 0.4 V	2.2	–	3	A
		V_{FB} < 0.4 V	0.5	–	1.2	A
ENB Open Circuit Voltage	V_{OC}	Output disabled	2.0	–	7	V
ENB Input Voltage Threshold	$V_{ENB(0)}$	LOW level input (Logic 0), output enabled	–	–	1.0	V
ENB Input Current	$I_{ENB(0)}$	V_{ENB} = 0 V	–10	–	–1	µA
VIN Undervoltage Threshold	V_{UVLO}	V_{IN} rising	6.6	6.9	7.2	V
VIN Undervoltage Hysteresis	$V_{UVLO(hys)}$	V_{IN} falling	0.7	–	1.1	V
Thermal Shutdown Temperature	T_{JTSD}	Temperature increasing	–	165	–	°C
Thermal Shutdown Hysteresis	$T_{JTSD(hys)}$	Recovery = T_{JTSD} – $T_{JTSD(hys)}$	–	15	–	°C

[1] Negative current is defined as coming out of (sourcing) the specified device pin.
[2] Specifications over the junction temperature range of 0°C to 125°C are assured by design and characterization.
[3] VBIAS is connected to VOUT when the V_{OUT} target is between 3.3 and 5 V.

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FUNCTIONAL DESCRIPTION

The A4447 is a fixed off-time, current mode controlled, buck regulator. The regulator requires an external clamping diode, inductor, and filter capacitor. It operates in both continuous and discontinuous modes. An internal blanking circuit is used to filter out transients resulting from the reverse recovery of the external clamp diode. Typical blanking time is 200 ns.

The value of a resistor between the TSET and GND determines the fixed off-time (see graph in the t_{OFF} section).

V_{OUT}. The output voltage is adjustable from 0.8 to 24 V, set by an external resistor divider. The voltage can be calculated with the following formula:

$$V_{OUT} = V_{FB} \times (1 + R1/R2) \qquad (1)$$

Light Load Regulation. To maintain voltage regulation during light load conditions, the switching regulator enters a cycle-skipping mode. As the output current decreases, there remains some energy that is stored during the power switch minimum on-time. In order to prevent the output voltage from rising, the regulator skips cycles once it reaches the minimum on-time, effectively making the off-time larger.

Soft Start. An internal ramp generator and counter allow the output to slowly ramp up. This limits the maximum demand on the external power supply by controlling the inrush current required to charge the external capacitor and any DC load at startup. Internally, the ramp is set to 10 ms nominal rise time. During soft start, current limit is 2.2 A minimum.

The following conditions are required to trigger a soft start:

- $V_{IN} > 6$ V
- ENB pin input falling edge
- Reset of a TSD (thermal shut down) event

V_{BIAS}. To improve overall system efficiency, the regulator output, V_{OUT}, is connected to the VBIAS input to supply the operating bias current during normal operating conditions. During startup the circuitry is run off of the VIN supply. VBIAS should be connected to VOUT when the V_{OUT} target level is between 3.3 and 5 V. If the output voltage is less than 3.3 V, then the A4447 can operate with an internal supply and pay a penalty in efficiency, as the bias current will come from the high voltage supply, VIN. VBIAS can also be supplied with an external voltage source. No power-up sequencing is required for normal operation.

ON/OFF Control. The ENB pin is externally pulled to ground to enable the device and begin the soft start sequence. When the ENB is open circuited, the switcher is disabled and the output decays to 0 V.

Protection. The buck switch will be disabled under one or more of the following fault conditions:

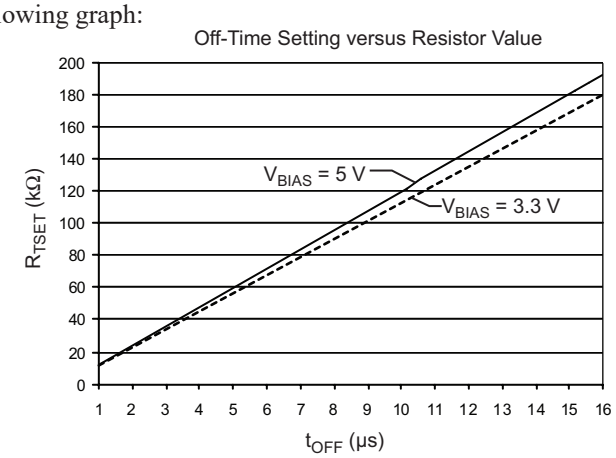
- $V_{IN} < 6$ V
- ENB pin = open circuit
- TSD fault

When the device comes out of a TSD fault, it will go into a soft start to limit inrush current.

t_{OFF}. The value of a resistor between the TSET pin and ground determines the fixed off-time. The formula to calculate t_{OFF} (µs) is:

$$t_{OFF} = R_{TSET}\left(\frac{1 - 0.03 \times V_{BIAS}}{10.2 \times 10^9}\right), \qquad (2)$$

where R_{TSET} (kΩ) is the value of the resistor. If the VBIAS pin is left open, use $V_{BIAS} = 0$ in equation 2. Results are shown in the following graph:



The R_{TSET} resistor should be not smaller than 7.65 kΩ ±2% to prevent very short off-times from violating the minimum on-time of the switcher.

Shorted Load. If the voltage on the FB pin falls below 0.4 V, the regulator will invoke a 0.85 A typical overcurrent limit to handle the shorted load condition at the regulator output. For low output voltages at power up and in the case of a shorted output, the off-time is extended to prevent loss of control of the current limit due to the minimum on-time of the switcher.

The extension of the off-time is based on the value of the TSET multiplier and the FB voltage, as shown in the following table:

V_{FB} (V)	TSET Multiplier
< 0.16	8 × t_{OFF}
< 0.32	4 × t_{OFF}
< 0.5	2 × t_{OFF}
> 0.5	t_{OFF}

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COMPONENT SELECTION

L1. The inductor must be rated to handle the total load current. The value should be chosen to keep the ripple current to a reasonable value. The ripple current, I_{RIPPLE}, can be calculated by:

$$I_{RIPPLE} = V_{L(OFF)} \times t_{OFF} / L \quad (3)$$

$$V_{L(OFF)} = V_{OUT} + V_f + I_{L(AV)} \times R_L \quad (4)$$

Example:

Given V_{OUT} = 5 V, V_f = 0.55 V, V_{IN} = 42 V, I_{LOAD} = 0.5 A, power inductor with L = 180 µH and R_L = 0.5 Ω Rdc at 55°C, t_{OFF} = 7 µs, and $R_{DS(on)}$ = 1 Ω.

Substituting into equation 4:

$$V_{L(OFF)} = 5\ V + 0.55\ V + 0.5\ A \times 0.5\ \Omega = 5.8\ V$$

Substituting into equation 3:

$$I_{RIPPLE} = 5.8\ V \times 7\ \mu s / 180\ \mu H = 225\ mA$$

The switching frequency, f_{SW}, can then be estimated by:

$$f_{SW} = 1 / (t_{ON} + t_{OFF}) \quad (5)$$

$$t_{ON} = I_{RIPPLE} \times L / V_{L(ON)} \quad (6)$$

$$V_{L(ON)} = V_{IN} - I_{L(AV)} \times R_{DS(on)} - I_{L(AV)} \times R_L - V_{OUT} \quad (7)$$

Substituting into equation 7:

$$V_{L(ON)} = 42\ V - 0.5\ A \times 1\ \Omega - 0.5\ A \times 0.5\ \Omega - 5\ V = 36\ V$$

Substituting into equation 6:

$$t_{ON} = 225\ mA \times 180\ \mu H / 36\ V = 1.12\ \mu s$$

Substituting into equation 7:

$$f_{SW} = 1 / (7\ \mu s + 1.12\ \mu s) = 123\ kHz$$

Higher inductor values can be chosen to lower the ripple current. This may be an option if it is required to increase the total maximum current available above that drawn from the switching regulator. The maximum total current available, $I_{LOAD(MAX)}$, is:

$$I_{LOAD(MAX)} = I_{CL}(min) - I_{RIPPLE} / 2 \quad (8)$$

where I_{CL}(min) is 2.2 A, from the Electrical Characteristics table.

D1. The Schottky catch diode should be rated to handle 1.2 times the maximum load current. The voltage rating should be higher than the maximum input voltage expected during all operating conditions. The duty cycle for high input voltages can be very close to 100%.

COUT. The main consideration in selecting an output capacitor is voltage ripple on the output. For electrolytic output capacitors, a low-ESR type is recommended.

The peak-to-peak output voltage ripple is simply I_{RIPPLE} × ESR. Note that increasing the inductor value can decrease the ripple current. The minimum voltage rating of the capacitor is 10 V. However, because ESR decreases with voltage, the most cost-effective choice may be rated higher in voltage. It is recommended that the ESR be less than 100 mΩ.

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RTSET Selection. Correct selection of RTSET values will ensure that minimum on time of the switcher is not violated and prevent the switcher from cycle skipping. For a given V_{IN} to V_{OUT} ratio, R_{TSET} must be greater than or equal to the value defined by the curve in the RTEST Value Selection graph below.

Note. The curve represents the minimum RTSET value. When calculating R_{TSET}, be sure to use V_{IN}(max) / V_{OUT}(min). Resistor tolerance should also be considered, so that under all operating conditions the resistance on the TSET pin remains as close to the curve as possible.

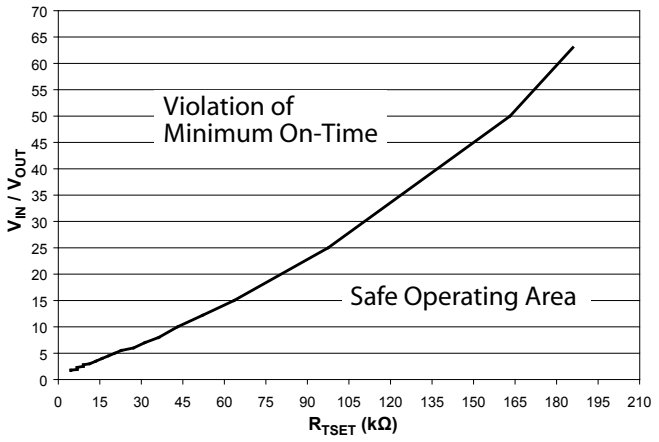
The RTEST Selection table shows recommended R_{TSET} values based on common operating conditions. For other operating conditions, refer to the RTSET Value Selection graph.

CBYP Selection. In certain applications, C_{BYP} can be used to improve closed loop response of the converter. Typically, a 0.22 uF capacitor ensures better loop response for wide range of applications. Resistor R3 prevents negative voltage on the FB pin due to C_{BYP} capacitor during sudden changes in V_{OUT}.

FB Resistor Selection. The impedance of the FB network should be kept low to improve noise immunity. Large value resistors can pick up noise generated by the inductor, which can affect voltage regulation of the switcher.

RTSET Value Selection*

Selection Graph



Recommended Common Values

V_{IN} (V)	V_{OUT} (V)	V_{IN}/V_{OUT}	R_{TSET} Value (kΩ)
42	5	8.4	37.4
42	3.3	12.7	54.9
42	1.8	23.3	90.9
42	1.5	28	105
24	5	4.8	20.0
24	3.3	7.3	32.4
24	1.8	13.3	54.9
24	1.5	16	66.5
12	5	2.4	7.68
12	3.3	3.6	13.7
12	1.8	6.6	30.1
12	1.5	8	37.4

*The R_{TSET} resistor should be not smaller than 7.65 kΩ ±2% to prevent very short off-times from violating the minimum on-time of the switcher.

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RECOMMENDED COMPONENTS

Component	Description			Part Number
L1	Sumida 68 µH			RCH1216BNP-680K
D1	NIEC Schottky Barrier Diode 60 V TO-252AA			NSQ03A06
C_{BYP}	Ceramic X7A 0.22 µF 100 V			Generic
CBOOT	Ceramic X7A 0.01 µF 100 V			Generic
CIN	Electrolytic 100 µF 50 V; must be able to handle worst case ripple curent			Generic
	Ceramic X7A 0.22 µF 50 V			Generic
COUT	United Chemi-Con PXA 220 µF 16 V Low ESR			PXA16VC221MJ12TP
	Rubycon ZL 220 µF 25 V Low ESR (Option 1)			25ZL220M8x11.5
	Panasonic FM 220 µF 25 V Low ESR (Option 2)			EEUFM1E221
	V_{OUT}			
	1.5 V	**1.8 V**	**3.3 V**	**5 V**
R1	1.30 kΩ	2.55 kΩ	2.87 kΩ	6.34 kΩ
R2	1.47 kΩ	2.00 kΩ	0.910 kΩ	1.20 kΩ
R3	10 kΩ			

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RECOMMENDED PCB LAYOUT

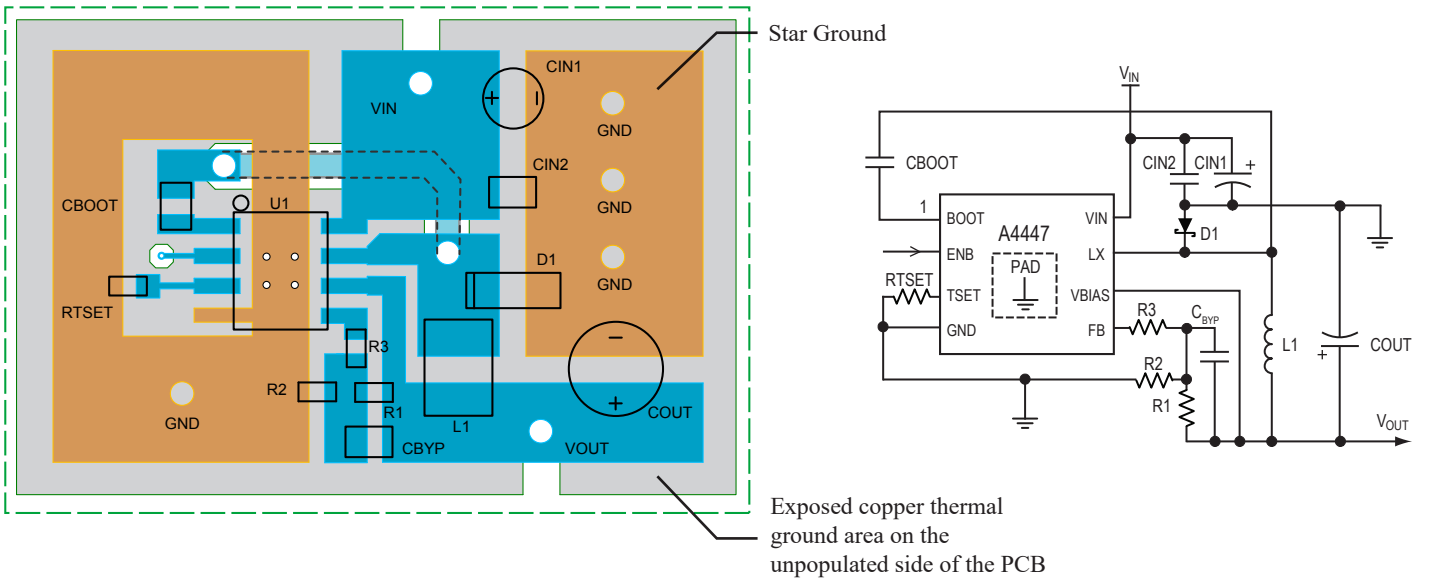
In order to minimize the effects of ground bounce and offset issues, it is important to have a low impedance ground located very close to the device. This grounding scheme is known as star grounding. It is likely that a ground plane will be necessary to meet thermal requirements. The recommended land pattern illustrates how to create a low impedance ground that will also assist with removing thermal energy from the device.

The input capacitor must be placed as close as possible to the VIN terminal because during the on cycle it is responsible for supplying the current to the switcher. During the off cycle, the current path is from the negative terminal of the COUT cap, through the diode and inductor, and then to the load. As a result, COUT and the rectifier diode must share the connection at the negative terminal of the CIN capacitor in order to reduce ground bounce when the diode is conducting.

The inductor should be connected as close as possible to the switching node to minimize noise. Some applications may require a shielded inductor due to EMI restrictions. This will depend on the application and parameters defined by the system that will host the regulator.

The high voltage-switching node could affect R_{TSET}. If longer off-times are used, the resistance on the RTSET pin can be quite large. When designing the layout, try to keep RTSET away from the inductor and switching node. It is also beneficial to keep the trace as short as possible to reduce the effect of noise injection. Because of this layout guideline, the TSET pin is located on the other side of the device, away from the switching node.

The FB resistor network should have a lower impedance to avoid interference from the switching node. Because the impedance on the FB node can be controlled, it is not as critical to keep the network isolated. It is important to keep the ground trace short so that ground bounce cannot effect the output voltage regulation.



The large star ground area on the populated side of the PCB, shown in the diagram as the GND nodes, supports high current throughput, and allows the VOUT node to be located as close as practical to the A4447 (U1). Thermal conduction from the A4447 is enhanced by direct contact of its exposed thermal pad to the smaller ground area under the A4447. This area is connected by thermal vias to the large copper ground plane on the unpopulated side of the PCB.

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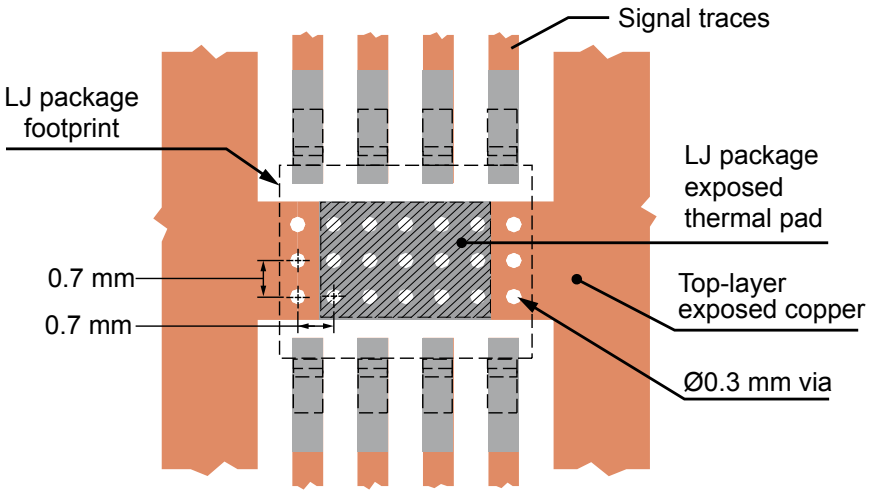
OPTIMIZING THERMAL LAYOUT

The features of the printed circuit board, including heat conduction and adjacent thermal sources such as other components, have a very significant effect on the thermal performance of the device. To optimize thermal performance, the following should be taken into account:

- The device exposed thermal pad should be connected to as much copper area as is available.
- Copper thickness should be as high as possible (for example, 2 oz. or greater for higher power applications).
- The greater the quantity of thermal vias, the better the dissipation. If the expense of vias is a concern, studies have shown that concentrating the vias directly under the device in a tight pattern, as shown in figure 6, has the greatest effect.
- Additional exposed copper area on the opposite side of the board should be connected by means of the thermal vias. The copper should cover as much area as possible.
- Other thermal sources should be placed as remote from the device as possible



Suggested PCB layout for thermal optimization (maximum available bottom-layer copper recommended)

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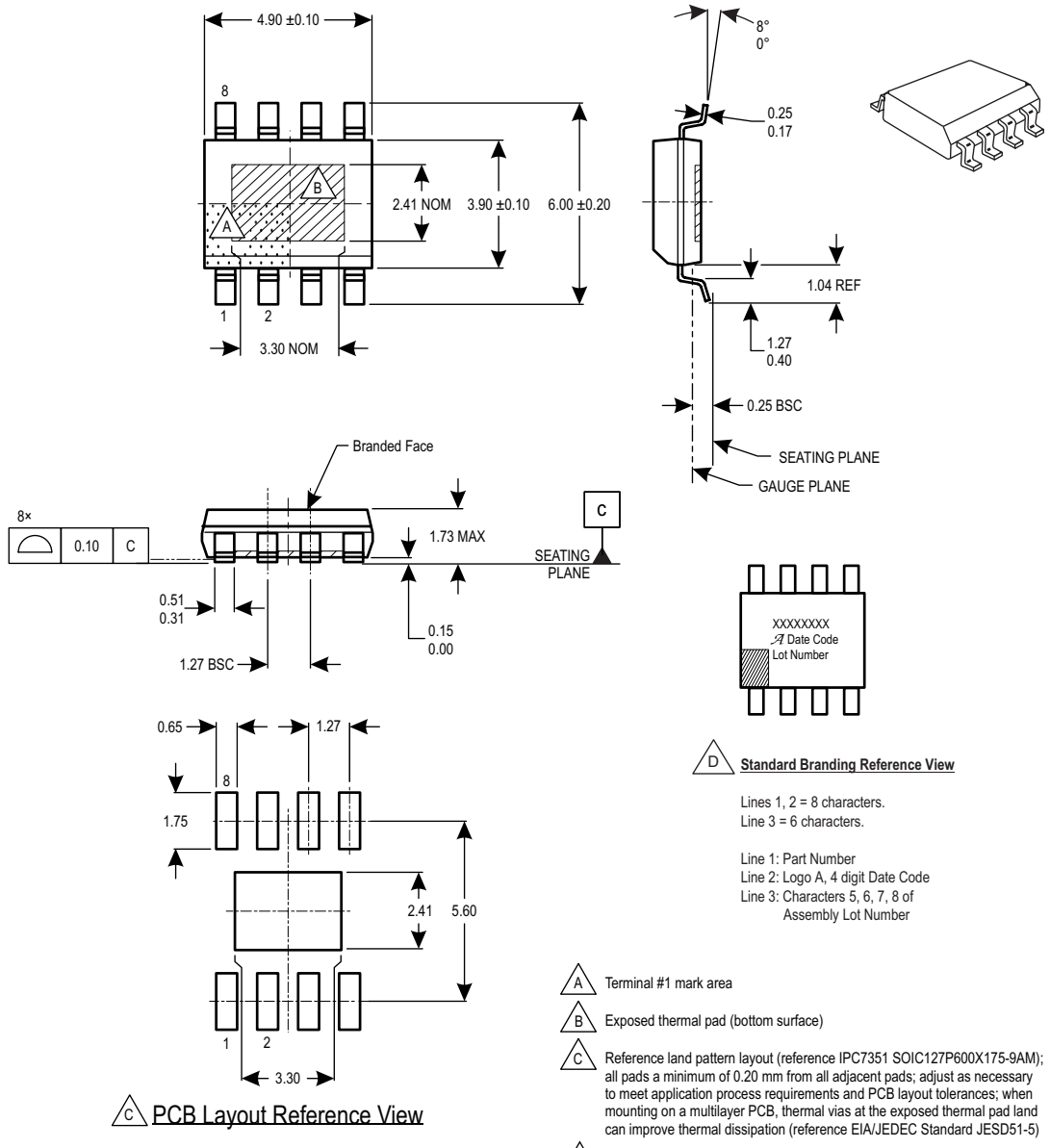
Package LJ, 8 Pin SOIC

For Reference Only – Not for Tooling Use

(Reference Allegro DWG-0000380, Rev. 2 and JEDEC MS-012BA)
Dimensions in millimeters – NOT TO SCALE
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown



C PCB Layout Reference View

D **Standard Branding Reference View**

Lines 1, 2 = 8 characters.
Line 3 = 6 characters.

Line 1: Part Number
Line 2: Logo A, 4 digit Date Code
Line 3: Characters 5, 6, 7, 8 of
Assembly Lot Number

A Terminal #1 mark area

B Exposed thermal pad (bottom surface)

C Reference land pattern layout (reference IPC7351 SOIC127P600X175-9AM); all pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

D Branding scale and appearance at supplier discretion

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Revision History

Number	Date	Description
2	March 19, 2013	Add component recommendations
3	December 20, 2019	Minor editorial updates
4	January 6, 2022	Updated package drawing (page 11) and minor editorial updates

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