14-Bit, 1.25 GSPS JESD204B, Dual Analog-to-Digital Converter

FEATURES

- JESD204B (Subclass 1) coded serial digital outputs
- 1.9 W total power per channel (default settings)
- SFDR = 77 dBFS at 340 MHz
- SNR = 63.4 dBFS at 340 MHz (A_{IN} = −1.0 dBFS)
- Noise density = −152.6 dBFS/Hz
- 1.25 V, 2.50 V, and 3.3 V dc supply operation
- No missing codes
- 1.58 V p-p differential full scale input voltage
- Flexible termination impedance
  - 400 Ω, 200 Ω, 100 Ω, and 50 Ω differential
- 1.5 GHz usable analog input full power bandwidth
- 95 dB channel isolation/crosstalk
- Amplitude detection bits for efficient AGC implementation
- 2 integrated wideband digital processors per channel
  - 12-bit NCO, up to 4 cascaded half-band filters
- Integer clock divide by 1, 2, 4, or 8
- Flexible JESD204B lane configurations
- Timestamp feature
- Small signal dither

APPLICATIONS

- Communications (wideband receivers and digital predistortion)
- Instrumentation (spectrum analyzers, network analyzers, integrated RF test solutions)
- DOCSIS 3.x CMTS upstream receive paths
- High speed data acquisition systems

GENERAL DESCRIPTION

The AD9691 is a dual, 14-bit, 1.25 GSPS analog-to-digital converter (ADC). The device has an on-chip buffer and sample-and-hold circuit designed for low power, small size, and ease of use. The device is designed for sampling wide bandwidth analog signals of up to 1.5 GHz.

The dual ADC cores feature a multistage, differential pipelined architecture with integrated output error correction logic. Each ADC features wide bandwidth inputs supporting a variety of user-selectable input ranges. An integrated voltage reference eases design considerations.

Each ADC data output is internally connected to two digital downconverters (DDCs). Each DDC consists of four cascaded signal processing stages: a 12-bit frequency translator (NCO) and four half-band decimation filters.

In addition to the DDC blocks, the AD9691 has a programmable threshold detector that allows monitoring of the incoming signal power using the fast detect output bits of the ADC. Because this threshold indicator has low latency, the user can quickly turn down the system gain to avoid an overrange condition at the ADC input.

Users can configure the Subclass 1 JESD204B-based high speed serialized output in a variety of one-, two-, four- or eight-lane configurations, depending on the DDC configuration and the acceptable lane rate of the receiving logic device. Multiple device synchronization is supported through the SYSREF± input pins.

The AD9691 is available in a Pb-free, 88-lead LFCSP and is specified over the −40°C to +85°C industrial temperature range. This product is protected by a U.S. patent.

PRODUCT HIGHLIGHTS

1. Low power consumption analog core, 14-bit, 1.25 GSPS dual ADC with 1.9 W per channel.
2. Wide full power bandwidth supports intermediate frequency (IF) sampling of signals up to 1.5 GHz.
3. Buffered inputs with programmable input termination eases filter design and implementation.
4. Flexible serial port interface (SPI) controls various product features and functions to meet specific system requirements.
5. Programmable fast overrange detection.
6. 12 mm × 12 mm, 88-lead LFCSP.

Rev. A

DOCUMENT FEEDBACK
TECHNICAL SUPPORT

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REVISION HISTORY

12/2023—Rev. 0 to Rev. A

Updated Outline Dimensions ... 74
Changes to Ordering Guide ... 74

7/2015—Revision 0: Initial Version

FUNCTIONAL BLOCK DIAGRAM

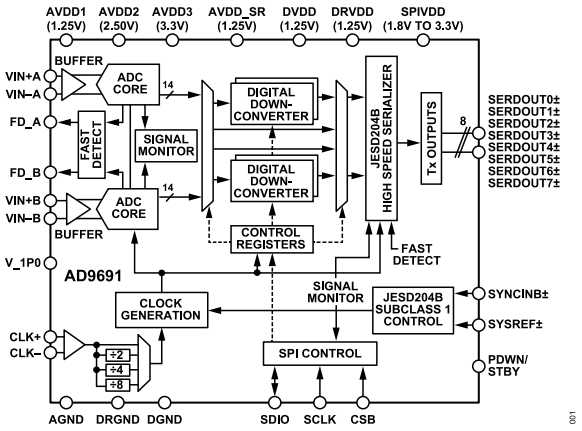

Figure 1.

SPECIFICATIONS

DC SPECIFICATIONS

AVDD1 = 1.25 V, AVDD2 = 2.50 V, AVDD3 = 3.3 V, AVDD1_SR = 1.25 V, DVDD = 1.25 V, DRVDD = 1.25 V, SPIVDD = 1.8 V, specified maximum sampling rate (1250 MSPS), 1.58 V p-p full-scale differential input, A_{IN} = −1.0 dBFS, clock divider = 2, default SPI settings, T_A = 25°C, unless otherwise noted.

Table 1.

Parameter	Temperature	Min	Typ	Max	Unit
RESOLUTION	Full	14			Bits
ACCURACY					
No Missing Codes	Full		Guaranteed		
Offset Error	Full	−0.31	0	+0.31	% FSR
Offset Matching	Full		0	0.3	% FSR
Gain Error	Full	−6	0	+6	% FSR
Gain Matching	Full		1	3.9	% FSR
Differential Nonlinearity (DNL)	Full	−0.8	±0.5	+0.8	LSB
Integral Nonlinearity (INL)	Full	−6.5	±2.6	+6.5	LSB
TEMPERATURE DRIFT					
Offset Error	25°C		−26		ppm/°C
Gain Error	25°C		±9.8		ppm/°C
INTERNAL VOLTAGE REFERENCE					
Voltage	Full		1.0		V
INPUT REFERRED NOISE					
V_{REF} = 1.0 V	25°C		3.53		LSB rms
ANALOG INPUTS					
Differential Input Voltage Range	Full		1.58		V p-p
Common-Mode Voltage (V_{CM})	25°C		2.05		V
Differential Input Capacitance	25°C		1.5		pF
Analog Input Full Power Bandwidth	25°C		2		GHz
POWER SUPPLY					
AVDD1	Full	1.22	1.25	1.28	V
AVDD2	Full	2.44	2.50	2.56	V
AVDD3	Full	3.2	3.3	3.4	V
AVDD1_SR	Full	1.22	1.25	1.28	V
DVDD	Full	1.22	1.25	1.28	V
DRVDD	Full	1.22	1.25	1.28	V
SPIVDD	Full	1.7	1.8	3.4	V
I_{AVDD1}	Full		800	840	mA
I_{AVDD2}	Full		670	770	mA
I_{AVDD3}	Full		125	140	mA
I_{AVDD1_SR}	Full		15	18	mA
I_{DVDD}[1]	Full		250	290	mA
I_{DRVDD}[2]	Full		310	380	mA
I_{SPIVDD}	Full		5	6	mA
POWER CONSUMPTION					
Total Power Dissipation (Including Output Drivers)[1]	Full		3.8		W
Power-Down Dissipation	Full		0.9		mW
Standby[3]	Full		1.5		W

[1] Default mode. No DDCs used. L = 8, M = 2, and F = 1.

SPECIFICATIONS

[2] All lanes running. Power dissipation on DRVDD changes with the lane rate and number of lanes used.

[3] Standby mode can be controlled by the SPI.

AC SPECIFICATIONS

AVDD1 = 1.25 V, AVDD2 = 2.50 V, AVDD3 = 3.3 V, AVDD1_SR = 1.25 V, DVDD = 1.25 V, DRVDD = 1.25 V, SPIVDD = 1.8 V, specified maximum sampling rate (1250 MSPS), 1.58 V p-p full-scale differential input, A_{IN} = −1.0 dBFS, clock divider = 2, default SPI settings, T_A = 25°C, unless otherwise noted.

Table 2.

Parameter[1]	Temperature	Min	Typ	Max	Unit
ANALOG INPUT FULL SCALE	Full		1.58		V p-p
NOISE DENSITY[2]	Full		−152.6		dBFS/Hz
SIGNAL-TO-NOISE RATIO (SNR)[3]					
f_{IN} = 10 MHz	25°C		64.6		dBFS
f_{IN} = 170 MHz	Full	60.8	64.2		dBFS
f_{IN} = 340 MHz	25°C		63.4		dBFS
f_{IN} = 450 MHz	25°C		62.9		dBFS
f_{IN} = 750 MHz	25°C		61.7		dBFS
f_{IN} = 985 MHz	25°C		59.7		dBFS
f_{IN} = 1205 MHz	25°C		58.3		dBFS
f_{IN} = 1600 MHz	25°C		56.5		dBFS
f_{IN} = 1950 MHz	25°C		55.1		dBFS
SNR AND DISTORTION RATIO (SINAD)[3]					
f_{IN} = 10 MHz	25°C		64.5		dBFS
f_{IN} = 170 MHz	Full	60.5	64.0		dBFS
f_{IN} = 340 MHz	25°C		63.0		dBFS
f_{IN} = 450 MHz	25°C		62.3		dBFS
f_{IN} = 750 MHz	25°C		61.3		dBFS
f_{IN} = 985 MHz	25°C		59.4		dBFS
f_{IN} = 1205 MHz	25°C		57.5		dBFS
f_{IN} = 1600 MHz	25°C		55.8		dBFS
f_{IN} = 1950 MHz	25°C		54.7		dBFS
EFFECTIVE NUMBER OF BITS (ENOB)					
f_{IN} = 10 MHz	25°C		10.4		Bits
f_{IN} = 170 MHz	Full	9.7	10.3		Bits
f_{IN} = 340 MHz	25°C		10.2		Bits
f_{IN} = 450 MHz	25°C		10.1		Bits
f_{IN} = 750 MHz	25°C		9.9		Bits
f_{IN} = 985 MHz	25°C		9.6		Bits
f_{IN} = 1205 MHz	25°C		9.2		Bits
f_{IN} = 1600 MHz	25°C		9.0		Bits
f_{IN} = 1950 MHz	25°C		8.8		Bits
SPURIOUS-FREE DYNAMIC RANGE (SFDR)[3]					
f_{IN} = 10 MHz	25°C		87		dBFS
f_{IN} = 170 MHz	Full	72	79		dBFS
f_{IN} = 340 MHz	25°C		77		dBFS
f_{IN} = 450 MHz	25°C		72		dBFS
f_{IN} = 750 MHz	25°C		73		dBFS
f_{IN} = 985 MHz	25°C		72		dBFS
f_{IN} = 1205 MHz	25°C		66		dBFS

SPECIFICATIONS

Table 2. (Continued)

Parameter[1]	Temperature	Min	Typ	Max	Unit
f_{IN} = 1600 MHz	25°C		66		dBFS
f_{IN} = 1950 MHz	25°C		69		dBFS
WORST HARMONIC, SECOND OR THIRD[3]					
f_{IN} = 10 MHz	25°C		−87		dBFS
f_{IN} = 170 MHz	Full		−84	−72	dBFS
f_{IN} = 340 MHz	25°C		−77		dBFS
f_{IN} = 450 MHz	25°C		−72		dBFS
f_{IN} = 750 MHz	25°C		−73		dBFS
f_{IN} = 985 MHz	25°C		−72		dBFS
f_{IN} = 1205 MHz	25°C		−66		dBFS
f_{IN} = 1600 MHz	25°C		−66		dBFS
f_{IN} = 1950 MHz	25°C		−69		dBFS
WORST OTHER, EXCLUDING SECOND OR THIRD HARMONIC[3]					
f_{IN} = 10 MHz	25°C		−93		dBFS
f_{IN} = 170 MHz	Full		−81	−76	dBFS
f_{IN} = 340 MHz	25°C		−79		dBFS
f_{IN} = 450 MHz	25°C		−81		dBFS
f_{IN} = 750 MHz	25°C		−77		dBFS
f_{IN} = 985 MHz	25°C		−76		dBFS
f_{IN} = 1205 MHz	25°C		−72		dBFS
f_{IN} = 1600 MHz	25°C		−72		dBFS
f_{IN} = 1950 MHz	25°C		−73		dBFS
TWO-TONE INTERMODULATION DISTORTION (IMD), A_{IN1} AND A_{IN2} = −7 dBFS					
f_{IN1} = 185 MHz, f_{IN2} = 188 MHz, Buffer Current Setting = 3.5×	25°C		82		dBFS
f_{IN1} = 449 MHz, f_{IN2} = 452 MHz, Buffer Current Setting = 6.5×	25°C		78		dBFS
CHANNEL ISOLATION/CROSSTALK[4]	25°C		95		dB
FULL POWER BANDWIDTH[5]	25°C		1.5		GHz

1 See the AN-835 Application Note, Understanding *High Speed ADC Testing and Evaluation*, for definitions and for details on how these tests were completed.

2 Noise density is measured at a low analog input frequency (30 MHz).

3 See Table 10 for the recommended settings for full-scale voltage and buffer current control.

4 Crosstalk is measured at 170 MHz with a −1.0 dBFS analog input on one channel and no input on the adjacent channel.

5 Measured with the circuit shown in Figure 41.

DIGITAL SPECIFICATIONS

AVDD1 = 1.25 V, AVDD2 = 2.50 V, AVDD3 = 3.3 V, AVDD1_SR = 1.25 V, DVDD = 1.25 V, DRVDD = 1.25 V, SPIVDD = 1.8 V, specified maximum sampling rate (1250 MSPS), 1.58 V p-p full-scale differential input, A_{IN} = −1.0 dBFS, clock divider = 2, default SPI settings, T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Temperature	Min	Typ	Max	Unit
CLOCK INPUTS (CLK+, CLK−)					
Logic Compliance	Full		LVDS/LVPECL		
Differential Input Voltage	Full	600	1200	1800	mV p-p
Input Common-Mode Voltage	Full		0.85		V
Input Resistance (Differential)	Full		35		kΩ
Input Capacitance	Full			2.5	pF

SPECIFICATIONS

Table 3. (Continued)

Parameter	Temperature	Min	Typ	Max	Unit
SYSTEM REFERENCE INPUTS (SYSREF+, SYSREF−)					
Logic Compliance	Full		LVDS/LVPECL		
Differential Input Voltage	Full	400	1200	1800	mV p-p
Input Common-Mode Voltage	Full	0.6	0.85	2.0	V
Input Resistance (Differential)	Full		35		kΩ
Input Capacitance (Differential)	Full			2.5	pF
LOGIC INPUTS (SDIO, SCLK, CSB, PDWN/STBY)					
Logic Compliance	Full		CMOS		
Logic 1 Voltage	Full	0.8 × SPIVDD			V
Logic 0 Voltage	Full	0		0.5	V
Input Resistance	Full		30		kΩ
LOGIC OUTPUT (SDIO)					
Logic Compliance	Full		CMOS		
Logic 1 Voltage (I_{OH} = 800 µA)	Full	0.8 × SPIVDD			V
Logic 0 Voltage (I_{OL} = 50 µA)	Full	0		0.5	V
SYNC INPUTS (SYNCINB+, SYNCINB−)					
Logic Compliance	Full		LVDS/LVPECL/CMOS		
Differential Input Voltage	Full	400	1200	1800	mV p-p
Input Common-Mode Voltage	Full	0.6	0.85	2.0	V
Input Resistance (Differential)	Full		35		kΩ
Input Capacitance	Full			2.5	pF
LOGIC OUTPUTS (FD_A, FD_B)					
Logic Compliance	Full		CMOS		
Logic 1 Voltage	Full	0.8 × SPIVDD			V
Logic 0 Voltage	Full	0		0.5	V
Input Resistance	Full		30		kΩ
DIGITAL OUTPUTS (SERDOUTx±, x = 0 TO 7)					
Logic Compliance	Full		CML		
Differential Output Voltage	Full	360		770	mV p-p
Output Common-Mode Voltage (V_{CM}), AC-Coupled	25°C	0		1.8	V
Short-Circuit Current (I_{DSHORT})	25°C	−100		+100	mA
Differential Return Loss (RL_{DIFF})[1]	25°C	8			dB
Common-Mode Return Loss (RL_{CM})[1]	25°C	6			dB
Differential Termination Impedance	Full	80	100	120	Ω

[1] Differential and common-mode return loss is measured from 100 MHz to 0.75 MHz × baud rate.

SWITCHING SPECIFICATIONS

AVDD1 = 1.25 V, AVDD2 = 2.50 V, AVDD3 = 3.3 V, AVDD1_SR = 1.25 V, DVDD = 1.25 V, DRVDD = 1.25 V, SPIVDD = 1.8 V, specified maximum sampling rate (1250 MSPS), 1.58 V p-p full-scale differential input, A_{IN} = −1.0 dBFS, clock divider = 2, default SPI settings, T_A = 25°C, unless otherwise noted.

Table 4.

Parameter	Temperature	Min	Typ	Max	Unit
CLOCK					
Clock Rate (at CLK+/CLK− Pins)	Full	0.3		4	GHz
Maximum Sample Rate[1]	Full	1250			MSPS
Minimum Sample Rate[2]	Full	300			MSPS

SPECIFICATIONS

Table 4. (Continued)

Parameter	Temperature	Min	Typ	Max	Unit
Clock Pulse Width					
High	Full	400			ps
Low	Full	400			ps
OUTPUT PARAMETERS					
Unit Interval (UI)[3]	Full	320	160		ps
Rise Time (t_R) (20% to 80% into 100 Ω Load)	25°C	24	32		ps
Fall Time (t_F) (20% to 80% into 100 Ω Load)	25°C	24	32		ps
PLL Lock Time	25°C		2		ms
Data Rate per Channel (NRZ)[4]	25°C	3.125	6.25	12.5	Gbps
LATENCY[5]					
Pipeline Latency	Full		55		Clock cycles
Fast Detect Latency	Full			28	Clock cycles
Wake-Up Time[6]					
Standby	25°C		1		ms
Power-Down	25°C			4	ms
APERTURE					
Aperture Delay (t_A)	Full		530		ps
Aperture Uncertainty (Jitter, t_j)	Full		55		fs rms
Out-of-Range Recovery Time	Full		1		Clock cycles

1 The maximum sample rate is the clock rate after the divider.

2 The minimum sample rate operates at 300 MSPS with L = 1.

3 Baud rate = 1/UI. A subset of this range is supported by the AD9691.

4 Default L = 8. This number can be changed based on the sample rate and decimation ratio.

5 No DDCs used. L = 8, M = 2, and F = 1.

6 Wake-up time is the time required to return to normal operation from power-down mode.

TIMING SPECIFICATIONS

Table 5.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
CLK+ to SYSREF+ TIMING REQUIREMENTS	See Figure 2				
t_{SU_SR}	Device clock to SYSREF+ setup time		117		ps
t_{H_SR}	Device clock to SYSREF+ hold time		−96		ps
SPI TIMING REQUIREMENTS	See Figure 3				
t_{DS}	Setup time between the data and the rising edge of SCLK	2			ns
t_{DH}	Hold time between the data and the rising edge of SCLK	2			ns
t_{CLK}	Period of the SCLK signal	40			ns
t_S	Setup time between CSB and SCLK	2			ns
t_H	Hold time between CSB and SCLK	2			ns
t_{HIGH}	Minimum period that SCLK must be in a logic high state	10			ns
t_{LOW}	Minimum period that SCLK must be in a logic low state	10			ns
t_{EN_SDIO}	Time required for the SDIO pin to switch from an input to an output relative to the SCLK falling edge (not shown in Figure 3)	10			ns
t_{DIS_SDIO}	Time required for the SDIO pin to switch from an output to an input relative to the SCLK rising edge (not shown in Figure 3)	10			ns

SPECIFICATIONS

Timing Diagrams

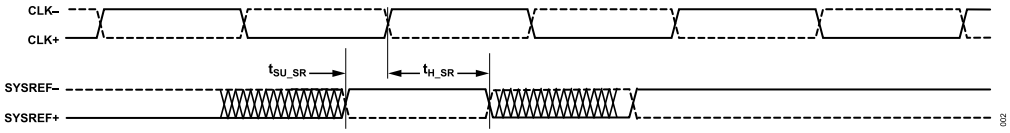

Figure 2. SYSREF+ Setup and Hold Timing Diagram

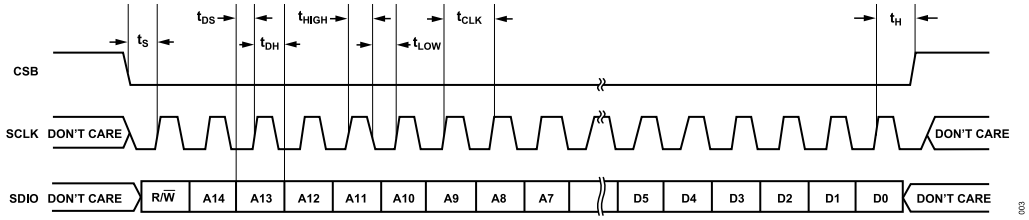

Figure 3. SPI Timing Diagram

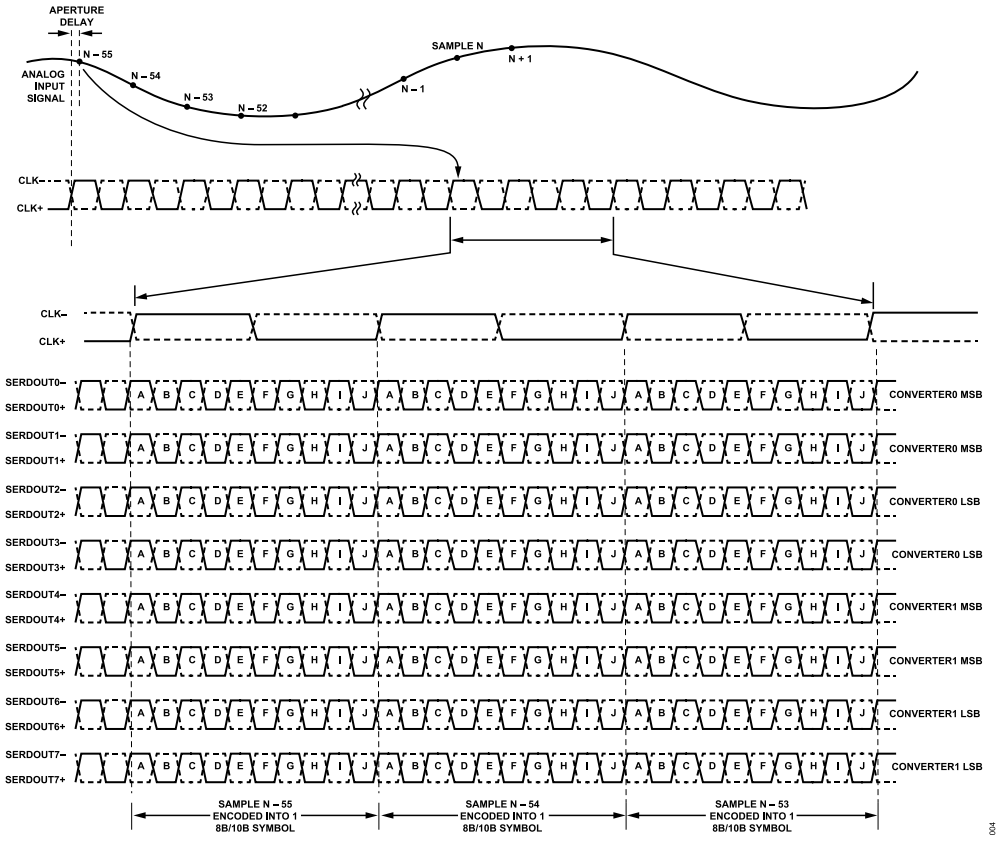

Figure 4. Data Output Timing (Full Bandwidth Mode, L = 8, M = 2, F = 1)

ABSOLUTE MAXIMUM RATINGS

Table 6.

Parameter	Rating
Electrical	
AVDD1 to AGND	1.32 V
AVDD1_SR to AGND	1.32 V
AVDD2 to AGND	2.75 V
AVDD3 to AGND	3.63 V
DVDD to DGND	1.32 V
DRVDD to DRGND	1.32 V
SPIVDD to AGND	3.63 V
AGND to DRGND	−0.3 V to +0.3 V
VIN±x to AGND	3.2 V
SCLK, SDIO, CSB to AGND	−0.3 V to SPIVDD + 0.3 V
PDWN/STBY to AGND	−0.3 V to SPIVDD + 0.3 V
Environmental	
Operating Temperature Range	−40°C to +85°C
Maximum Junction Temperature	115°C
Storage Temperature Range (Ambient)	−65°C to +150°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL CHARACTERISTICS

Typical θ_{JA}, Ψ_{JB}, θ_{JC_TOP}, and θ_{JC_BOT} values are specified vs. the number of printed circuit board (PCB) layers in different airflow velocities (in m/sec). Airflow increases heat dissipation effectively reducing θ_{JA} and Ψ_{JB}. The use of appropriate thermal management techniques is recommended to ensure that the maximum junction temperature does not exceed the limits shown in Table 7.

Table 7.

PCB Type	Airflow Velocity (m/sec)	θ_{JA}[1, 2]	Ψ_{JB}[1, 3]	θ_{JC_TOP}[1, 4]	θ_{JC_BOT}[1, 4]	Unit
JEDEC2s 2p Board	0.0	17.41	4.70	6.01	1.12	°C/W
	1.0	13.83	4.32	N/A[5]	N/A[5]	°C/W
	2.5	12.47	4.21	N/A[5]	N/A[5]	°C/W

1 Per JEDEC 51-7, plus JEDEC 51-5 2s2p test board.

2 Per JEDEC JESD51-2 (still air) or JEDEC JESD51-6 (moving air).

3 Per JEDEC JESD51-8 (still air).

4 Per MIL-STD 883, Method 1012.1.

5 N/A means not applicable.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

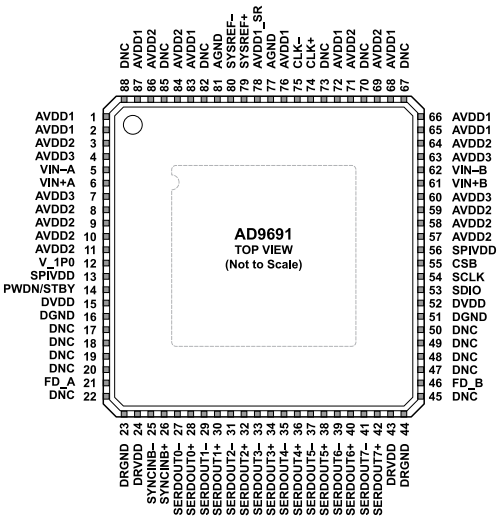

Figure 5. Pin Configuration

Table 8. Pin Function Descriptions

Pin No.	Mnemonic	Type	Description
Power Supplies			
0	EPAD	Ground	Exposed Pad. The exposed thermal pad on the bottom of the package provides the ground reference for AVDDx. The exposed thermal pad must be connected to AGND.
1, 2, 65, 66, 68, 72, 76, 83, 87	AVDD1	Supply	Analog Power Supply (1.25 V Nominal).
3, 8, 9, 10, 11, 57, 58, 59, 64, 69, 71, 84, 86	AVDD2	Supply	Analog Power Supply (2.50 V Nominal).
4, 7, 60, 63	AVDD3	Supply	Analog Power Supply (3.3 V Nominal).
13, 56	SPIVDD	Supply	Digital Power Supply for SPI (1.8 V to 3.3 V).
15, 52	DVDD	Supply	Digital Power Supply (1.25 V Nominal).
16, 51	DGND	Ground	Ground Reference for DVDD.
23, 44	DRGND	Ground	Ground Reference for DRVDD.
24, 43	DRVDD	Supply	Digital Driver Power Supply (1.25 V Nominal).
77, 81	AGND[1]	Ground	Ground Reference for SYSREF±.
78	AVDD1_SR[1]	Supply	Analog Power Supply for SYSREF± (1.25 V Nominal).
Analog			
5, 6	VIN−A, VIN+A	Input	ADC A Analog Input Complement/True.
12	V_1P0	Input/DNC	1.0 V Reference Voltage Input/Do Not Connect. This pin is configurable through the SPI as a no connect or as an input. Do not connect this pin if using the internal reference. This pin requires a 1.0 V reference voltage input if using an external voltage reference source.
61, 62	VIN+B, VIN−B	Input	ADC B Analog Input True/Complement.
74, 75	CLK+, CLK−	Input	Clock Input True/Complement.
CMOS Outputs			
21, 46	FD_A, FD_B	Output	Fast Detect Outputs for Channel A and Channel B, respectively.
Digital Inputs			
25, 26	SYNCINB−, SYNCINB+	Input	Active Low JESD204B LVDS Sync Input Complement/True.
79, 80	SYSREF+, SYSREF−	Input	Active Low JESD204B LVDS System Reference Input True/Complement.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

Table 8. Pin Function Descriptions (Continued)

Pin No.	Mnemonic	Type	Description
Data Outputs			
27, 28	SERDOUT0−, SERDOUT0+	Output	Lane 0 Output Data Complement/True.
29, 30	SERDOUT1−, SERDOUT1+	Output	Lane 1 Output Data Complement/True.
31, 32	SERDOUT2−, SERDOUT2+	Output	Lane 2 Output Data Complement/True.
33, 34	SERDOUT3−, SERDOUT3+	Output	Lane 3 Output Data Complement/True.
35, 36	SERDOUT4−, SERDOUT4+	Output	Lane 4 Output Data Complement/True.
37, 38	SERDOUT5−, SERDOUT5+	Output	Lane 5 Output Data Complement/True.
39, 40	SERDOUT6−, SERDOUT6+	Output	Lane 6 Output Data Complement/True.
41, 42	SERDOUT7−, SERDOUT7+	Output	Lane 7 Output Data Complement/True.
Device Under Test (DUT) Controls			
14	PDWN/STBY	Input	Power-Down Input (Active High). The operation of this pin depends on the SPI mode and can be configured as power-down or standby.
53	SDIO	Input/output	SPI Serial Data Input/Output.
54	SCLK	Input	SPI Serial Clock.
55	CSB	Input	SPI Chip Select (Active Low).
No Connections			
17, 18, 19, 20, 22, 45, 47, 48, 49, 50, 67, 70, 73, 82, 85, 88	DNC		Do No Connect. These pins must be left unconnected.

[1] To ensure proper ADC operation, connect AVDD1_SR and AGND separately from the AVDD1 and EPAD connection. For more information, see the Applications Information section.

TYPICAL PERFORMANCE CHARACTERISTICS

AVDD1 = 1.25 V, AVDD1_SR = 1.25 V, AVDD2 = 2.50 V, AVDD3 = 3.3 V, DVDD = 1.25 V, DRVDD = 1.25 V, SPIVDD = 1.8 V, specified maximum sampling rate (1250 MSPS), 1.58 V p-p full-scale differential input, A_{IN} = −1.0 dBFS, default SPI settings, clock divider = 2, T_A = 25°C, 128k FFT sample, unless otherwise noted.

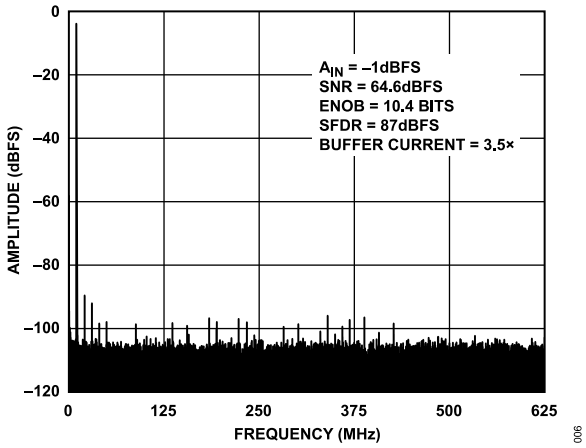

Figure 6. Single-Tone FFT with f_{IN} = 10.3 MHz

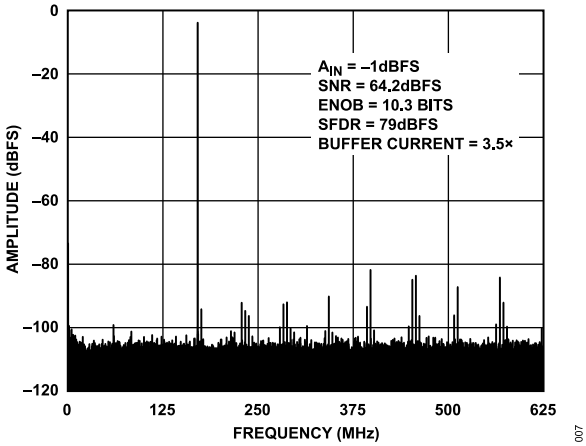

Figure 7. Single-Tone FFT with f_{IN} = 170.3 MHz

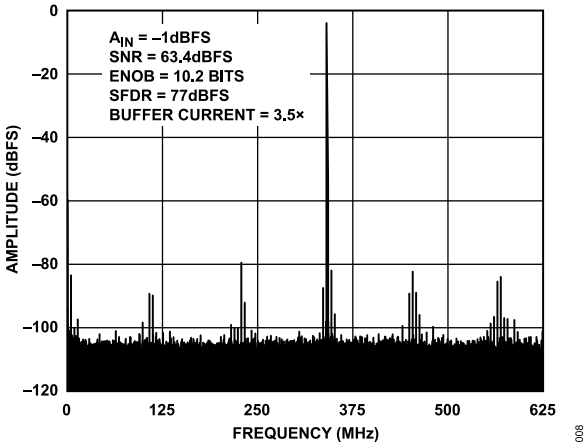

Figure 8. Single-Tone FFT with f_{IN} = 340.3 MHz

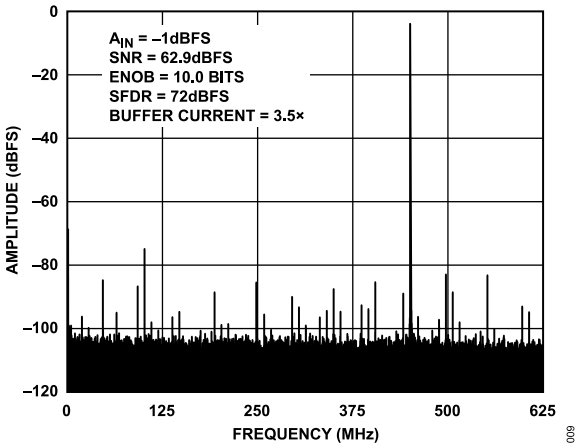

Figure 9. Single-Tone FFT with f_{IN} = 450.3 MHz

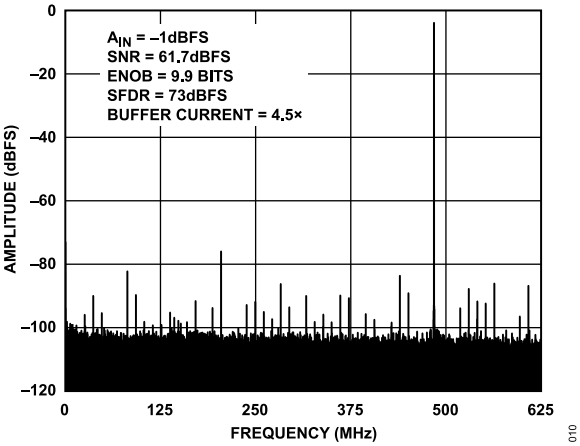

Figure 10. Single-Tone FFT with f_{IN} = 752.3 MHz

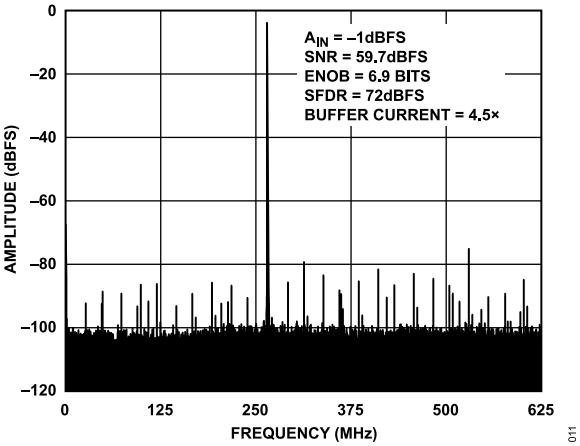

Figure 11. Single-Tone FFT with f_{IN} = 985.3 MHz

TYPICAL PERFORMANCE CHARACTERISTICS

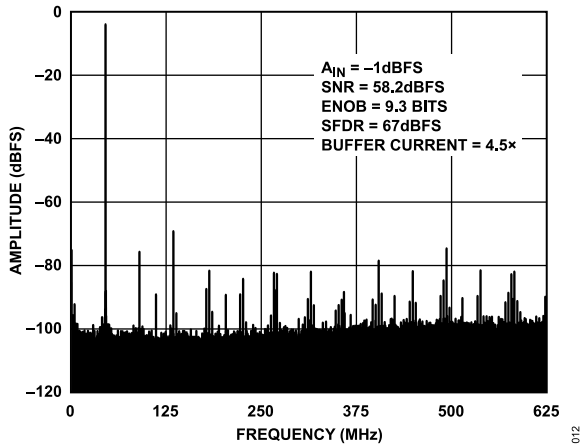

Figure 12. Single-Tone FFT with f_{IN} = 1205.3 MHz

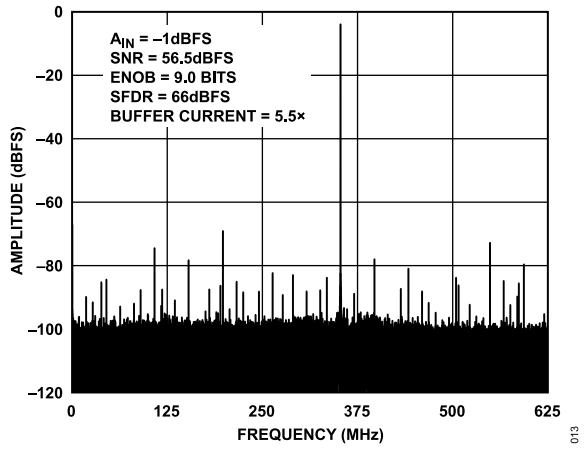

Figure 13. Single-Tone FFT with f_{IN} = 1600.3 MHz

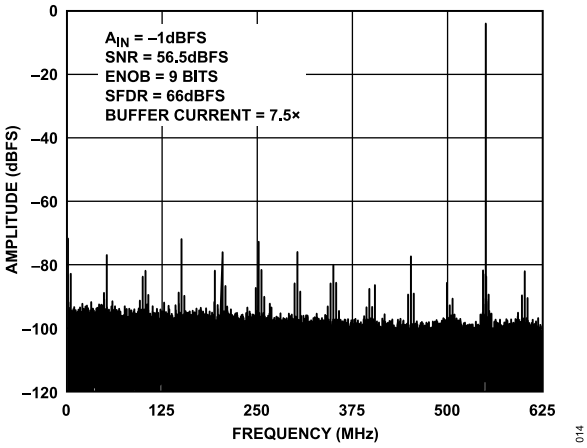

Figure 14. Single-Tone FFT with f_{IN} = 1950.3 MHz

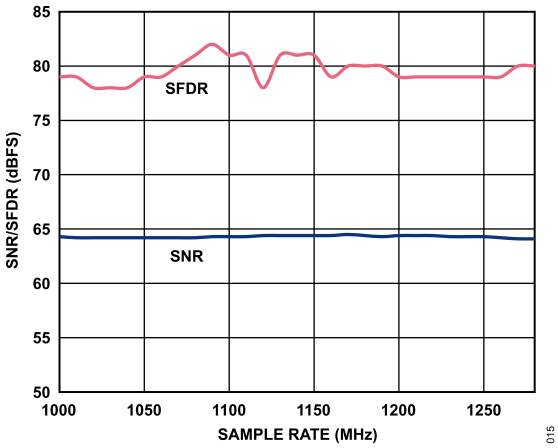

Figure 15. SNR/SFDR vs. Sample Rate (f_S), f_{IN} = 170.3 MHz, Buffer Current = 3.0×

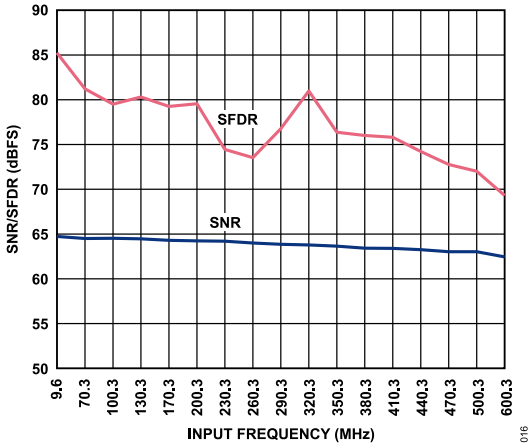

Figure 16. SNR/SFDR vs. Input Frequency (f_{IN}), f_{IN} < 600 MHz,Buffer Current = 3.5× (See Figure 41 and Table 9)

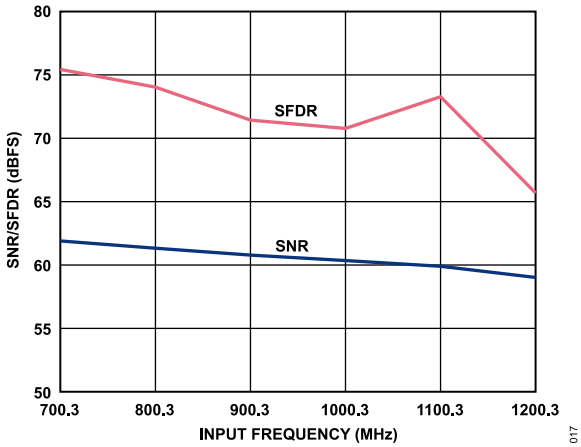

Figure 17. SNR/SFDR vs. Input Frequency (f_{IN}), 700 MHz < f_{IN} < 1200 MHz, Buffer Current = 4.5× (See Figure 41 and Table 9)

TYPICAL PERFORMANCE CHARACTERISTICS

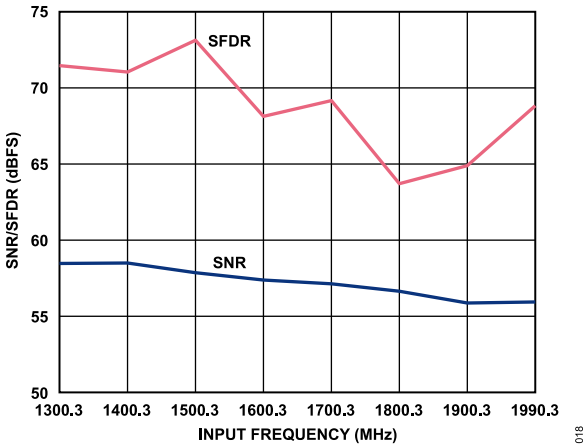

Figure 18. SNR/SFDR vs. Input Frequency (f_{IN}), 1300 MHz < f_{IN} < 2000 MHz, Buffer Current = 7.5× (See Figure 41 and Table 9)

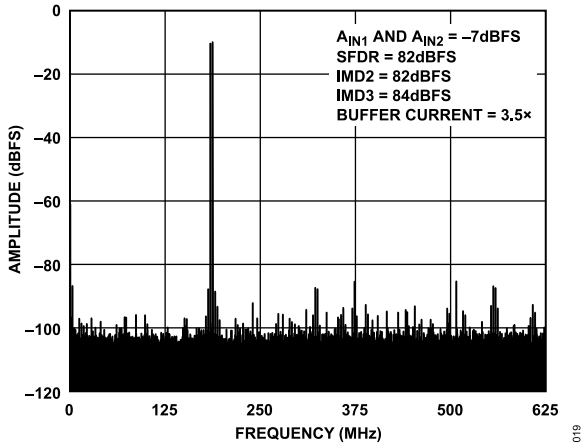

Figure 19. Two-Tone FFT, f_{IN1} = 184 MHz, f_{IN2} = 187 MHz

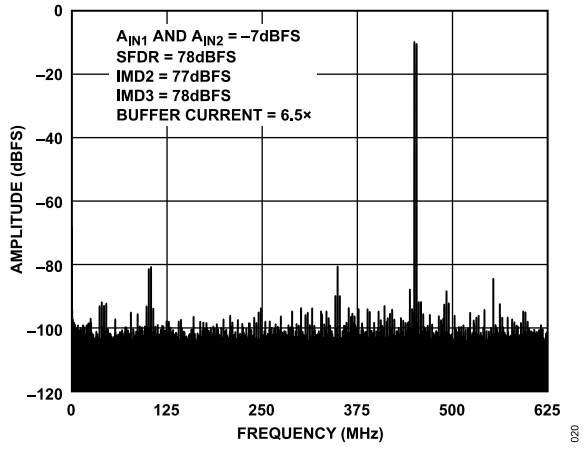

Figure 20. Two-Tone FFT, f_{IN1} = 449 MHz, f_{IN2} = 452 MHz

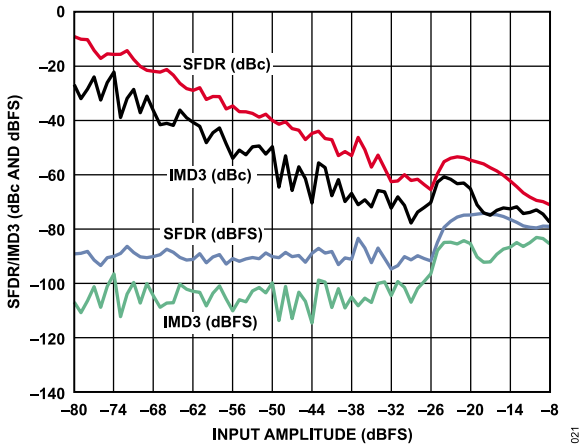

Figure 21. Two-Tone SFDR/IMD3 vs. Input Amplitude (A_{IN}) with f_{IN1} = 184 MHz and f_{IN2} = 187 MHz

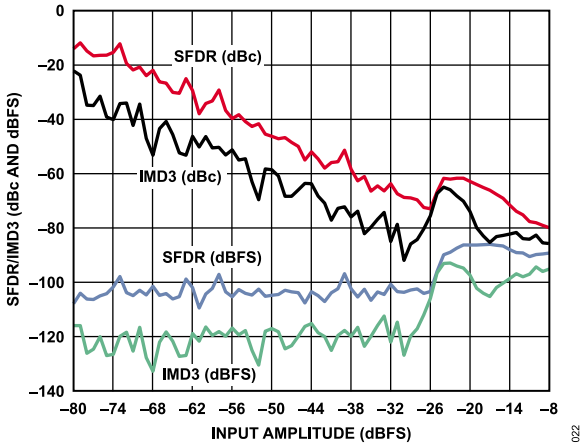

Figure 22. Two-Tone SFDR/IMD3 vs. Input Amplitude (A_{IN}) with f_{IN1} = 449 MHz and f_{IN2} = 452 MHz

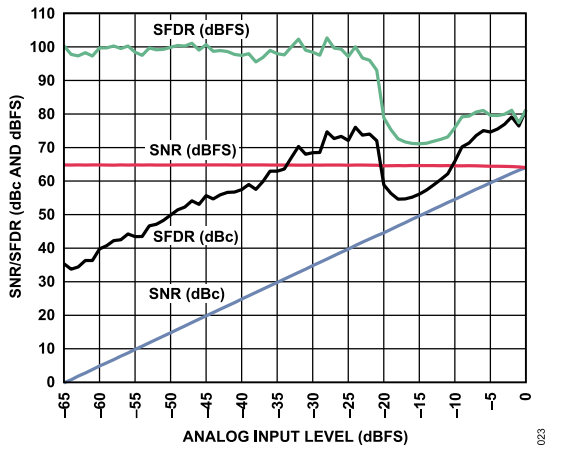

Figure 23. SNR/SFDR vs. Analog Input Level, f_{IN} = 170.3 MHz, Buffer Current = 3.5×

TYPICAL PERFORMANCE CHARACTERISTICS

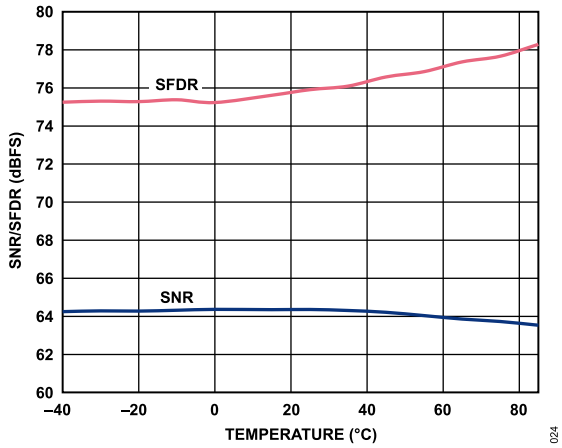

Figure 24. SNR/SFDR vs. Temperature, f_{IN} = 170.3 MHz

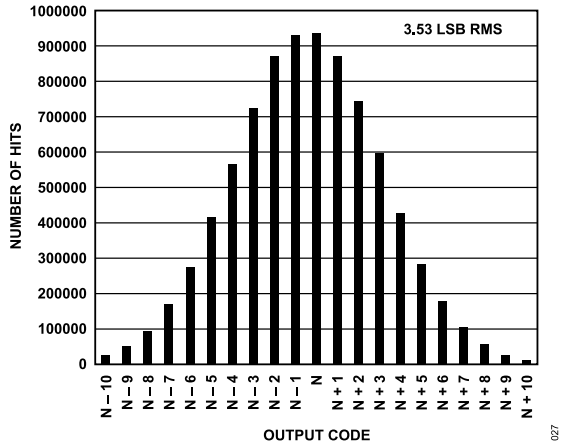

Figure 27. Input Referred Noise Histogram

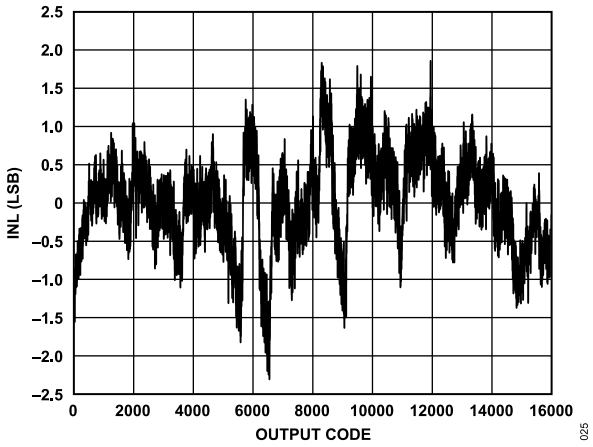

Figure 25. INL, f_{IN} = 10.3 MHz

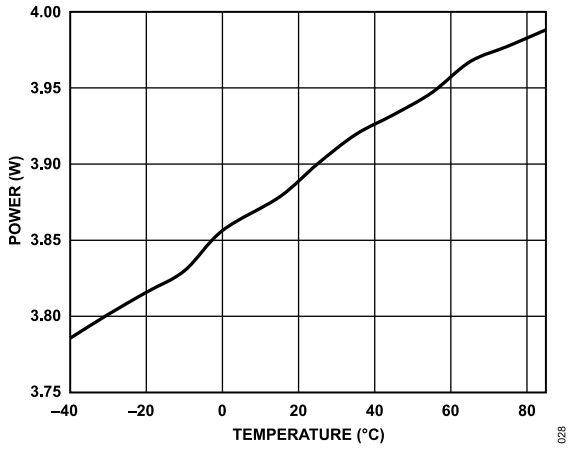

Figure 28. Power vs. Temperature

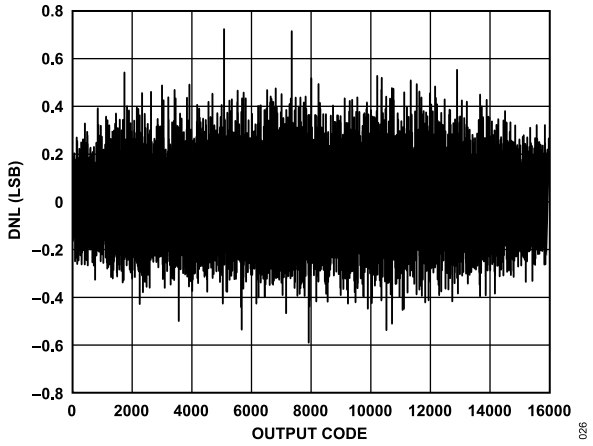

Figure 26. DNL, f_{IN} = 10 MHz

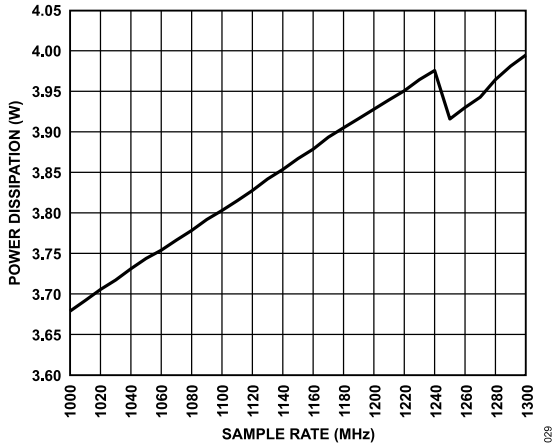

Figure 29. Power Dissipation vs. Sample Rate (f_S)

EQUIVALENT CIRCUITS

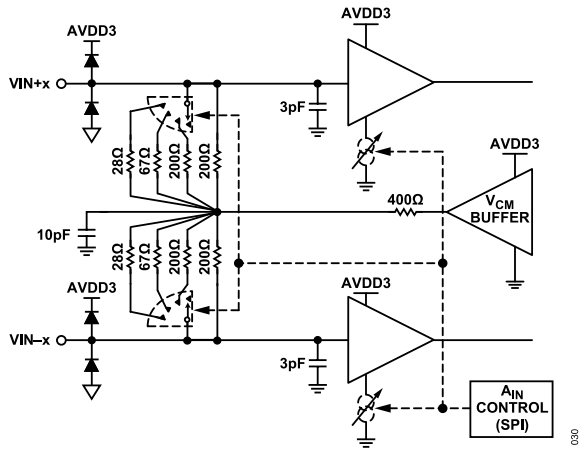

Figure 30. Analog Inputs

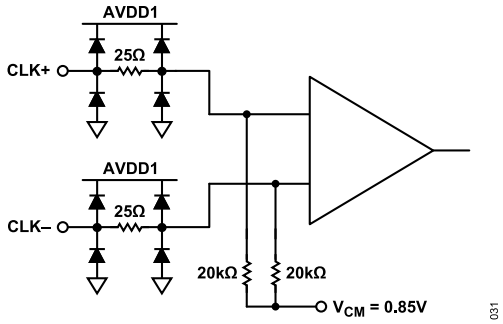

Figure 31. Clock Inputs

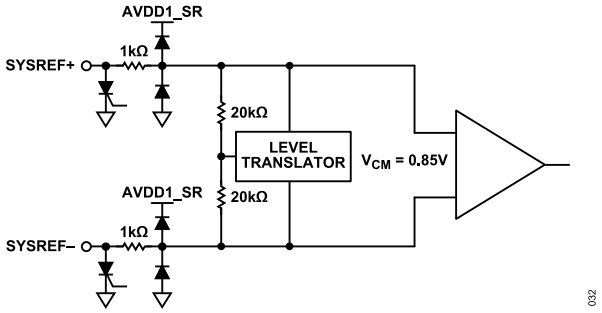

Figure 32. SYSREF± Inputs

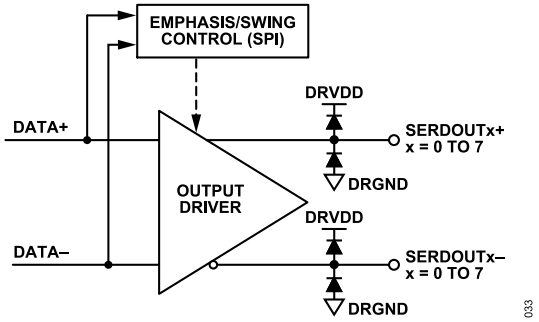

Figure 33. Digital Outputs

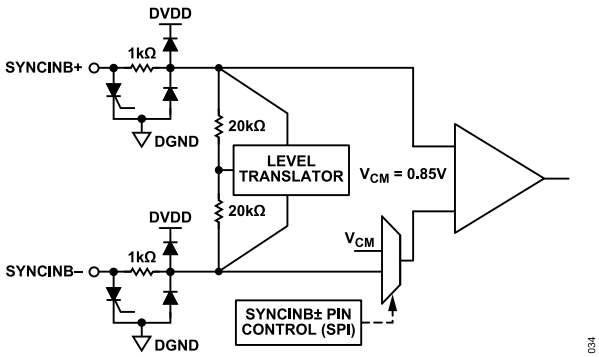

Figure 34. SYNCINB± Inputs

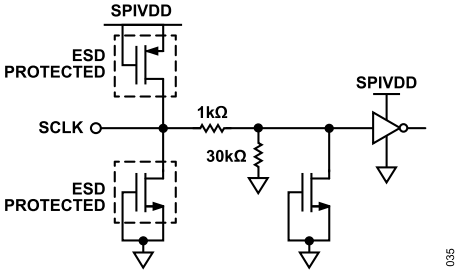

Figure 35. SCLK Input

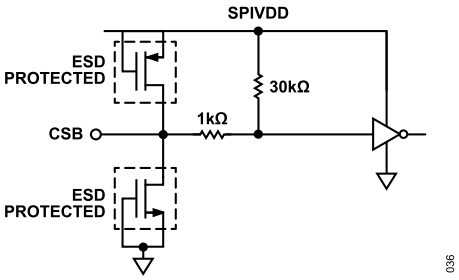

Figure 36. CSB Input

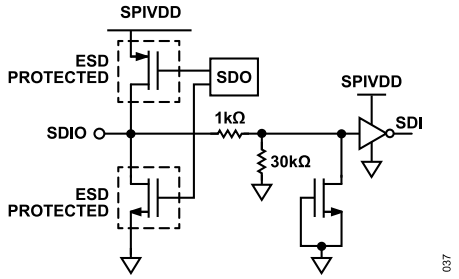

Figure 37. SDIO Input

EQUIVALENT CIRCUITS

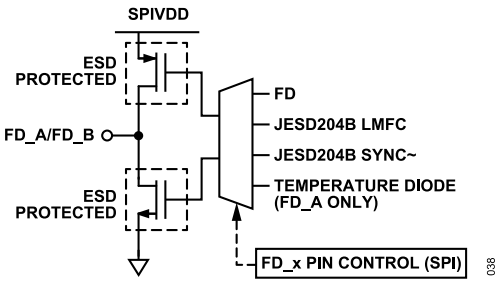

Figure 38. FD_A/FD_B Outputs

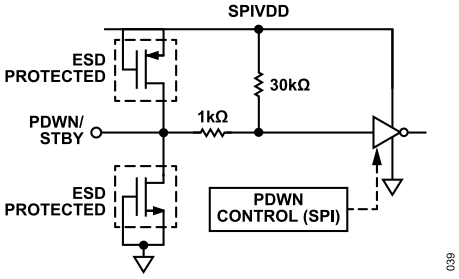

Figure 39. PDWN/STBY Input

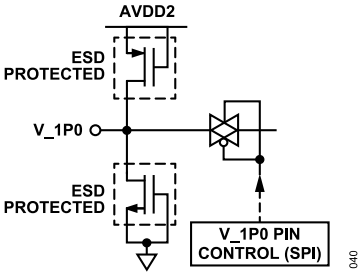

Figure 40. V_1P0 Input

THEORY OF OPERATION

The AD9691 has two analog input channels and four JESD204B output lane pairs. The ADC is designed to sample wide bandwidth analog signals of up to 1.5 GHz. The AD9691 is optimized for wide input bandwidth, a high sampling rate, excellent linearity, and low power in a small package.

The dual ADC cores feature multistage, differential pipelined architecture with integrated output error correction logic. Each ADC features wide bandwidth inputs supporting a variety of user-selectable input ranges. An integrated voltage reference eases design considerations.

The AD9691 has several functions that simplify the AGC function in a communications receiver. The programmable threshold detector allows monitoring of the incoming signal power using the fast detect output bits of the ADC. If the input signal level exceeds the programmable threshold, the fast detect indicator goes high. Because this threshold indicator has low latency, the user can quickly turn down the system gain to avoid an overrange condition at the ADC input.

The Subclass 1 JESD204B-based, high speed serialized output data rate can be configured in one-lane (L = 1), two-lane (L = 2), four-lane (L = 4), and eight-lane (L = 8) configurations, depending on the sample rate and the decimation ratio (DCM). Multiple device synchronization is supported through the SYSREF± and SYNCINB± input pins.

ADC ARCHITECTURE

The architecture of the AD9691 consists of an input buffered pipelined ADC. The input buffer provides a termination impedance to the analog input signal. This termination impedance can be changed using the SPI to meet the termination needs of the driver or amplifier. The default termination value is set to 400 Ω. The equivalent circuit diagram of the analog input termination is shown in Figure 30. The input buffer is optimized for high linearity, low noise, and low power.

The input buffer provides a linear high input impedance (for ease of drive) and reduces the kickback from the ADC. The buffer is optimized for high linearity, low noise, and low power. The quantized outputs from each stage are combined into a final 14-bit result in the digital correction logic. The pipelined architecture permits the first stage to operate with a new input sample; at the same time, the remaining stages operate with the preceding samples. Sampling occurs on the rising edge of the clock.

ANALOG INPUT CONSIDERATIONS

The analog input to the AD9691 is a differential buffer. The internal common-mode voltage of the buffer is 2.05 V. The clock signal alternately switches the input circuit between sample mode and hold mode. When the input circuit is switched into sample mode, the signal source must be capable of charging the sample capacitors and settling within one-half of a clock cycle. A small resistor, in series with each input, helps reduce the peak transient current injected from the output stage of the driving source. In addition, place low Q inductors or ferrite beads on each section of the input to reduce high differential capacitance at the analog inputs and, thus, achieve the maximum bandwidth of the ADC. Such use of low Q inductors or ferrite beads is required when driving the converter front end at high IF frequencies. Place either a differential capacitor or two single-ended capacitors on the inputs to provide a matching passive network. This configuration ultimately creates a low-pass filter at the input, which limits unwanted broadband noise. For more information, see the AN-742 Application Note, the AN-827 Application Note, and the *Analog Dialogue* article "Transformer-Coupled Front-End for Wideband A/D Converters" (Volume 39, April 2005). In general, the precise values depend on the application.

For best dynamic performance, the source impedances driving VIN+x and VIN−x must be matched such that common-mode settling errors are symmetrical. These errors are reduced by the common-mode rejection of the ADC. An internal reference buffer creates a differential reference that defines the span of the ADC core.

The maximum SNR performance is achieved by setting the ADC to the largest span in a differential configuration. In the case of the AD9691, the available span is 1.58 V p-p differential.

Differential Input Configurations

There are several ways to drive the AD9691, either actively or passively. However, optimum performance is achieved by driving the analog input differentially.

For applications where SNR and SFDR are key parameters, differential transformer coupling is the recommended input configuration (see Figure 41 and Table 9) because the noise performance of most amplifiers is not adequate to achieve the true performance of the AD9691.

For low to midrange frequencies, a double balun or double transformer network (see Figure 41) is recommended for optimum performance of the AD9691. For higher frequencies in the second and third Nyquist zones, it is better to remove some of the front-end passive components to ensure wideband operation (see Table 9).

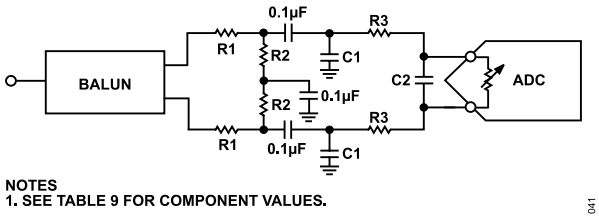

Figure 41. Differential Transformer-Coupled Configuration

THEORY OF OPERATION

Table 9. Differential Transformer-Coupled Input Configuration Component Values

Frequency Range	Transformer/Balun	R1 (Ω)	R2 (Ω)	R3 (Ω)	C1 (pF)	C2 (pF)
<625 MHz	BAL-0006/BAL-0006SMG/ETC1-1-13	10	50	15	Open	3
>625 MHz	BAL-0006/BAL-0006SMG	10	50	0	Open	Open

Input Common Mode

The analog inputs of the AD9691 are internally biased to the common mode as shown in Figure 42. The common-mode buffer has a limited range in that the performance suffers greatly if the common-mode voltage drops by more than 100 mV. Therefore, in dc-coupled applications, set the common-mode voltage to 2.05 V ± 100 mV to ensure proper ADC operation.

Analog Input Controls and SFDR Optimization

The AD9691 offers flexible controls for the analog inputs, such as input termination and buffer current. All of the available controls are shown in Figure 42.

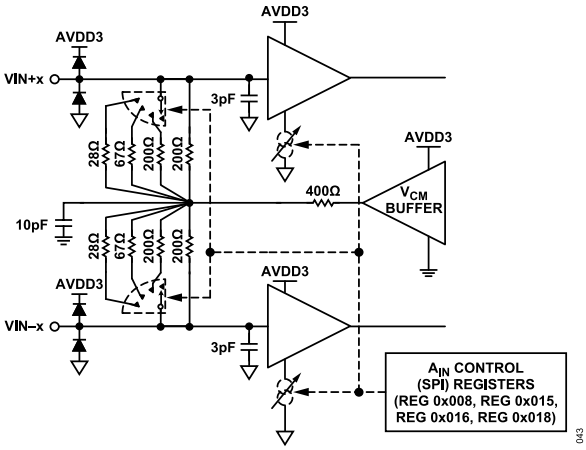

Figure 42. Analog Input Controls

Using Register 0x018, the buffer currents on each channel can be scaled to optimize the SFDR over various input frequencies and bandwidths of interest. As the input buffer currents are set, the amount of current required by the AVDD3 supply changes. This relationship is shown in Figure 43. For a complete list of buffer current settings, see Table 35.

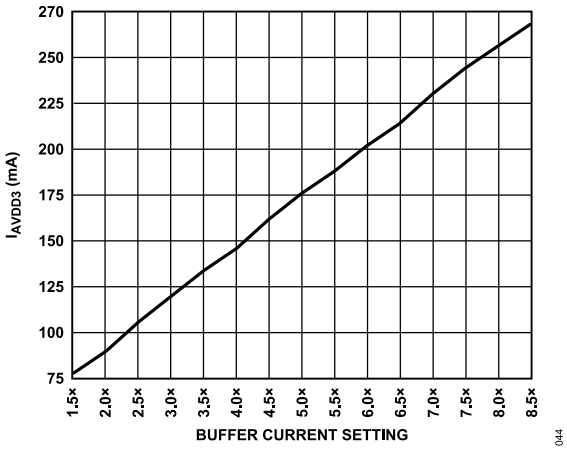

Figure 43. AVDD3 Power (I_{AVDD3}) vs. Buffer Current Setting

Figure 44, Figure 45, and Figure 46 show how the SFDR can be optimized using the buffer current setting in Register 0x018 for different Nyquist zones. At frequencies greater than 1 GHz, it is better to run the ADC at input amplitudes less than −1 dBFS (−3 dBFS, for example). This greatly improves the linearity of the converted signal without sacrificing SNR performance.

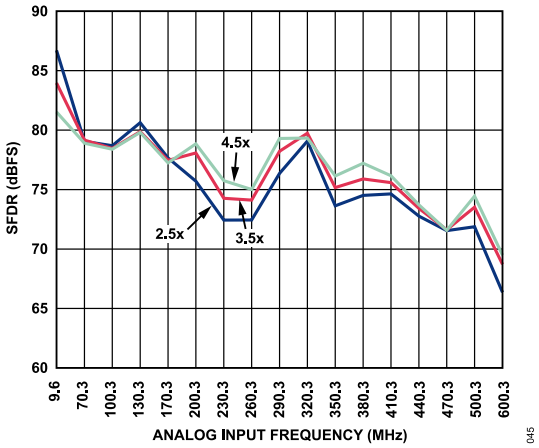

Figure 44. Buffer Current Sweeps, SFDR vs. Analog Input Frequency vs. I_{BUFF}; f_{IN} < 600 MHz

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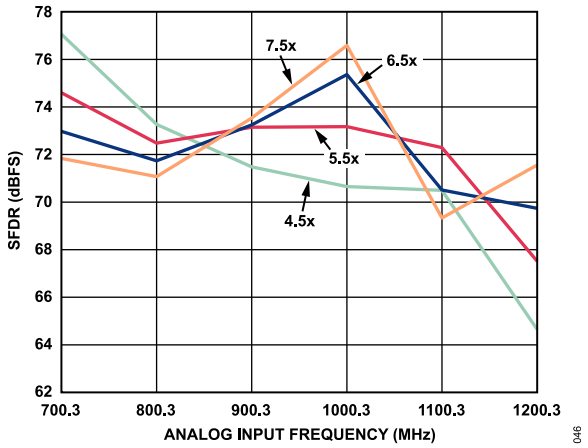

Figure 45. Buffer Current Sweeps, SFDR vs. Analog Input Frequency vs. I_{BUFF}; 700 MHz < f_{IN} < 1200 MHz

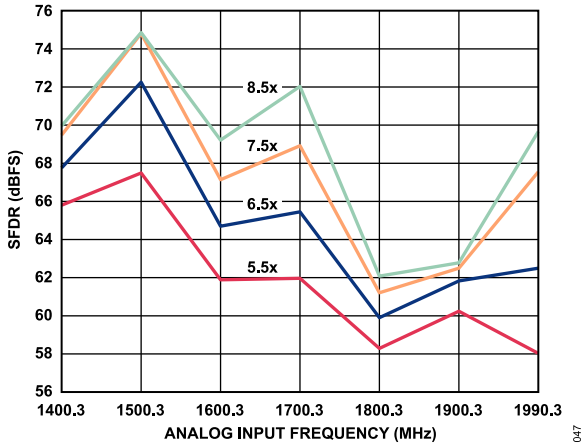

Figure 46. Buffer Current Sweeps, SFDR vs. Analog Input Frequency vs. I_{BUFF}; 1300 MHz < f_{IN} < 2000 MHz

Table 10 shows the recommended buffer current and full-scale voltage settings for the different analog input frequency ranges.

Table 10. SFDR Optimization for Input Frequencies

Input Frequency	Input Buffer Current Control Setting (Register 0x018)	Buffer Control 2 Register (Register 0x935)
<500 MHz	3.5×	0x04
500 MHz to 1 GHz	5.5× or 6.5×	0x00
>1 GHz	6.5× or higher	0x00

Absolute Maximum Input Swing

The absolute maximum input swing allowed at the inputs of the AD9691 is 4.3 V p-p differential. Signals operating near or at this level can cause permanent damage to the ADC.

VOLTAGE REFERENCE

A stable and accurate 1.0 V voltage reference is built into the AD9691. This internal 1.0 V reference sets the full-scale input range of the ADC. For more information on adjusting the input swing, see Table 35. Figure 47 shows the block diagram of the internal 1.0 V reference controls.

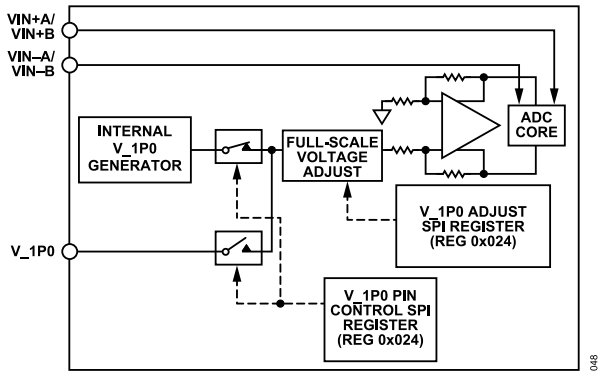

Figure 47. Internal Reference Configuration and Controls

Register 0x024 enables the user to either use this internal 1.0 V reference, or to provide an external 1.0 V reference. When using an external voltage reference, provide a 1.0 V reference. The full-scale adjustment is made using the SPI, irrespective of the reference voltage. For more information on adjusting the full-scale level of the AD9691, see the Memory Map Register Table section.

The use of an external reference may be necessary, in some applications, to enhance the gain accuracy of the ADC or improve thermal drift characteristics. Figure 48 shows the typical drift characteristics of the internal 1.0 V reference.

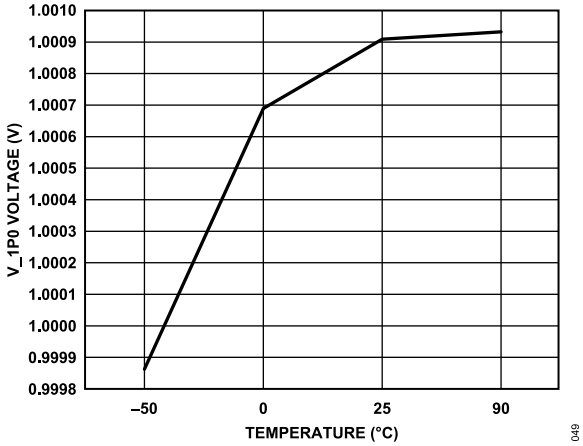

Figure 48. Typical V_1P0 Drift

The external reference must be a stable 1.0 V reference. The ADR130 is a good option for providing the 1.0 V reference. Figure 49 shows how the ADR130 can be used to provide the external 1.0 V reference to the AD9691. The grayed out areas show unused blocks within the AD9691 when using the ADR130 to provide the external reference.

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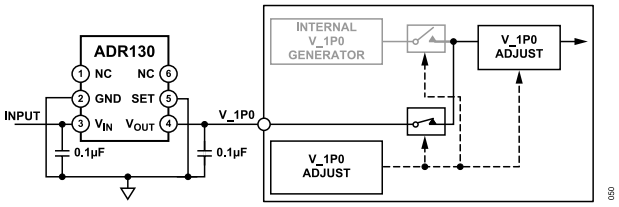

Figure 49. External Reference Using the ADR130

CLOCK INPUT CONSIDERATIONS

For optimum performance, drive the AD9691 sample clock inputs (CLK+ and CLK−) with a differential signal. This signal is typically ac-coupled to the CLK+ and CLK− pins via a transformer or clock drivers. These pins are biased internally and require no additional biasing.

Figure 50 shows a preferred method for clocking the AD9691. The low jitter clock source is converted from a single-ended signal to a differential signal using an RF transformer.

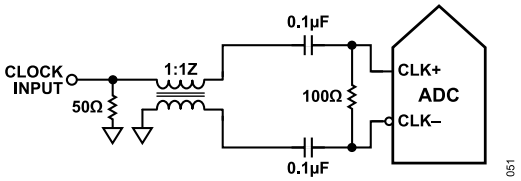

Figure 50. Transformer-Coupled Differential Clock

Another option is to ac couple a differential CML or LVDS signal to the sample clock input pins, as shown in Figure 51 and Figure 52.

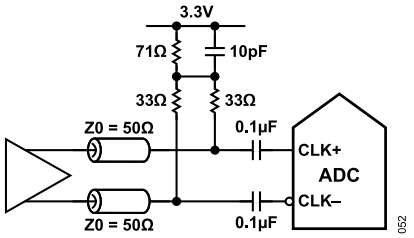

Figure 51. Differential CML Sample Clock

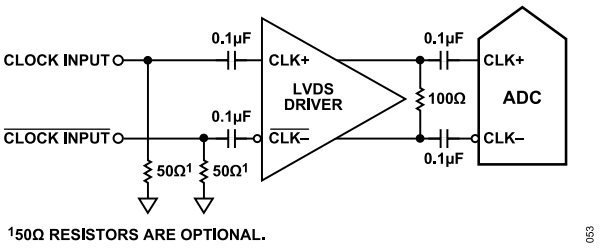

Figure 52. Differential LVDS Sample Clock

Clock Duty Cycle Considerations

Typical high speed ADCs use both clock edges to generate a variety of internal timing signals. As a result, these ADCs may be sensitive to the clock duty cycle. Commonly, a 5% tolerance is required on the clock duty cycle to maintain dynamic performance characteristics. In applications where the clock duty cycle cannot be guaranteed to be 50%, a higher multiple frequency clock can be supplied to the device. The AD9691 can be clocked at 1.5 GHz with the internal clock divider set to 2. The output of the divider offers a 50% duty cycle, high slew rate (fast edge) clock signal to the internal ADC. See the Memory Map section for more details on using this feature.

Input Clock Divider ½ Period Delay Adjust

The input clock divider inside the AD9691 provides phase delay in increments of ½ the input clock cycle. Register 0x10C can be programmed to enable this delay independently for each channel. Changing this register does not affect the stability of the JESD204B link.

Input Clock Divider

The AD9691 contains an input clock divider with the ability to divide the Nyquist input clock by 1, 2, 4, or 8. The divider ratios can be selected using Register 0x10B. This is shown in Figure 53.

The maximum frequency at the CLK± inputs is 4 GHz. This is the limit of the divider. In applications where the clock input is a multiple of the sample clock, the appropriate divider ratio must be programmed into the clock divider before applying the clock signal. This ensures that the current transients during device startup are controlled.

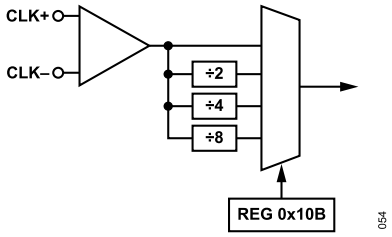

Figure 53. Clock Divider Circuit

The AD9691 clock divider can be synchronized using the external SYSREF± input. A valid SYSREF± signal causes the clock divider to reset to a programmable state. Enable this feature by setting Bit 7 of Register 0x10D. This synchronization feature allows multiple devices to have their clock dividers aligned to guarantee simultane-

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ous input sampling. See the Multichip Synchronization section for more information.

Clock Fine Delay Adjust

The AD9691 sampling edge instant can be adjusted by writing to Register 0x117 and Register 0x118. Setting Bit 0 of Register 0x117 enables the feature, and Register 0x118, Bits[7:0] set the value of the delay. This value can be programmed individually for each channel. The clock delay can be adjusted from −151.7 ps to +150 ps in 1.7 ps increments. The clock delay adjust takes effect immediately when it is enabled via SPI writes. Enabling the clock fine delay adjust in Register 0x117 causes a datapath reset. However, the contents of Register 0x118 can be changed without affecting the stability of the JESD204B link.

Clock Jitter Considerations

High speed, high resolution ADCs are sensitive to the quality of the clock input. The degradation in SNR at a given input frequency (f_A) due only to aperture jitter (t_J) can be calculated by

$$SNR = 20\log_{10}(2 \times \pi \times f_A \times t_J)$$

In this equation, the rms aperture jitter represents the root mean square of all jitter sources, including the clock input, analog input signal, and ADC aperture jitter specifications. IF undersampling applications are particularly sensitive to jitter (see Figure 54).

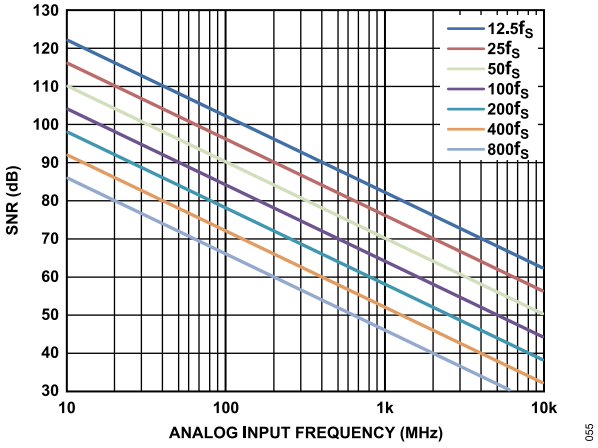

Figure 54. Ideal SNR vs. Analog Input Frequency and Jitter

Treat the clock input as an analog signal in cases where aperture jitter may affect the dynamic range of the AD9691. Separate power supplies for clock drivers from the ADC output driver supplies to avoid modulating the clock signal with digital noise. If the clock is generated from another type of source (by gating, dividing, or other methods), retime the clock by the original clock at the last step. For more in-depth information about jitter performance as it relates to ADCs, see the AN-501 Application Note and the AN-756 Application Note.

POWER-DOWN/STANDBY MODE

The AD9691 has a PDWN/STBY pin that configures the device in power-down or standby mode. The default operation is the power-down function. The PDWN/STBY pin is a logic high pin. When in power-down mode, the JESD204B link is disrupted. The power-down option can also be set via Register 0x03F and Register 0x040.

In standby mode, the JESD204B link is not disrupted and transmits zeros for all converter samples. This can be changed using Register 0x571, Bit 7 to select /K/ characters.

TEMPERATURE DIODE

The AD9691 contains a diode-based temperature sensor for measuring the temperature of the die. This diode can output a voltage and serve as a coarse temperature sensor to monitor the internal die temperature.

The temperature diode voltage can be output to the FD_A pin using the SPI. Use Register 0x028, Bit 0 to enable or disable the diode. Register 0x028 is a local register; therefore, Channel A must be selected in the device index register (Register 0x008) to enable the temperature diode readout. Configure the FD_A pin to output the diode voltage by programming Register 0x040, Bits[2:0]. See Table 35 for more information.

The voltage response of the temperature diode (SPIVDD = 1.8 V) is shown in Figure 55.

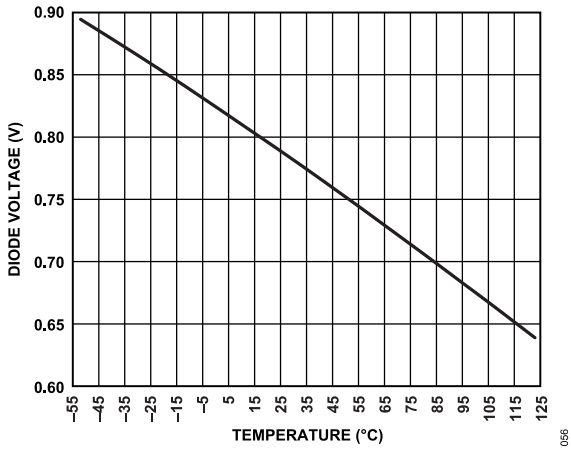

Figure 55. Diode Voltage vs. Temperature

ADC OVERRANGE AND FAST DETECT

In receiver applications, it is desirable to have a mechanism to reliably determine when the converter is about to clip. The standard overrange bit in the JESD204B outputs provides information on the state of the analog input that is of limited usefulness. Therefore, it is helpful to have a programmable threshold below full scale that allows time to reduce the gain before the clip actually occurs. In addition, because input signals can have significant slew rates, the latency of this function is of major concern. Highly pipelined converters can have significant latency. The AD9691 contains fast detect circuitry for individual channels to monitor the threshold and assert the FD_A and FD_B pins.

ADC OVERRANGE

The ADC overrange indicator is asserted when an overrange is detected on the input of the ADC. The overrange indicator can be embedded within the JESD204B link as a control bit (when CSB > 0). The latency of this overrange indicator matches the sample latency.

The AD9691 also records any overrange condition in any of the four virtual converters. For more information on the virtual converters, see Figure 61. The overrange status of each virtual converter is registered as a sticky bit in Register 0x563. The contents of Register 0x563 can be cleared using Register 0x562, by toggling the bits corresponding to the virtual converter to the set and reset positions.

FAST THRESHOLD DETECTION (FD_A AND FD_B)

The fast detect (FD) bit (enabled via the control bits in Register 0x559 and Register 0x55A) is immediately set whenever the absolute value of the input signal exceeds the programmable upper threshold level. The FD bit is cleared only when the absolute value of the input signal drops below the lower threshold level for greater than the programmable dwell time. This feature provides hysteresis and prevents the FD bit from excessively toggling.

The operation of the upper threshold and lower threshold registers, along with the dwell time registers, is shown in Figure 56.

The FD indicator is asserted if the input magnitude exceeds the value programmed in the fast detect upper threshold registers, located at Register 0x247 and Register 0x248. The selected threshold register is compared with the signal magnitude at the output of the ADC. The fast upper threshold detection has a latency of 28 clock cycles (maximum). The approximate upper threshold magnitude is defined by

Upper Threshold Magnitude (dBFS) = 20log(*Threshold Magnitude*/ 2^{13})

The FD indicators are not cleared until the signal drops below the lower threshold for the programmed dwell time. The lower threshold is programmed in the fast detect lower threshold registers, located at Register 0x249 and Register 0x24A. The fast detect lower threshold register is a 13-bit register that is compared with the signal magnitude at the output of the ADC. This comparison is subject to the ADC pipeline latency, but is accurate in terms of converter resolution. The lower threshold magnitude is defined by

Lower Threshold Magnitude (dBFS) = 20log(*Threshold Magnitude*/ 2^{13})

For example, to set an upper threshold of −6 dBFS, write 0xFFF to Register 0x247 and Register 0x248. To set a lower threshold of −10 dBFS, write 0xA1D to Register 0x249 and Register 0x24A.

To program the dwell time from 1 to 65,535 sample clock cycles, place the desired value in the fast detect dwell time registers, located at Register 0x24B and Register 0x24C. See the Memory Map section (Register 0x040, and Register 0x245 to Register 0x24C in Table 35) for more details.

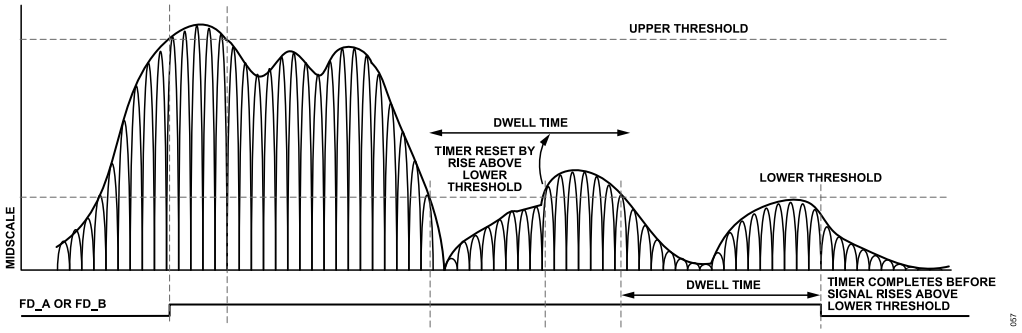

Figure 56. Threshold Settings for FD_A and FD_B Signals

SIGNAL MONITOR

The signal monitor block provides additional information about the signal being digitized by the ADC. The signal monitor computes the peak magnitude of the digitized signal. This information can be used to drive an AGC loop to optimize the range of the ADC in the presence of real-world signals.

The results of the signal monitor block can be obtained either by reading back the internal values from the SPI port or by embedding the signal monitoring information into the JESD204B interface as special control bits. A global, 24-bit programmable period controls the duration of the measurement. Figure 57 shows the simplified block diagram of the signal monitor block.

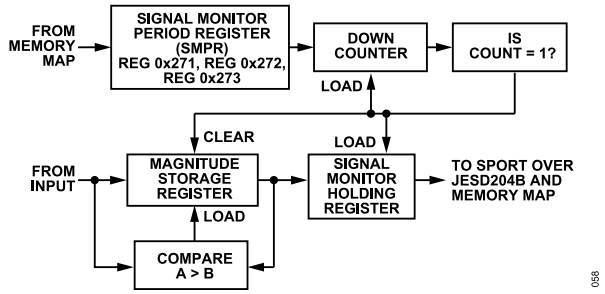

Figure 57. Signal Monitor Block

The peak detector captures the largest signal within the observation period. The detector only observes the magnitude of the signal. The resolution of the peak detector is a 13-bit value, and the observation period is 24 bits and represents converter output samples. The peak magnitude can be derived by using the following equation:

Peak Magnitude (dBFS) = 20log(*Peak Detector Value*/2^{13})

The magnitude of the input port signal is monitored over a programmable time period, which is determined by the signal monitor period register (SMPR). The peak detector function is enabled by setting Bit 1 of Register 0x270 in the signal monitor control register. The 24-bit SMPR must be programmed before activating this mode.

After enabling this mode, the value in the SMPR is loaded into a monitor period timer, which decrements at the decimated clock rate. The magnitude of the input signal is compared to the value in the internal magnitude storage register (not accessible to the user), and the greater of the two is updated as the current peak level. The initial value of the magnitude storage register is set to the current ADC input signal magnitude. This comparison continues until the monitor period timer reaches a count of 1.

When the monitor period timer reaches a count of 1, the 13-bit peak level value is transferred to the signal monitor holding register, which can be read through the memory map or output through the SPORT over the JESD204B interface. The monitor period timer is reloaded with the value in the SMPR, and the countdown is restarted. In addition, the magnitude of the first input sample is updated in the magnitude storage register, and the comparison and update procedure continues.

SPORT OVER JESD204B

The signal monitor data can also be serialized and sent over the JESD204B interface as control bits. These control bits must be deserialized from the samples to reconstruct the statistical data. This function is enabled by setting Bits[1:0] of Register 0x279 and Bit 1 of Register 0x27A. Figure 58 shows two different example configurations for the signal monitor control bit locations inside the JESD204B samples. A maximum of three control bits can be inserted into the JESD204B samples; however, only one control bit is required for the signal monitor. Control bits are inserted from MSB to LSB. If only one control bit is to be inserted (CS = 1), only the most significant control bit is used (see Example Configuration 1 and Example Configuration 2 in Figure 58). To select the SPORT over JESD204B option, program Register 0x559, Register 0x55A, and Register 0x58F. See Table 35 for more information on setting these bits.

Figure 59 shows the 25-bit frame data that encapsulates the peak detector value. The frame data is transmitted MSB first with five 5-bit subframes. Each subframe contains a start bit that can be used by a receiver to validate the deserialized data. Figure 60 shows the SPORT over JESD204B signal monitor data with a monitor period timer set to 80 samples.

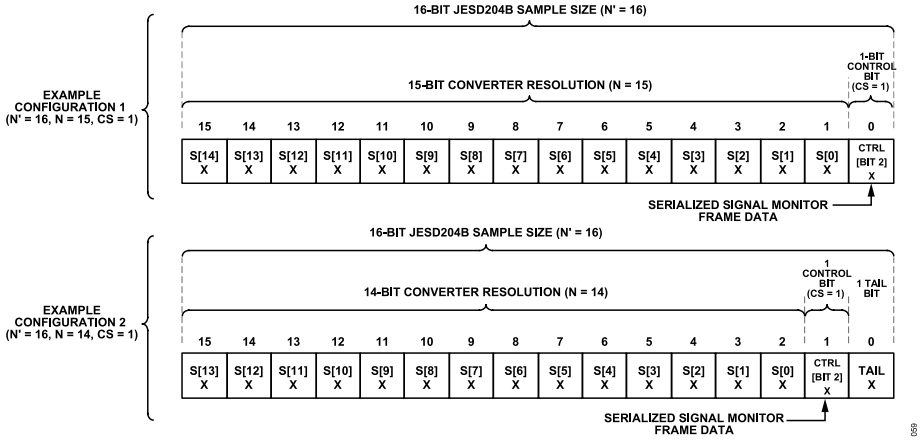

Figure 58. Signal Monitor Control Bit Locations

SIGNAL MONITOR

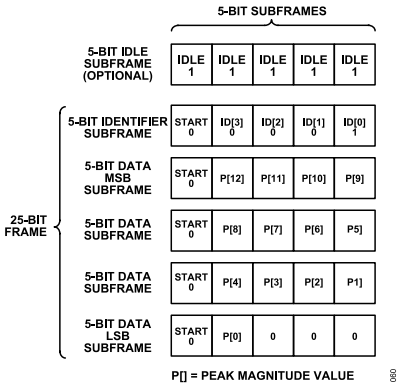

Figure 59. SPORT over JESD204B Signal Monitor Frame Data

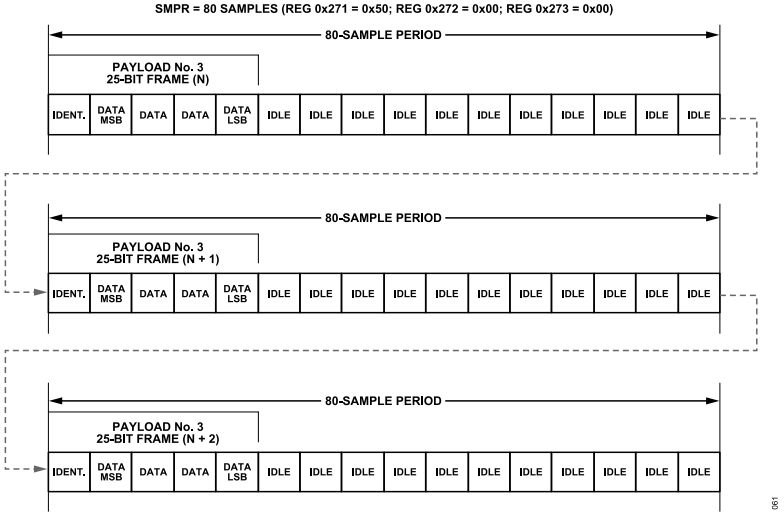

Figure 60. SPORT over JESD204B Signal Monitor Example with Period = 80 Samples

DIGITAL DOWNCONVERTERS (DDCS)

The AD9691 includes four digital downconverters (DDC 0 to DDC 3) that provide filtering and reduce the output data rate. This digital processing section includes a numerically controlled oscillator (NCO), a half-band decimating filter, a finite impulse response (FIR) filter, a gain stage, and a complex to real conversion stage. Each of these processing blocks have control lines that allow it to be independently enabled and disabled to provide the desired processing function. The digital downconverters can be configured to output either real data or complex output data.

DDC I/Q INPUT SELECTION

The AD9691 has two ADC channels and four DDC channels. Each DDC channel has two input ports that can be paired to support both real or complex inputs through the I/Q crossbar mux. For real signals, both DDC input ports must select the same ADC channel (for example, DDC Input Port I = ADC Channel A, and Input Port Q = ADC Channel A). For complex signals, each DDC input port must select different ADC channels (for example, DDC Input Port I = ADC Channel A, and Input Port Q = ADC Channel B).

The inputs to each DDC are controlled by the DDC input selection registers (Register 0x311, Register 0x331, Register 0x351, and Register 0x371). See Table 35 for information on how to configure the DDCs.

DDC I/Q OUTPUT SELECTION

Each DDC channel has two output ports that can be paired to support both real or complex outputs. For real output signals, only the DDC Output Port I is used (the DDC Output Port Q is invalid). For complex I/Q output signals, both DDC Output Port I and DDC Output Port Q are used.

The I/Q outputs to each DDC channel are controlled by the DDC complex to real enable bit (Bit 3) in the DDC control registers (Register 0x310, Register 0x330, Register 0x350, and Register 0x370).

The Chip Q ignore bit (Bit 5) in the chip application mode register (Register 0x200) controls the chip output muxing of all the DDC channels. When all DDC channels use real outputs, this bit must be set high to ignore all DDC Q output ports. When any of the DDC channels are set to use complex I/Q outputs, the user must clear this bit to use both DDC Output Port I and DDC Output Port Q. For more information, refer to Memory Map Register Table section.

DDC GENERAL DESCRIPTION

The four DDC blocks extract a portion of the full digital spectrum captured by the ADC(s). They are intended for IF sampling or oversampled baseband radios requiring wide bandwidth input signals.

Each DDC block contains the following signal processing stages:

- Frequency translation stage (optional)
- Filtering stage
- Gain stage (optional)
- Complex to real conversion stage (optional)

Frequency Translation Stage (Optional)

The frequency translation stage consists of a 12-bit complex NCO and quadrature mixers that can be used for frequency translation of both real or complex input signals. This stage shifts a portion of the available digital spectrum down to baseband.

Filtering Stage

After shifting down to baseband, the filtering stage decimates the frequency spectrum using a chain of up to four half-band low-pass filters for rate conversion. The decimation process lowers the output data rate, which in turn reduces the output interface rate.

Gain Stage (Optional)

Due to losses associated with mixing a real input signal down to baseband, the gain stange compensates by adding an additional 0 dB or 6 dB of gain.

Complex to Real Conversion Stage (Optional)

When real outputs are necessary, the complex to real conversion stage converts the complex outputs back to real by performing an $f_S/4$ mixing operation plus a filter to remove the complex component of the signal.

Figure 61 shows the detailed block diagram of the DDCs implemented in the AD9691.

DIGITAL DOWNCONVERTERS (DDCS)

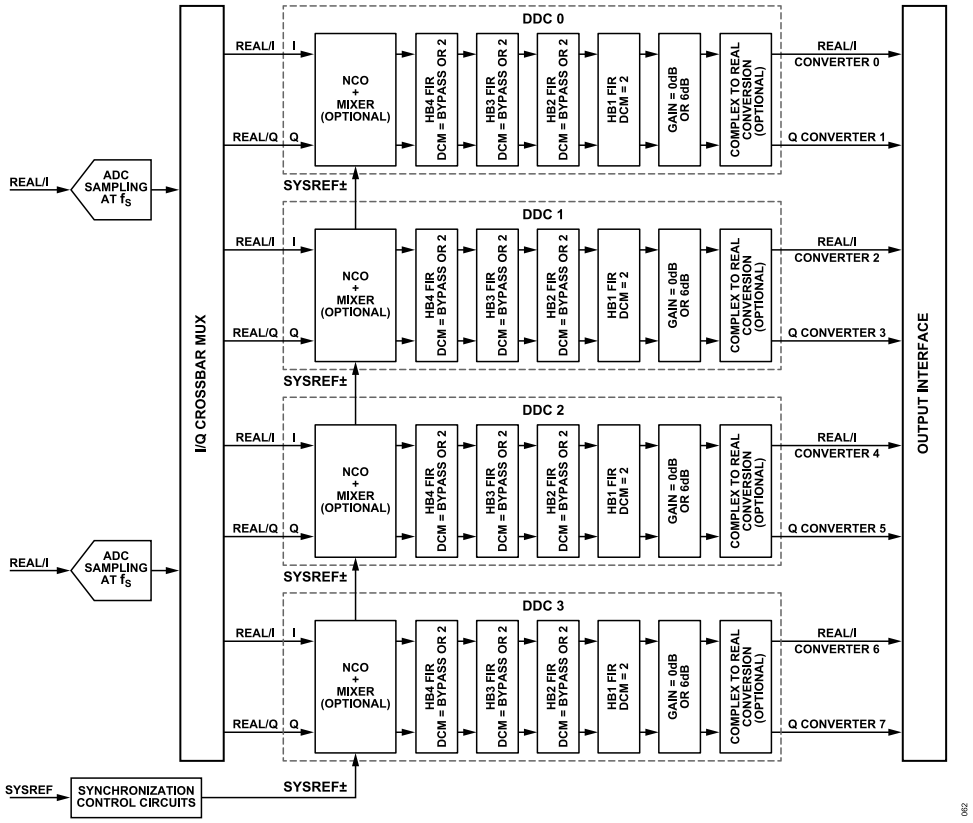

Figure 61. DDC Detailed Block Diagram

Figure 62 shows an example usage of one of the four DDC blocks with a real input signal and four half-band filters (HB4, HB3, HB2, and HB1). It shows both complex (decimate by 16) and real (decimate by 8) output options.

When DDCs have different decimation ratios, the chip decimation ratio (Register 0x201) must be set to the lowest decimation ratio of all the DDC blocks. In this scenario, samples of higher decimation ratio DDCs are repeated to match the chip decimation ratio sample rate. Whenever the NCO frequency is set or changed, the DDC soft reset must be issued. If the DDC soft reset is not issued, the output may potentially show amplitude variations.

Table 11, Table 12, Table 13, Table 14, and Table 15 show the DDC samples when the chip decimation ratio is set to 1, 2, 4, 8, or 16, respectively.

DIGITAL DOWNCONVERTERS (DDCS)

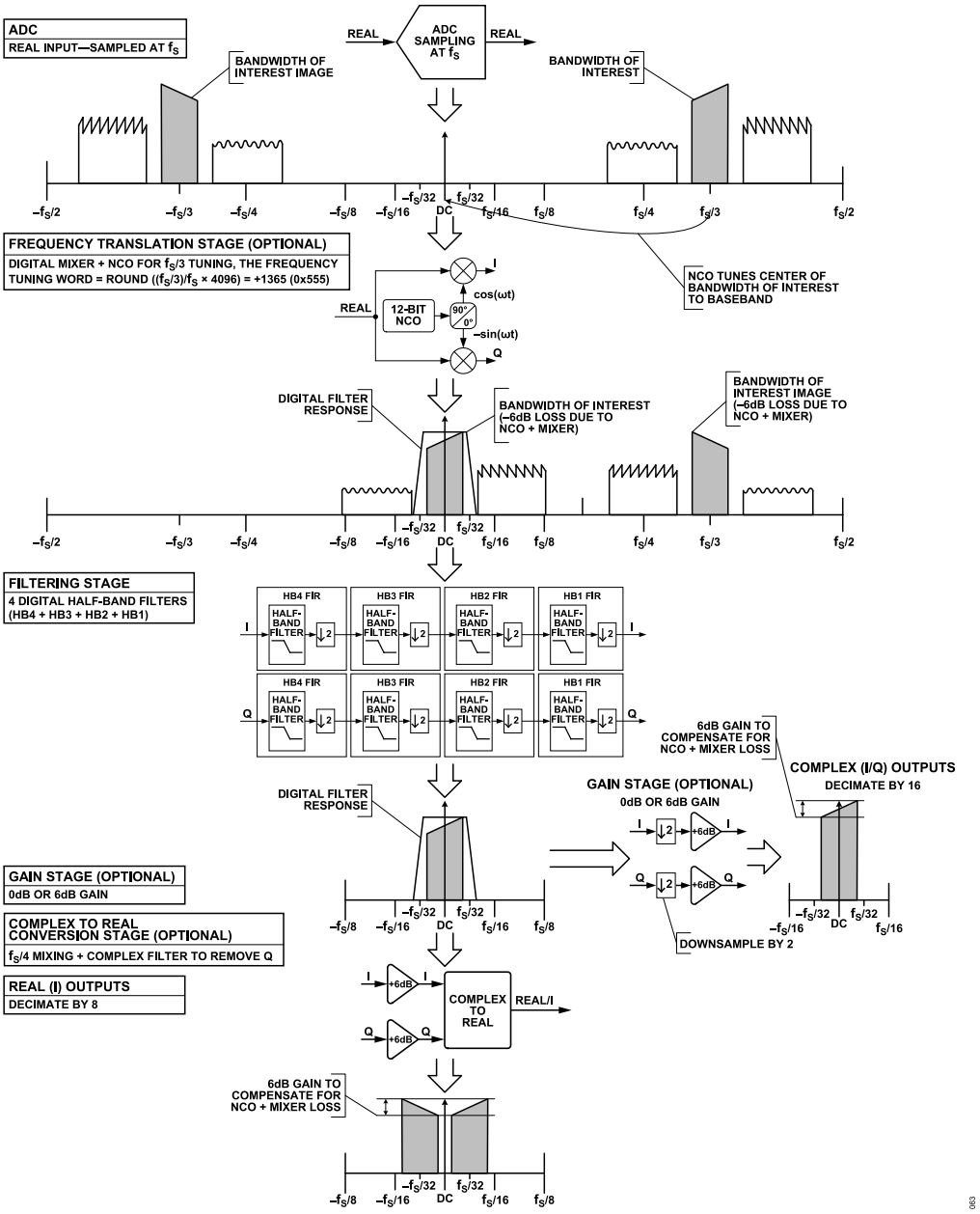

Figure 62. DDC Theory of Operation Example (Real Input—Decimate by 16)

Table 11. DDC Samples, Chip Decimation Ratio = 1

Real (I) Output (Complex to Real Enabled)				Complex (I/Q) Outputs (Complex to Real Disabled)			
HB1 FIR (DCM[1] = 1)	HB2 FIR + HB1 FIR (DCM[1] = 2)	HB3 FIR + HB2 FIR + HB1 FIR (DCM[1] = 4)	HB4 FIR + HB3 FIR + HB2 FIR + HB1 FIR (DCM[1] = 8)	HB1 FIR (DCM[1] = 2)	HB2 FIR + HB1 FIR (DCM[1] = 4)	HB3 FIR + HB2 FIR + HB1 FIR (DCM[1] = 8)	HB4 FIR + HB3 FIR + HB2 FIR + HB1 FIR (DCM[1] = 16)
N	N	N	N	N	N	N	N
N + 1	N + 1	N + 1	N + 1	N + 1	N + 1	N + 1	N + 1
N + 2	N	N	N	N	N	N	N
N + 3	N + 1	N + 1	N + 1	N + 1	N + 1	N + 1	N + 1
N + 4	N + 2	N	N	N + 2	N	N	N
N + 5	N + 3	N + 1	N + 1	N + 3	N + 1	N + 1	N + 1

DIGITAL DOWNCONVERTERS (DDCS)

Table 11. DDC Samples, Chip Decimation Ratio = 1 (Continued)

Real (I) Output (Complex to Real Enabled)				Complex (I/Q) Outputs (Complex to Real Disabled)			
HB1 FIR (DCM[1] = 1)	HB2 FIR + HB1 FIR (DCM[1] = 2)	HB3 FIR + HB2 FIR + HB1 FIR (DCM[1] = 4)	HB4 FIR + HB3 FIR + HB2 FIR + HB1 FIR (DCM[1] = 8)	HB1 FIR (DCM[1] = 2)	HB2 FIR + HB1 FIR (DCM[1] = 4)	HB3 FIR + HB2 FIR + HB1 FIR (DCM[1] = 8)	HB4 FIR + HB3 FIR + HB2 FIR + HB1 FIR (DCM[1] = 16)
N + 6	N + 2	N	N	N + 2	N	N	N
N + 7	N + 3	N + 1	N + 1	N + 3	N + 1	N + 1	N + 1
N + 8	N + 4	N + 2	N	N + 4	N + 2	N	N
N + 9	N + 5	N + 3	N + 1	N + 5	N + 3	N + 1	N + 1
N + 10	N + 4	N + 2	N	N + 4	N + 2	N	N
N + 11	N + 5	N + 3	N + 1	N + 5	N + 3	N + 1	N + 1
N + 12	N + 6	N + 2	N	N + 6	N + 2	N	N
N + 13	N + 7	N + 3	N + 1	N + 7	N + 3	N + 1	N + 1
N + 14	N + 6	N + 2	N	N + 6	N + 2	N	N
N + 15	N + 7	N + 3	N + 1	N + 7	N + 3	N + 1	N + 1
N + 16	N + 8	N + 4	N + 2	N + 8	N + 4	N + 2	N
N + 17	N + 9	N + 5	N + 3	N + 9	N + 5	N + 3	N + 1
N + 18	N + 8	N + 4	N + 2	N + 8	N + 4	N + 2	N
N + 19	N + 9	N + 5	N + 3	N + 9	N + 5	N + 3	N + 1
N + 20	N + 10	N + 4	N + 2	N + 10	N + 4	N + 2	N
N + 21	N + 11	N + 5	N + 3	N + 11	N + 5	N + 3	N + 1
N + 22	N + 10	N + 4	N + 2	N + 10	N + 4	N + 2	N
N + 23	N + 11	N + 5	N + 3	N + 11	N + 5	N + 3	N + 1
N + 24	N + 12	N + 6	N + 2	N + 12	N + 6	N + 2	N
N + 25	N + 13	N + 7	N + 3	N + 13	N + 7	N + 3	N + 1
N + 26	N + 12	N + 6	N + 2	N + 12	N + 6	N + 2	N
N + 27	N + 13	N + 7	N + 3	N + 13	N + 7	N + 3	N + 1
N + 28	N + 14	N + 6	N + 2	N + 14	N + 6	N + 2	N
N + 29	N + 15	N + 7	N + 3	N + 15	N + 7	N + 3	N + 1
N + 30	N + 14	N + 6	N + 2	N + 14	N + 6	N + 2	N
N + 31	N + 15	N + 7	N + 3	N + 15	N + 7	N + 3	N + 1

[1] DCM is decimation.

Table 12. DDC Samples, Chip Decimation Ratio = 2

Real (I) Output (Complex to Real Enabled)			Complex (I/Q) Outputs (Complex to Real Disabled)			
HB2 FIR + HB1 FIR(DCM[1] = 2)	HB3 FIR + HB2 FIR + HB1 FIR(DCM[1] = 4)	HB4 FIR + HB3 FIR + HB2 FIR + HB1 FIR(DCM[1] = 8)	HB1 FIR(DCM[1] = 2)	HB2 FIR + HB1 FIR(DCM[1] = 4)	HB3 FIR + HB2 FIR + HB1 FIR(DCM[1] = 8)	HB4 FIR + HB3 FIR + HB2 FIR + HB1 FIR(DCM[1] = 16)
N	N	N	N	N	N	N
N + 1	N + 1	N + 1	N + 1	N + 1	N + 1	N + 1
N + 2	N	N	N + 2	N	N	N
N + 3	N + 1	N + 1	N + 3	N + 1	N + 1	N + 1
N + 4	N + 2	N	N + 4	N + 2	N	N
N + 5	N + 3	N + 1	N + 5	N + 3	N + 1	N + 1
N + 6	N + 2	N	N + 6	N + 2	N	N
N + 7	N + 3	N + 1	N + 7	N + 3	N + 1	N + 1
N + 8	N + 4	N + 2	N + 8	N + 4	N + 2	N
N + 9	N + 5	N + 3	N + 9	N + 5	N + 3	N + 1
N + 10	N + 4	N + 2	N + 10	N + 4	N + 2	N
N + 11	N + 5	N + 3	N + 11	N + 5	N + 3	N + 1

DIGITAL DOWNCONVERTERS (DDCS)

Table 12. DDC Samples, Chip Decimation Ratio = 2 (Continued)

Real (I) Output (Complex to Real Enabled)			Complex (I/Q) Outputs (Complex to Real Disabled)			
HB2 FIR + HB1 FIR(DCM[1] = 2)	HB3 FIR + HB2 FIR + HB1 FIR(DCM[1] = 4)	HB4 FIR + HB3 FIR + HB2 FIR + HB1 FIR(DCM[1] = 8)	HB1 FIR(DCM[1] = 2)	HB2 FIR + HB1 FIR(DCM[1] = 4)	HB3 FIR + HB2 FIR + HB1 FIR(DCM[1] = 8)	HB4 FIR + HB3 FIR + HB2 FIR + HB1 FIR(DCM[1] = 16)
N + 12	N + 6	N + 2	N + 12	N + 6	N + 2	N
N + 13	N + 7	N + 3	N + 13	N + 7	N + 3	N + 1
N + 14	N + 6	N + 2	N + 14	N + 6	N + 2	N
N + 15	N + 7	N + 3	N + 15	N + 7	N + 3	N + 1

[1] DCM is decimation.

Table 13. DDC Samples, Chip Decimation Ratio = 4

Real (I) Output (Complex to Real Enabled)		Complex (I/Q) Outputs (Complex to Real Disabled)		
HB3 FIR + HB2 FIR + HB1 FIR (DCM[1] = 4)	HB4 FIR + HB3 FIR + HB2 FIR + HB1 FIR(DCM[1] = 8)	HB2 FIR + HB1 FIR(DCM[1] = 4)	HB3 FIR + HB2 FIR + HB1 FIR (DCM[1] = 8)	HB4 FIR + HB3 FIR + HB2 FIR + HB1 FIR(DCM[1] = 16)
N	N	N	N	N
N + 1	N + 1	N + 1	N + 1	N + 1
N + 2	N	N + 2	N	N
N + 3	N + 1	N + 3	N + 1	N + 1
N + 4	N + 2	N + 4	N + 2	N
N + 5	N + 3	N + 5	N + 3	N + 1
N + 6	N + 2	N + 6	N + 2	N
N + 7	N + 3	N + 7	N + 3	N + 1

[1] DCM is decimation.

Table 14. DDC Samples, Chip Decimation Ratio = 8

Real (I) Output (Complex to Real Enabled)	Complex (I/Q) Outputs (Complex to Real Disabled)	
HB4 FIR + HB3 FIR + HB2 FIR + HB1 FIR (DCM[1] = 8)	HB3 FIR + HB2 FIR + HB1 FIR(DCM[1] = 8)	HB4 FIR + HB3 FIR + HB2 FIR + HB1 FIR (DCM[1] = 16)
N	N	N
N + 1	N + 1	N + 1
N + 2	N + 2	N
N + 3	N + 3	N + 1
N + 4	N + 4	N + 2
N + 5	N + 5	N + 3
N + 6	N + 6	N + 2
N + 7	N + 7	N + 3

[1] DCM is decimation.

Table 15. DDC Samples, Chip Decimation Ratio = 16

Real (I) Output (Complex to Real Enabled)	Complex (I/Q) Outputs (Complex to Real Disabled)
HB4 FIR + HB3 FIR + HB2 FIR + HB1 FIR (DCM = 16)	HB4 FIR + HB3 FIR + HB2 FIR + HB1 FIR (DCM[1] = 16)
Not applicable	N
Not applicable	N + 1
Not applicable	N + 2
Not applicable	N + 3

[1] DCM is decimation.

DIGITAL DOWNCONVERTERS (DDCS)

If the chip decimation ratio is set to decimate by 4, DDC 0 is set to use HB2 + HB1 filters (complex outputs, decimate by 4), and DDC 1 is set to use HB4 + HB3 + HB2 + HB1 filters (real outputs, decimate by 8). Then, DDC 1 repeats its output data two times for every one DDC 0 output. The resulting output samples are shown in Table 16.

Table 16. DDC Output Samples when Chip DCM[1] = 4, DDC 0 DCM[1] = 4 (Complex), and DDC 1 DCM[1] = 8 (Real)

	DDC 0		DDC 1	
DDC Input Samples	**Output Port I**	**Output Port Q**	**Output Port I**	**Output Port Q**
N N + 1 N + 2 N + 3	I0 (N)	Q0 (N)	I1 (N)	Not applicable
N + 4 N + 5 N + 6 N + 7	I0 (N + 1)	Q0 (N + 1)	I1 (N + 1)	Not applicable
N + 8 N + 9 N + 10 N + 11	I0 (N + 2)	Q0 (N + 2)	I1 (N)	Not applicable
N + 12 N + 13 N + 14 N + 15	I0 (N + 3)	Q0 (N + 3)	I1 (N + 1)	Not applicable

[1] DCM is decimation.

FREQUENCY TRANSLATION

GENERAL DESCRIPTION

Frequency translation is accomplished using a 12-bit complex NCO with a digital quadrature mixer. The frequency translation translates either a real or complex input signal from an IF to a baseband complex digital output (carrier frequency = 0 Hz).

The frequency translation stage of each DDC can be controlled individually and supports four different IF modes using Bits[5:4] of the DDC control registers (Register 0x310, Register 0x330, Register 0x350, and Register 0x370). These IF modes are

- Variable IF mode
- 0 Hz IF, or zero IF (ZIF), mode
- $f_S/4$ Hz IF mode
- Test mode

Variable IF Mode

The NCO and the mixers are enabled. The NCO output frequency can be used to digitally tune the IF frequency.

0 Hz IF (ZIF) Mode

The mixers are bypassed and the NCO is disabled.

$F_S/4$ Hz IF Mode

The mixers and NCO are enabled in a special downmixing by $f_S/4$ mode to save power.

Test Mode

The input samples are forced to 0.999 to positive full scale. The NCO is enabled. This test mode allows the NCOs to drive the decimation filters directly.

Figure 63 and Figure 64 show examples of the frequency translation stage for both real and complex inputs.

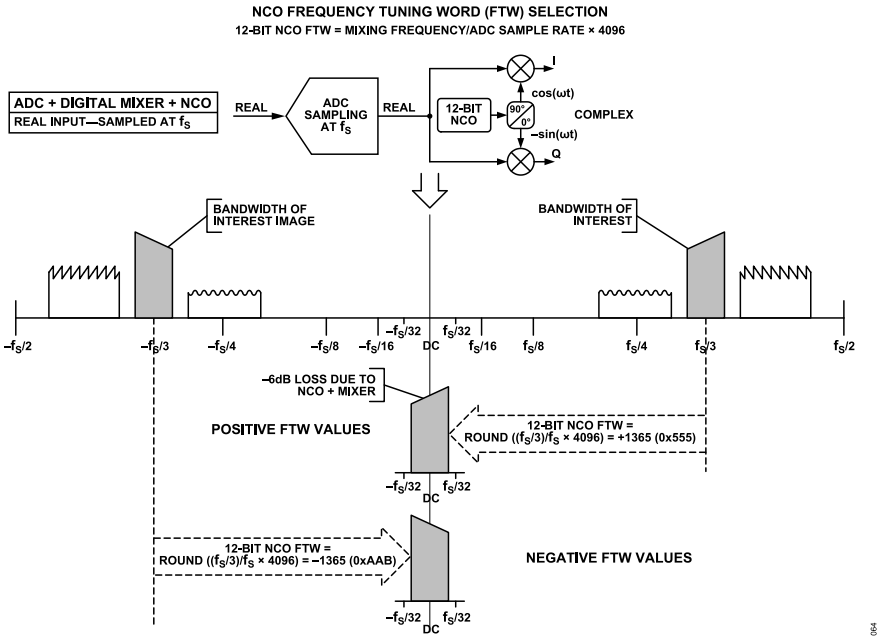

Figure 63. DDC NCO Frequency Tuning Word Selection—Real Inputs

FREQUENCY TRANSLATION

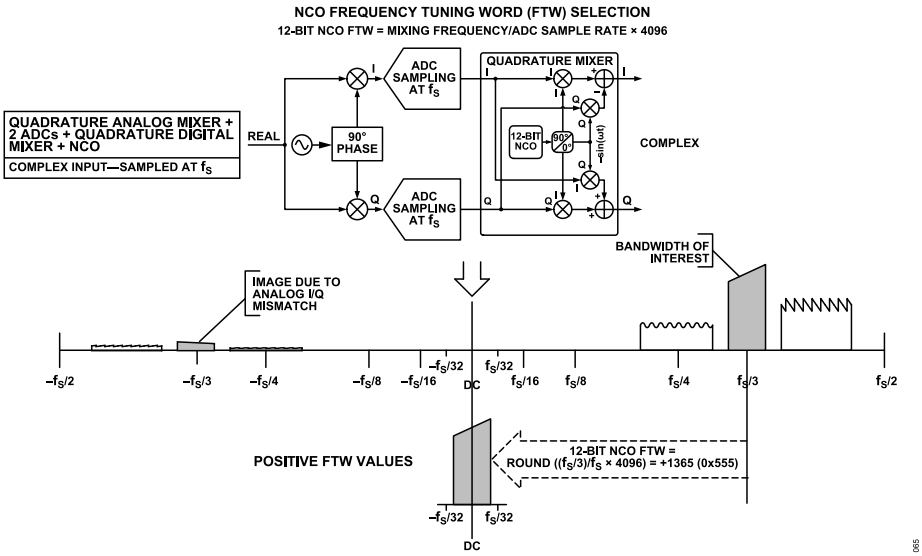

Figure 64. DDC NCO Frequency Tuning Word Selection—Complex Inputs

DDC NCO PLUS MIXER LOSS AND SFDR

When mixing a real input signal down to baseband, 6 dB of loss is introduced in the signal due to filtering of the negative image. The NCO introduces an additional 0.05 dB of loss. The total loss of a real input signal mixed down to baseband is 6.05 dB. For this reason, it is recommended to compensate for this loss by enabling the additional 6 dB of gain in the gain stage of the DDC to recenter the dynamic range of the signal within the full scale of the output bits.

When mixing a complex input signal down to baseband, the maximum value that each I/Q sample can reach is 1.414 × full scale after it passes through the complex mixer. To avoid overrange of the I/Q samples and to keep the data bit-widths aligned with real mixing, introduce 3.06 dB of loss (0.707 × full-scale) in the mixer for complex signals. The NCO introduces an additional 0.05 dB of loss. The total loss of a complex input signal mixed down to baseband is −3.11 dB.

The worst case spurious signal from the NCO is greater than 102 dBc SFDR for all output frequencies.

NUMERICALLY CONTROLLED OSCILLATOR

The AD9691 has a 12-bit NCO for each DDC that enables the frequency translation process. The NCO allows the input spectrum to be tuned to dc, where it can be effectively filtered by the subsequent filter blocks to prevent aliasing. The NCO can be set up by providing a frequency tuning word (FTW) and a phase offset word (POW).

Setting Up the NCO FTW and POW

The NCO frequency value is given by the 12-bit twos complement number entered in the NCO FTW. Frequencies between $\pm f_S$ ($+f_S/2$ excluded) are represented using the following frequency words:

- 0x800 represents a frequency of $-f_S/2$.
- 0x000 represents dc (frequency is 0 Hz).
- 0x7FF represents a frequency of $f_S/2 - f_S/2^{12}$.

Calculate the NCO frequency tuning word using the following equation:

$$NCO_FTW = round\left(2^{12}\frac{mod(f_C, f_S)}{f_S}\right) \quad (1)$$

where:
NCO_FTW is a 12-bit twos complement number representing the NCO FTW.
f_C is the desired carrier frequency in Hz.
f_S is the AD9691 sampling frequency (clock rate) in Hz. mod( ) is a remainder function. For example, mod(110,100) = 10, and for negative numbers, mod(−32, +10) = −2. round( ) is a rounding function. For example, round(3.6) = 4, and for negative numbers, round(−3.4) = −3.

Note that this equation applies to the aliasing of signals in the digital domain (that is, aliasing introduced when digitizing analog signals).

For example, if the ADC sampling frequency (f_S) is 1250 MSPS and the carrier frequency (f_C) is 416.667 MHz,

$$NCO_FTW = round\left(2^{12}\frac{mod(416.667, 1250}{1250}\right) = 1365\text{MHz} \quad (2)$$

FREQUENCY TRANSLATION

This, in turn, converts to 0x555 in the 12-bit twos complement representation for NCO_FTW. Calculate the actual carrier frequency using the following equation:

$$f_{C_ACTUAL} = \frac{NCO_FTW \times f_S}{2^{12}} = 416.56\text{MHz} \quad (3)$$

A 12-bit POW is available for each NCO to create a known phase relationship between multiple AD9691 chips or individual DDC channels inside one AD9691.

The following procedure must be followed to update the FTW and/or POW registers to ensure proper operation of the NCO:

1. Write to the FTW registers for all the DDCs.
2. Write to the POW registers for all the DDCs.
3. Synchronize the NCOs either through the DDC soft reset bit accessible through the SPI, or through the assertion of the SYSREF± pin.

Note that the NCOs must be synchronized either through the SPI or through the SYSREF± pin after all writes to the FTW or POW registers are complete. This synchronization is necessary to ensure the proper operation of the NCO.

NCO Synchronization

Each NCO contains a separate phase accumulator word (PAW) that determines the instantaneous phase of the NCO. The initial reset value of each PAW is determined by the POW described in the Setting Up the NCO FTW and POW section. The phase increment value of each PAW is determined by the FTW.

Use the following two methods to synchronize multiple PAWs within the chip:

- Using the SPI. Use the DDC NCO soft reset bit in the DDC synchronization control register (Register 0x300, Bit 4) to reset all the PAWs in the chip. This is accomplished by toggling the DDC NCO soft reset bit. This method synchronizes DDC channels within the same AD9691 chip only.
- Using the SYSREF± pin. When the SYSREF± pin is enabled in the SYSREF± control registers (Register 0x120 and Register 0x121), and the DDC synchronization is enabled in Bits[1:0] in the DDC synchronization control register (Register 0x300), any subsequent SYSREF± event resets all the PAWs in the chip. This method synchronizes DDC channels within the same AD9691 chip, or DDC channels within separate AD9691 chips.

Mixer

The NCO is accompanied by a mixer, which operates similarly to an analog quadrature mixer. It performs the downconversion of input signals (real or complex) by using the NCO frequency as a local oscillator. For real input signals, this mixer performs a real mixer operation with two multipliers. For complex input signals, the mixer performs a complex mixer operation with four multipliers and two adders. The mixer adjusts its operation based on the input signal (real or complex) provided to each individual channel. The selection of real or complex inputs can be controlled individually for each DDC block by using Bit 7 of the DDC control registers (Register 0x310, Register 0x330, Register 0x350, and Register 0x370).

FIR FILTERS

GENERAL DESCRIPTION

There are four sets of decimate by 2, low-pass, half-band, FIR filters (labeled HB1 FIR, HB2 FIR, HB3 FIR, and HB4 FIR in Figure 61) following the frequency translation stage. After the carrier of interest is tuned down to dc (carrier frequency = 0 Hz), these filters efficiently lower the sample rate while providing sufficient alias rejection from unwanted adjacent carriers around the bandwidth of interest.

HB1 FIR is always enabled and cannot be bypassed. The HB2, HB3, and HB4 FIR filters are optional and can be bypassed for higher output sample rates.

Table 17 shows the different bandwidth options by including different half-band filters. In all cases, the DDC filtering stage of the AD9691 provides less than −0.001 dB of pass-band ripple and greater than 100 dB of stop-band alias rejection.

Table 18 shows the amount of stop-band alias rejection for multiple pass-band ripple/cutoff points. The decimation ratio of the filtering stage of each DDC can be controlled individually through Bits[1:0] of the DDC control registers (Register 0x310, Register 0x330, Register 0x350, and Register 0x370).

Table 17. DDC Filter Characteristics

ADC Sample Rate (MSPS)	DDC Decimation Ratio	Real Output Sample Rate (MSPS)	Complex (I/Q) Output Sample Rate (MSPS)	Alias Protected Bandwidth (MHz)	Ideal SNR Improvement[1] (dB)	Pass-Band Ripple (dB)	Alias Rejection (dB)
1250	2 (HB1)	1250	625 (I) + 625 (Q)	481.3	+1	<−0.001	>100
	4 (HB1 + HB2)	625	312.5 (I) + 312.5 (Q)	240.6	+4		
	8 (HB1 + HB2 + HB3)	312.5	156.25 (I) + 156.25 (Q)	120.3	+7		
	16 (HB1 + HB2 + HB3 + HB4)	156.25	78.125 (I) + 78.125 (Q)	60.2	+10		

[1] The ideal SNR improvement due to oversampling and filtering = 10log(bandwidth/(f_S/2)).

Table 18. DDC Filter Alias Rejection

Alias Rejection (dB)	Pass-Band Ripple/Cutoff Point (dB)	Alias Protected Bandwidth for Real (I) Outputs[1]	Alias Protected Bandwidth for Complex (I/Q) Outputs[1]
>100	<−0.001	<38.5% × f_{OUT}	<77% × f_{OUT}
90	<−0.001	<38.7% × f_{OUT}	<77.4% × f_{OUT}
85	<−0.001	<38.9% × f_{OUT}	<77.8% × f_{OUT}
63.3	<−0.006	<40% × f_{OUT}	<80% × f_{OUT}
25	−0.5	44.4% × f_{OUT}	88.8% × f_{OUT}
19.3	−1.0	45.6% × f_{OUT}	91.2% × f_{OUT}
10.7	−3.0	48% × f_{OUT}	96% × f_{OUT}

[1] f_{OUT} = ADC input sample rate (f_S) ÷ DDC decimation ratio.

FIR FILTERS

HALF-BAND FILTERS

The AD9691 offers four half-band filters to enable digital signal processing of the ADC converted data. These half-band filters are bypassable and can be individually selected.

HB4 Filter

The first decimate by 2, half-band, low-pass FIR filter (HB4) uses an 11-tap, symmetrical, fixed-coefficient filter implementation that is optimized for low power consumption. The HB4 filter is used only when complex outputs (decimate by 16) or real outputs (decimate by 8) are enabled; otherwise, the filter is bypassed. Table 19 and Figure 65 show the coefficients and response of the HB4 filter.

Table 19. HB4 Filter Coefficients

HB4 Coefficient Number	Normalized Coefficient	Decimal Coefficient (15-Bit)
C1, C11	0.006042	99
C2, C10	0	0
C3, C9	−0.049316	−808
C4, C8	0	0
C5, C7	0.293273	4805
C6	0.500000	8192

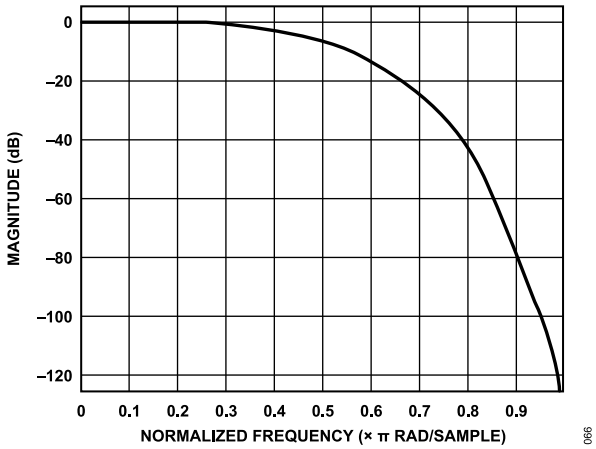

Figure 65. HB4 Filter Response

HB3 Filter

The second decimate by 2, half-band, low-pass, FIR filter (HB3) uses an 11-tap, symmetrical, fixed coefficient filter implementation that is optimized for low power consumption. The HB3 filter is only used when complex outputs (decimate by 8 or 16) or real outputs (decimate by 4 or 8) are enabled; otherwise, the filter is bypassed. Table 20 and Figure 66 show the coefficients and response of the HB3 filter.

Table 20. HB3 Filter Coefficients

HB3 Coefficient Number	Normalized Coefficient	Decimal Coefficient (18-Bit)
C1, C11	0.006554	859
C2, C10	0	0
C3, C9	−0.050819	−6661
C4, C8	0	0
C5, C7	0.294266	38,570
C6	0.500000	65,536

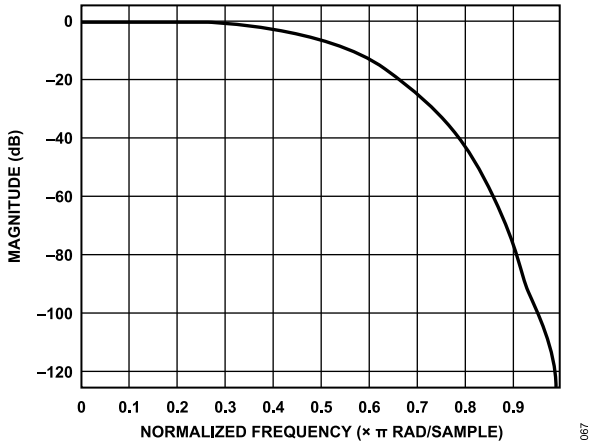

Figure 66. HB3 Filter Response

HB2 Filter

The third decimate by 2, half-band, low-pass FIR filter (HB2) uses a 19-tap, symmetrical, fixed coefficient filter implementation that is optimized for low power consumption. The HB2 filter is only used when complex outputs (decimate by 4, 8, or 16) or real outputs (decimate by 2, 4, or 8) are enabled; otherwise, the filter is bypassed.

Table 21 and Figure 67 show the coefficients and response of the HB2 filter.

Table 21. HB2 Filter Coefficients

HB2 Coefficient Number	Normalized Coefficient	Decimal Coefficient (19-Bit)
C1, C19	0.000614	161
C2, C18	0	0
C3, C17	−0.005066	−1328
C4, C16	0	0
C5, C15	0.022179	5814
C6, C14	0	0
C7, C13	−0.073517	−19,272
C8, C12	0	0
C9, C11	0.305786	80,160
C10	0.500000	131,072

FIR FILTERS

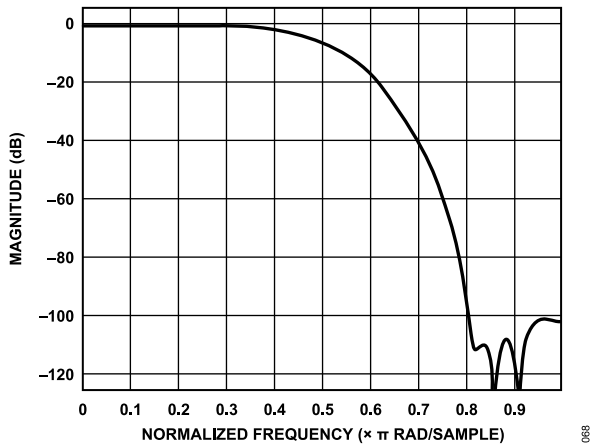

Figure 67. HB2 Filter Response

HB1 Filter

The fourth and final decimate by 2, half-band, low-pass FIR filter (HB1) uses a 55-tap, symmetrical, fixed coefficient filter implementation that is optimized for low power consumption. The HB1 filter is always enabled and cannot be bypassed. Table 22 and Figure 68 show the coefficients and response of the HB1 filter.

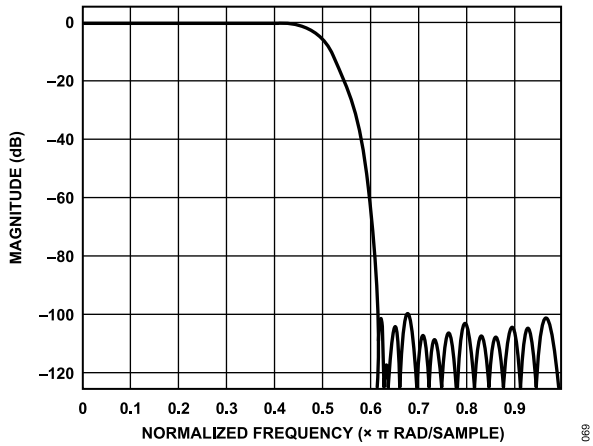

Figure 68. HB1 Filter Response

Table 22. HB1 Filter Coefficients

HB1 Coefficient Number	Normalized Coefficient	Decimal Coefficient (21-Bit)
C1, C55	−0.000023	−24
C2, C54	0	0
C3, C53	0.000097	102
C4, C52	0	0
C5, C51	−0.000288	−302
C6, C50	0	0
C7, C49	0.000696	730
C8, C48	0	0

Table 22. HB1 Filter Coefficients (Continued)

HB1 Coefficient Number	Normalized Coefficient	Decimal Coefficient (21-Bit)
C9, C47	−0.0014725	−1544
C10, C46	0	0
C11, C45	0.002827	2964
C12, C44	0	0
C13, C43	−0.005039	−5284
C14, C42	0	0
C15, C41	0.008491	8903
C16, C40	0	0
C17, C39	−0.013717	−14,383
C18, C38	0	0
C19, C37	0.021591	22,640
C20, C36	0	0
C21, C35	−0.033833	−35,476
C22, C34	0	0
C23, C33	0.054806	57,468
C24, C32	0	0
C25, C31	−0.100557	−105,442
C26, C30	0	0
C27, C29	0.316421	331,792
C28	0.500000	524,288

DDC GAIN STAGE

Each DDC contains an independently controlled gain stage. The gain is selectable as either 0 dB or 6 dB. When mixing a real input signal down to baseband, it is recommended to enable the 6 dB of gain to recenter the dynamic range of the signal within the full scale of the output bits.

When mixing a complex input signal down to baseband, the mixer has already recentered the dynamic range of the signal within the full scale of the output bits and no additional gain is necessary. However, the optional 6 dB gain compensates for low signal strengths. The downsample by 2 portion of the HB1 FIR filter is bypassed when using the complex to real conversion stage (see Figure 69).

DDC COMPLEX TO REAL CONVERSION BLOCK

Each DDC contains an independently controlled complex to real conversion block. The complex to real conversion block reuses the last filter (HB1 FIR) in the filtering stage, along with an $f_S/4$ complex mixer to upconvert the signal.

After upconverting the signal, the Q portion of the complex mixer is no longer needed and is dropped.

Figure 69 shows a simplified block diagram of the complex to real conversion.

FIR FILTERS

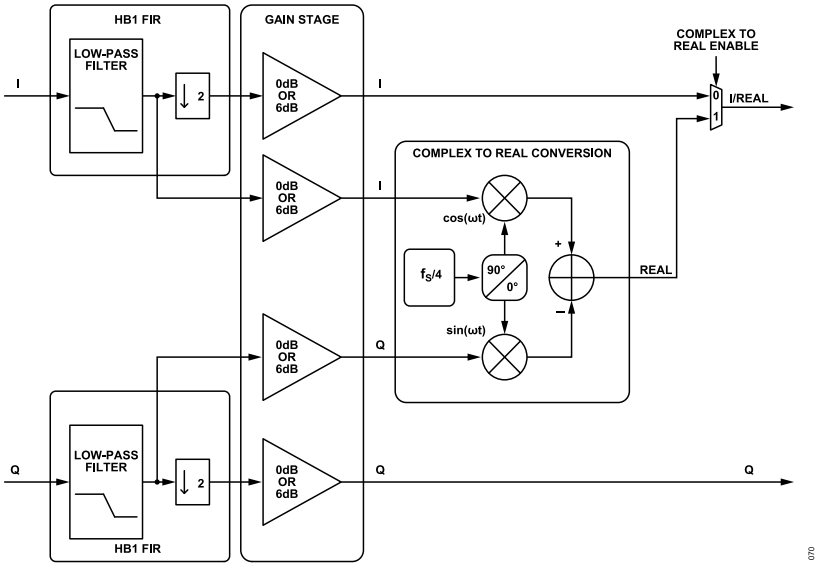

Figure 69. Complex to Real Conversion Block

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DDC EXAMPLE CONFIGURATIONS

Table 23 describes the register settings for multiple DDC example configurations.

Table 23. DDC Example Configurations

Chip Application Layer	Chip Decimation Ratio	DDC Input Type	DDC Output Type	Bandwidth Per DDC[1]	No. of Virtual Converters Required (M)	Register Settings[2]
One DDC	2	Complex	Complex	38.5% × f_S	2	Register 0x200 = 0x01 (one DDC, I/Q selected) Register 0x201 = 0x01 (chip decimate by 2) Register 0x310 = 0x83 (complex mixer, 0 dB gain, variable IF, complex outputs, HB1 filter) Register 0x311 = 0x04 (DDC I input = ADC Channel A, DDC Q input = ADC Channel B) Register 0x314, Register 0x315, Register 0x320, Register 0x321 = FTW and POW set as required by application for DDC 0
Two DDCs	4	Complex	Complex	19.25% × f_S	4	Register 0x200 = 0x02 (two DDCs, I/Q selected) Register 0x201 = 0x02 (chip decimate by 4) Register 0x310, Register 0x330 = 0x80 (complex mixer, 0 dB gain, variable IF, complex outputs, HB2 + HB1 filters) Register 0x311, Register 0x331 = 0x04 (DDC I input = ADC Channel A, DDC Q input = ADC Channel B) Register 0x314, Register 0x315, Register 0x320, Register 0x321 = FTW and POW set as required by application for DDC 0 Register 0x334, Register 0x335, Register 0x340, Register 0x341 = FTW and POW set as required by application for DDC 1
Two DDCs	4	Complex	Real	9.63% × f_S	2	Register 0x200 = 0x22 (two DDCs, I only selected) Register 0x201 = 0x02 (chip decimate by 4) Register 0x310, Register 0x330 = 0x89 (complex mixer, 0 dB gain, variable IF, real output, HB3 + HB2 + HB1 filters) Register 0x311, Register 0x331 = 0x04 (DDC I input = ADC Channel A, DDC Q input = ADC Channel B) Register 0x314, Register 0x315, Register 0x320, Register 0x321 = FTW and POW set as required by application for DDC 0 Register 0x334, Register 0x335, Register 0x340, Register 0x341 = FTW and POW set as required by application for DDC 1
Two DDCs	4	Real	Real	9.63% × f_S	2	Register 0x200 = 0x22 (two DDCs, I only selected) Register 0x201 = 0x02 (chip decimate by 4) Register 0x310, Register 0x330 = 0x49 (real mixer, 6 dB gain, variable IF, real output, HB3 + HB2 + HB1 filters) Register 0x311 = 0x00 (DDC 0 I input = ADC Channel A, DDC 0 Q input = ADC Channel A) Register 0x331 = 0x05 (DDC 1 I input = ADC Channel B, DDC 1 Q input = ADC Channel B) Register 0x314, Register 0x315, Register 0x320, Register 0x321 = FTW and POW set as required by application for DDC 0 Register 0x334, Register 0x335, Register 0x340, Register 0x341 = FTW and POW set as required by application for DDC 1

FIR FILTERS

Table 23. DDC Example Configurations (Continued)

Chip Application Layer	Chip Decimation Ratio	DDC Input Type	DDC Output Type	Bandwidth Per DDC[1]	No. of Virtual Converters Required (M)	Register Settings[2]
Two DDCs	4	Real	Complex	19.25% × f_S	4	Register 0x200 = 0x02 (two DDCs, I/Q selected) Register 0x201 = 0x02 (chip decimate by 4) Register 0x310, 0x330 = 0x40 (real mixer, 6 dB gain, variable IF, complex output, HB2 + HB1 filters) Register 0x311 = 0x00 (DDC 0 I input = ADC Channel A, DDC 0 Q input = ADC Channel A) Register 0x331 = 0x05 (DDC 1 I input = ADC Channel B, DDC 1 Q input = ADC Channel B) Register 0x314, Register 0x315, Register 0x320, Register 0x321 = FTW and POW set as required by application for DDC 0 Register 0x334, Register 0x335, Register 0x340, Register 0x341 = FTW and POW set as required by application for DDC 1
Two DDCs	8	Real	Real	4.81% × f_S	2	Register 0x200 = 0x22 (two DDCs, I only selected) Register 0x201 = 0x03 (chip decimate by 8) Register 0x310, Register 0x330 = 0x4A (real mixer, 6 dB gain, variable IF, real output, HB4 + HB3 + HB2 + HB1 filters) Register 0x311 = 0x00 (DDC 0 I input = ADC Channel A, DDC 0 Q input = ADC Channel A) Register 0x331 = 0x05 (DDC 1 I input = ADC Channel B, DDC 1 Q input = ADC Channel B) Register 0x314, Register 0x315, Register 0x320, Register 0x321 = FTW and POW set as required by application for DDC 0 Register 0x334, Register 0x335, Register 0x340, Register 0x341 = FTW and POW set as required by application for DDC 1
Four DDCs	8	Real	Complex	9.63% × f_S	8	Register 0x200 = 0x03 (four DDCs, I/Q selected) Register 0x201 = 0x03 (chip decimate by 8) Register 0x310, Register 0x330, Register 0x350, Register 0x370 = 0x41 (real mixer, 6 dB gain, variable IF, complex output, HB3 + HB2 + HB1 filters) Register 0x311 = 0x00 (DDC 0 I input = ADC Channel A, DDC 0 Q input = ADC Channel A) Register 0x331 = 0x00 (DDC 1 I input = ADC Channel A, DDC 1 Q input = ADC Channel A) Register 0x351 = 0x05 (DDC 2 I input = ADC Channel B, DDC 2 Q input = ADC Channel B) Register 0x371 = 0x05 (DDC 3 I input = ADC Channel B, DDC 3 Q input = ADC Channel B) Register 0x314, Register 0x315, Register 0x320, Register 0x321 = FTW and POW set as required by application for DDC 0 Register 0x334, Register 0x335, Register 0x340, Register 0x341 = FTW and POW set as required by application for DDC 1 Register 0x354, Register 0x355, Register 0x360, Register 0x361 = FTW and POW set as required by application for DDC 2

FIR FILTERS

Table 23. DDC Example Configurations (Continued)

Chip Application Layer	Chip Decimation Ratio	DDC Input Type	DDC Output Type	Bandwidth Per DDC[1]	No. of Virtual Converters Required (M)	Register Settings[2]
						Register 0x374, Register 0x375, Register 0x380, Register 0x381 = FTW and POW set as required by application for DDC 3
Four DDCs	8	Real	Real	4.81% × f_S	4	Register 0x200 = 0x23 (four DDCs, I only selected) Register 0x201 = 0x03 (chip decimate by 8) Register 0x310, Register 0x330, Register 0x350, Register 0x370 = 0x4A (real mixer, 6 dB gain, variable IF, real output, HB4 + HB3 + HB2 + HB1 filters) Register 0x311 = 0x00 (DDC 0 I input = ADC Channel A, DDC 0 Q input = ADC Channel A) Register 0x331 = 0x00 (DDC 1 I input = ADC Channel A, DDC 1 Q input = ADC Channel A) Register 0x351 = 0x05 (DDC 2 I input = ADC Channel B, DDC 2 Q input = ADC Channel B) Register 0x371 = 0x05 (DDC 3 I input = ADC Channel B, DDC 3 Q input = ADC Channel B) Register 0x314, Register 0x315, Register 0x320, Register 0x321 = FTW and POW set as required by application for DDC 0 Register 0x334, Register 0x335, Register 0x340, Register 0x341 = FTW and POW set as required by application for DDC 1 Register 0x354, Register 0x355, Register 0x360, Register 0x361 = FTW and POW set as required by application for DDC 2 Register 0x374, Register 0x375, Register 0x380, Register 0x381 = FTW and POW set as required by application for DDC 3
Four DDCs	16	Real	Complex	4.81% × f_S	8	Register 0x200 = 0x03 (four DDCs, I/Q selected) Register 0x201 = 0x04 (chip decimate by 16) Register 0x310, Register 0x330, Register 0x350, Register 0x370 = 0x42 (real mixer, 6 dB gain, variable IF, complex output, HB4 + HB3 + HB2 + HB1 filters) Register 0x311 = 0x00 (DDC 0 I input = ADC Channel A, DDC 0 Q input = ADC Channel A) Register 0x331 = 0x00 (DDC 1 I input = ADC Channel A, DDC 1 Q input = ADC Channel A) Register 0x351 = 0x05 (DDC 2 I input = ADC Channel B, DDC 2 Q input = ADC Channel B) Register 0x371 = 0x05 (DDC 3 I input = ADC Channel B, DDC 3 Q input = ADC Channel B) Register 0x314, Register 0x315, Register 0x320, Register 0x321 = FTW and POW set as required by application for DDC 0. Register 0x334, Register 0x335, Register 0x340, Register 0x341 = FTW and POW set as required by application for DDC 1 Register 0x354, Register 0x355, Register 0x360, Register 0x361 = FTW and POW set as required by application for DDC 2

FIR FILTERS

Table 23. DDC Example Configurations (Continued)

Chip Application Layer	Chip Decimation Ratio	DDC Input Type	DDC Output Type	Bandwidth Per DDC[1]	No. of Virtual Converters Required (M)	Register Settings[2]
						Register 0x374, Register 0x375, Register 0x380, Register 0x381 = FTW and POW set as required by application for DDC 3

[1] f_S is the ADC sample rate. Bandwidths listed are <−0.001 dB of pass-band ripple and >100 dB of stop-band alias rejection.

[2] The NCOs must be synchronized either through the SPI or through the SYSREF± pin after all writes to the FTW or POW registers have completed. This is necessary to ensure the proper operation of the NCO. See the NCO Synchronization section for more information.

DIGITAL OUTPUTS

INTRODUCTION TO THE JESD204B INTERFACE

The AD9691 digital outputs are designed to the JEDEC Standard JESD204B serial interface for data converters. JESD204B is a protocol to link the AD9691 to a digital processing device over a serial interface with lane rates of up to 10 Gbps. The benefits of the JESD204B interface over the LVDS interface include a reduction in required board area for data interface routing, and an ability to enable smaller packages for converter and logic devices.

JESD204B OVERVIEW

The JESD204B data transmit block assembles the parallel data from the ADC into frames and uses 8B/10B encoding as well as optional scrambling to form serial output data. Lane synchronization is supported through the use of special control characters during the initial establishment of the link. Additional control characters are embedded in the data stream to maintain synchronization thereafter. A JESD204B receiver is required to complete the serial link. For additional details on the JESD204B interface, refer to the JESD204B standard.

The AD9691 JESD204B data transmit block maps up to two physical ADCs or up to eight virtual converters (when DDCs are enabled) over a link. A link can be configured to use one, two, or four JESD204B lanes. The JESD204B specification refers to a number of parameters to define the link, and these parameters must match between the JESD204B transmitter (the AD9691 output) and the JESD204B receiver (the logic device input).

The JESD204B link is described according to the following parameters:

- L is the number of lanes per converter device (lanes per link) (AD9691 value = 1, 2, or 4)
- M is the number of converters per converter device (virtual converters per link) (AD9691 value = 1, 2, 4, or 8)
- F is the octets per frame (AD9691 value = 1, 2, 4, 8, or 16)
- N′ is the number of bits per sample (JESD204B word size) (AD9691 value = 8 or 16)
- N is the converter resolution (AD9691 value = 7 to 16)
- CS is the number of control bits per sample (AD9691 value = 0 to 3)
- K is the number of frames per multiframe (AD9691 value = 4, 8, 12, 16, 20, 24, 28, or 32)
- S is the samples transmitted per single converter per frame cycle (AD9691 value = set automatically based on L, M, F, and N′)
- HD is the high density mode (AD9691 value = set automatically based on L, M, F, and N′)
- CF is the number of control words per frame clock cycle per converter device (AD9691 value = 0)

Figure 70 shows a simplified block diagram of the AD9691 JESD204B link. By default, the AD9691 is configured to use two converters and four lanes. Converter A data is output to SERDOUT0±, SERDOUT1±, SERDOUT2±, and SERDOUT3±, and Converter B data is output to SERDOUT4±, SERDOUT5±, SERDOUT6±, and SERDOUT7±. The AD9691 allows other configurations such as combining the outputs of both converters onto a single lane, or changing the mapping of the Converter A and Converter B digital output paths. These modes are set up via a quick configuration register in the SPI register map, along with additional customizable options.

By default in the AD9691, the 14-bit converter word from each converter is broken into two octets (eight bits of data). Bit 13 (MSB) through Bit 6 are in the first octet. The second octet contains Bit 5 through Bit 0 (LSB) and two tail bits. The tail bits can be configured as zeros or a pseudorandom number (PN) sequence. The tail bits can also be replaced with control bits indicating overrange, SYSREF±, signal monitor, or fast detect output.

The two resulting octets can be scrambled. Scrambling is optional; however, it is recommended to avoid spectral peaks when transmitting similar digital data patterns. The scrambler uses a self synchronizing, polynomial-based algorithm defined by the equation $1 + x^{14} + x^{15}$. The descrambler in the receiver is a self synchronizing version of the scrambler polynomial.

The two octets are then encoded with an 8B/10B encoder. The 8B/10B encoder takes eight bits of data (an octet) and encodes them into a 10-bit symbol. Figure 71 shows how the 14-bit data is taken from the ADC, the tail bits are added, the two octets are scrambled, and how the octets are encoded into two 10-bit symbols. Figure 71 illustrates the default data framing.

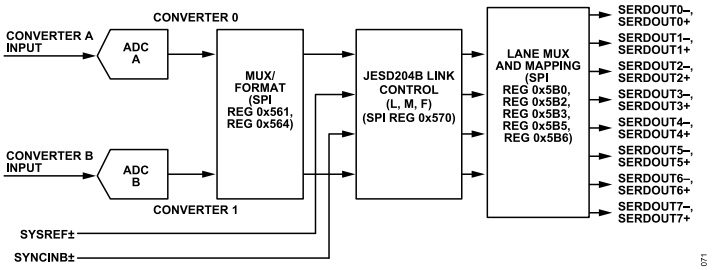

Figure 70. Transmit Link Simplified Block Diagram Showing Full Bandwidth Mode (Register 0x200 = 0x00)

DIGITAL OUTPUTS

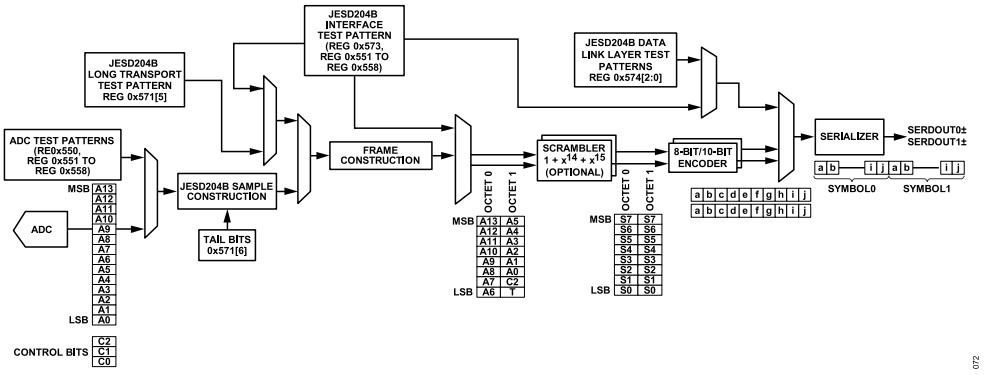

Figure 71. ADC Output Datapath Showing Data Framing

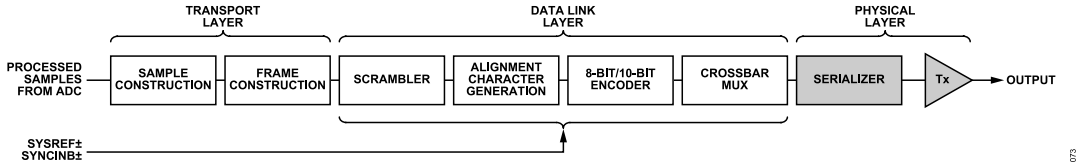

Figure 72. Data Flow

FUNCTIONAL OVERVIEW

The block diagram in Figure 72 shows the flow of data through the JESD204B hardware from the sample input to the physical output. The processing can be divided into layers that are derived from the open-source initiative (OSI) model widely used to describe the abstraction layers of communications systems. These layers are the transport layer, the data link layer, and the physical layer, which includes the serializer and output driver).

Transport Layer

The transport layer handles packing the data (consisting of samples and optional control bits) into JESD204B frames that are mapped to 8-bit octets. These octets are sent to the data link layer. The transport layer mapping is controlled by rules derived from the link parameters. Tail bits are added to fill gaps where required. The following equation can be used to determine the number of tail bits within a sample (JESD204B word):

$$T = N' - N - CS$$

Data Link Layer

The data link layer manages the low level functions of passing data across the link. These functions include optionally scrambling the data, inserting control characters for multichip synchronization/lane alignment/monitoring, encoding 8-bit octets into 10-bit symbols, and remapping data using the crossbar mux. The data link layer is also responsible for sending the initial lane alignment sequence (ILAS), which contains the link configuration data used by the receiver to verify the settings in the transport layer.

Physical Layer

The physical layer consists of the high speed circuitry clocked at the serial clock rate. In this layer, parallel data is converted into one, two, or four lanes of high speed differential serial data.

JESD204B LINK ESTABLISHMENT

The AD9691 JESD204B transmitter (Tx) interface operates in Subclass 1 as defined in the JEDEC Standard JESD204B (July 2011 specification). The link establishment process is divided into the following steps: code group synchronization and SYNCINB±, initial lane alignment sequence, and user data and error correction.

Code Group Synchronization (CGS) and SYNCINB±

The CGS is the process by which the JESD204B receiver finds the boundaries between the 10-bit symbols in the stream of data. During the CGS phase, the JESD204B transmit block transmits the /K28.5/ characters. The receiver must locate the /K28.5/ characters in its input data stream using clock and data recovery (CDR) techniques.

The receiver issues a synchronization request by asserting the SYNCINB± pin of the AD9691 low. The JESD204B Tx then begins sending /K/ characters. After the receiver is synchronized, it waits for the correct reception of at least four consecutive /K/ symbols. It then deasserts SYNCINB±. The AD9691 then transmits an ILAS on the following local multiframe clock (LMFC) boundary.

For more information on the code group synchronization phase, refer to the JEDEC Standard JESD204B, July 2011, Section 5.3.3.1.

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The SYNCINB± pin operation can also be controlled by the SPI. The SYNCINB± signal is a differential LVDS mode signal by default, but it can also be driven single-ended. For more information on configuring the SYNCINB± pin operation,see Register 0x572 in Table 35.

Initial Lane Alignment Sequence (ILAS)

The ILAS phase follows the CGS phase and begins on the next LMFC boundary. The ILAS consists of four multiframes, with an /R/ character marking the beginning and an /A/ character marking the end. The ILAS begins by sending an /R/ character followed by 0 to 255 ramp data for one multiframe. On the second multiframe, the link configuration data is sent, starting with the third character. The second character is a /Q/ character to confirm that the link configuration data follows. All undefined data slots are filled with ramp data. The ILAS sequence is never scrambled.

The ILAS sequence construction is shown in Figure 73. The four multiframes include the following:

- Multiframe 1, which begins with an /R/ character (/K28.0/) and ends with an /A/ character (/K28.3/).
- Multiframe 2, which begins with an /R/ character followed by a /Q/ (/K28.4/) character, followed by link configuration parameters over 14 configuration octets (see Table 24) and ends with an /A/ character. Many of the parameter values are of the value –1 notation.
- Multiframe 3, which begins with an /R/ character (/K28.0/) and ends with an /A/ character (/K28.3/).
- Multiframe 4, which begins with an /R/ character (/K28.0/) and ends with an /A/ character (/K28.3/).

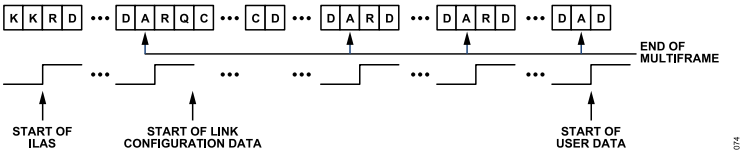

Figure 73. Initial Lane Alignment Sequence

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User Data and Error Detection

After the initial lane alignment sequence is complete, the user data is sent. Normally, all characters within a frame are considered user data. However, to monitor the frame clock and multiframe clock synchronization, there is a mechanism for replacing characters with /F/ or /A/ alignment characters when the data meets certain conditions. These conditions are different for unscrambled and scrambled data. The scrambling operation is enabled by default, but it can be disabled using the SPI.

For scrambled data, any 0xFC character at the end of a frame is replaced by an /F/ character, and any 0x7C character at the end of a multiframe is replaced with an /A/ character. The JESD204B receiver (Rx) checks for /F/ and /A/ characters in the received data stream and verifies that they only occur in the expected locations. If an unexpected /F/ or /A/ character is found, the receiver handles the situation by using dynamic realignment or asserting the SYNCINB± signal for more than four frames to initiate a resynchronization. For unscrambled data, when the final character of two subsequent frames is equal, the second character is replaced with an /F/ character if it is at the end of a frame, and an /A/ character if it is at the end of a multiframe.

Insertion of alignment characters can be modified using the SPI. The frame alignment character insertion (FACI) is enabled by default. For more information on the link controls, see the Memory Map section, Register 0x571.

8B/10B Encoder

The 8B/10B encoder converts 8-bit octets into 10-bit symbols and inserts control characters into the stream when needed. The control characters used in JESD204B are shown in Table 24. The 8B/10B encoding ensures that the signal is dc balanced by using the same number of ones and zeros across multiple symbols.

The 8B/10B interface has options that can be controlled via the SPI. These operations include bypass and invert. These options are intended to be troubleshooting tools for the verification of the digital front end (DFE). See the Memory Map section, Register 0x572, Bits[2:1] for information on configuring the 8B/10B encoder.

Table 24. AD9691 Control Characters Used in JESD204B

Abbreviation	Control Symbol	8-Bit Value	10-Bit Value, RD[1] = −1	10-Bit Value, RD[1] = +1	Description
/R/	/K28.0/	000 11100	001111 0100	110000 1011	Start of multiframe
/A/	/K28.3/	011 11100	001111 0011	110000 1100	Lane alignment
/Q/	/K28.4/	100 11100	001111 0010	110000 1101	Start of link configuration data
/K/	/K28.5/	101 11100	001111 1010	110000 0101	Group synchronization
/F/	/K28.7/	111 11100	001111 1000	110000 0111	Frame alignment

[1] RD means running disparity.

DIGITAL OUTPUTS

PHYSICAL LAYER (DRIVER) OUTPUTS

Digital Outputs, Timing, and Controls

The AD9691 physical layer consists of drivers that are defined in the JEDEC Standard JESD204B (July 2011). The differential digital outputs are powered up by default. The drivers use a dynamic 100 Ω internal termination to reduce unwanted reflections.

Place a 100 Ω differential termination resistor at each receiver, which results in a nominal 300 mV p-p swing at the receiver (see Figure 74). It is recommended to use ac coupling to connect the AD9691 serializer/deserializer (SERDES) outputs to the receiver.

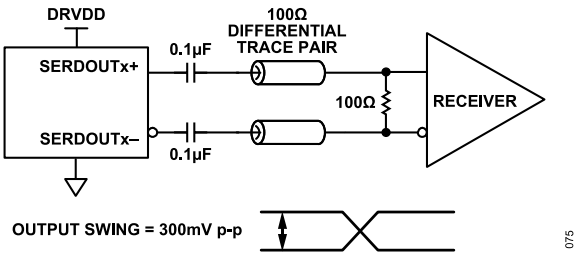

Figure 74. AC-Coupled Digital Output Termination Example

If there is no far end receiver termination, or if there is poor differential trace routing, timing errors may result. To avoid such timing errors, it is recommended that the trace length be less than six inches, and that the differential output traces be close together and at equal lengths.

Figure 75 to Figure 77 show examples of the digital output data eye, time interval error (TIE) jitter histogram, and bathtub curve, respectively, for one AD9691 lane running at 6 Gbps. The format of the output data is twos complement by default. To change the output data format, see the Memory Map section (Register 0x561 in Table 35).

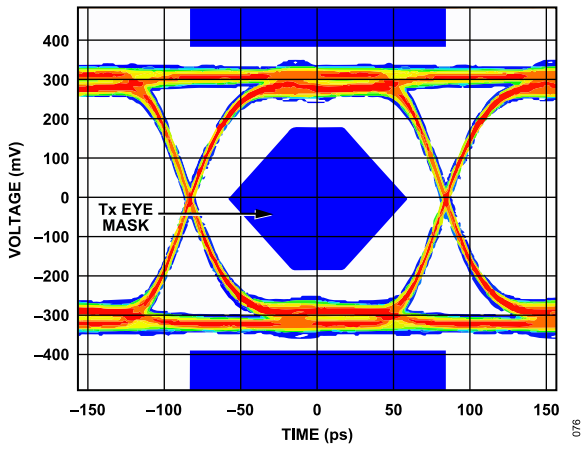

Figure 75. Digital Outputs Data Eye, External 100 Ω Terminations at 6 Gbps

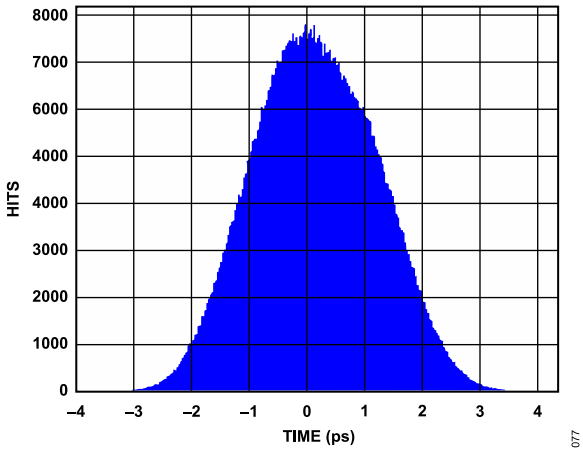

Figure 76. Digital Outputs Histogram, External 100 Ω Terminations at 6 Gbps

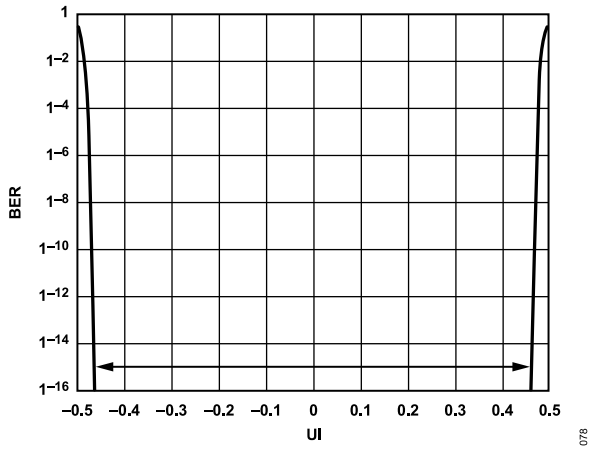

Figure 77. Digital Outputs Bathtub Curve, External 100 Ω Terminations at 6 Gbps

De-Emphasis

De-emphasis enables the receiver eye diagram mask to be met in conditions where the interconnect insertion loss does not meet the JESD204B specification. Use the de-emphasis feature only when the receiver cannot recover the clock due to excessive insertion loss. Under normal conditions, it is disabled to conserve power. Additionally, enabling and setting too high a de-emphasis value on a short link may cause the receiver eye diagram to fail. Use the de-emphasis setting with caution because it may increase electromagnetic interference (EMI). See the Memory Map section (Register 0x5C1 to Register 0x5C5 in Table 35) for more details.

Phase-Locked Loop (PLL)

The PLL generates the serializer clock, which operates at the JESD204B lane rate. The JESD204B lane rate in Register 0x56E, Bit 4 must be set to correspond with the lane rate.

DIGITAL OUTPUTS

CONFIGURING THE JESD204B LINK

The AD9691 has one JESD204B link. The device offers an easy way to set up the JESD204B link through the quick configuration register (Register 0x570). The serial outputs (SERDOUT0± to SERDOUT3±) are considered to be part of one JESD204B link. The basic parameters that determine the link setup are

- Number of lanes per link (L)
- Number of converters per link (M)
- Number of octets per frame (F)

The maximum lane rate allowed by the JESD204B specification is 12.5 Gbps. The lane rate is related to the JESD204B parameters using the following equation:

$$Lane \quad Rate = \frac{M \times N' \times \left(\frac{10}{8}\right) \times f_{OUT}}{L} \tag{4}$$

where $f_{OUT} = f_{ADC_CLOCK} \div$ *Chip decimation ratio.*

Use the following steps to configure the output:

1. Power down the link.
2. Select the quick configuration options.
3. Configure the detailed options.
4. Set the output lane mapping (optional).
5. Set additional driver configuration options (optional).
6. Power up the link.

If the lane rate calculated is less than 6.25 Gbps, select the low lane rate option. This is done by programming a value of 0x10 to Register 0x56E.

Table 25 and Table 26 show the JESD204B output configurations supported for both N′ = 16 and N′ = 8 for a given number of virtual converters. Take care to ensure that the serial lane rate for a given configuration is within the supported range of 3.125 Gbps to 12.5 Gbps.

Table 25. JESD204B Output Configurations for N′ = 16

Number of Virtual Converters Supported (Same Value as M)	JESD204B Quick Configuration (Register 0x570)	JESD204B Serial Lane Rate[1]	JESD204B Transport Layer Settings[2]								
			L	M	F	S	HD	N	N'	CS	K[3]
1	0x01	20 × f_{OUT}	1	1	2	1	0	8 to 16	16	0 to 3	Only valid K values that are divisible by 4 are supported
	0x40	10 × f_{OUT}	2	1	1	1	1	8 to 16	16	0 to 3	
	0x41	10 × f_{OUT}	2	1	2	2	0	8 to 16	16	0 to 3	
	0x80	5 × f_{OUT}	4	1	1	2	1	8 to 16	16	0 to 3	
	0x81	5 × f_{OUT}	4	1	2	4	0	8 to 16	16	0 to 3	
	0xC0	2.5 × f_{OUT}	8	1	1	4	1	8 to 16	16	0 to 3	
	0xC1	2.5 × f_{OUT}	8	1	2	8	0	8 to 16	16	0 to 3	
2	0x0A	40 × f_{OUT}	1	2	4	1	0	8 to 16	16	0 to 3	
	0x49	20 × f_{OUT}	2	2	2	1	0	8 to 16	16	0 to 3	
	0x88	10 × f_{OUT}	4	2	1	1	1	8 to 16	16	0 to 3	
	0x89	10 × f_{OUT}	4	2	2	2	0	8 to 16	16	0 to 3	
	0xC8	5 × f_{OUT}	8	2	1	2	1	8 to 16	16	0 to 3	
	0xC9	5 × f_{OUT}	8	2	2	4	0	8 to 16	16	0 to 3	
4	0x13	80 × f_{OUT}	1	4	8	1	0	8 to 16	16	0 to 3	
	0x52	40 × f_{OUT}	2	4	4	1	0	8 to 16	16	0 to 3	
	0x91	20 × f_{OUT}	4	4	2	1	0	8 to 16	16	0 to 3	
	0xD0	10 × f_{OUT}	8	4	1	1	1	8 to 16	16	0 to 3	
	0xD1	10 × f_{OUT}	8	4	2	2	0	8 to 16	16	0 to 3	
8	0x1C	160 × f_{OUT}	1	8	16	1	0	8 to 16	16	0 to 3	
	0x5B	80 × f_{OUT}	2	8	8	1	0	8 to 16	16	0 to 3	
	0x9A	40 × f_{OUT}	4	8	4	1	0	8 to 16	16	0 to 3	
	0xD9	20 × f_{OUT}	8	8	2	1	0	8 to 16	16	0 to 3	

[1] f_{OUT} = output sample rate = $f_{ADC_CLOCK} \div$ chip decimation ratio. The JESD204B serial lane rate must be ≥3.125 Gbps and ≤12.5 Gbps; when the serial lane rate is ≤12.5 Gbps and ≥6.25 Gbps, the low lane rate mode must be disabled (set Bit 4 to 0x0 in Register 0x56E). When the serial lane rate is <6.25 Gbps and ≥3.125 Gbps, the low lane rate mode must be enabled (set Bit 4 to 0x1 in Register 0x56E).

[2] The JESD204B transport layer descriptions are as described in the JESD204B Overview section.

[3] For F = 1, K = 20, 24, 28, and 32. For F = 2, K = 12, 16, 20, 24, 28, and 32. For F = 4, K = 8, 12, 16, 20, 24, 28, and 32. For F = 8 and F = 16, K = 4, 8, 12, 16, 20, 24, 28, and 32.

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Table 26. JESD204B Output Configurations for N'= 8

Number of Virtual Converters Supported (Same Value as M)	JESD204B Quick Configuration (Register 0x570)	JESD204B Serial Lane Rate[1]	JESD204B Transport Layer Settings[2]								
			L	M	F	S	HD	N	N'	CS	K[3]
1	0x00	10 × f_{OUT}	1	1	1	1	0	7 to 8	8	0 to 1	Only valid K values which are divisible by 4 are supported
	0x01	10 × f_{OUT}	1	1	2	2	0	7 to 8	8	0 to 1	
	0x40	5 × f_{OUT}	2	1	1	2	0	7 to 8	8	0 to 1	
	0x41	5 × f_{OUT}	2	1	2	4	0	7 to 8	8	0 to 1	
	0x42	5 × f_{OUT}	2	1	4	8	0	7 to 8	8	0 to 1	
	0x80	2.5 × f_{OUT}	4	1	1	4	0	7 to 8	8	0 to 1	
	0x81	2.5 × f_{OUT}	4	1	2	8	0	7 to 8	8	0 to 1	
2	0x09	20 × f_{OUT}	1	2	2	1	0	7 to 8	8	0 to 1	
	0x48	10 × f_{OUT}	2	2	1	1	0	7 to 8	8	0 to 1	
	0x49	10 × f_{OUT}	2	2	2	2	0	7 to 8	8	0 to 1	
	0x88	5 × f_{OUT}	4	2	1	2	0	7 to 8	8	0 to 1	
	0x89	5 × f_{OUT}	4	2	2	4	0	7 to 8	8	0 to 1	
	0x8A	5 × f_{OUT}	4	2	4	8	0	7 to 8	8	0 to 1	

1 f_{OUT} = output sample rate = f_{ADC_CLOCK} ÷ chip decimation ratio. The JESD204B serial lane rate must be ≥3125 Mbps and ≤12.5 Gbps; when the serial lane rate is ≤12.5 Gbps and ≥6.25 Gbps, the low lane rate mode must be disabled (set Bit 4 to 0x0 in Register 0x56E). When the serial lane rate is <6.25 Gbps and ≥3.125 Gbps, the low lane rate mode must be enabled (set Bit 4 to 0x1 in Register 0x56E).

2 The JESD204B transport layer descriptions are as described in the JESD204B Overview section.

3 For F = 1, K = 20, 24, 28, and 32. For F = 2, K = 12, 16, 20, 24, 28, and 32. For F = 4, K = 8, 12, 16, 20, 24, 28, and 32. For F = 8 and F = 16, K = 4, 8, 12, 16, 20, 24, 28, and 32.

See the Example 1: Full Bandwidth Mode section and the Example 2: ADC With DDC Option (Two ADCs Plus Two DDCs) section for two examples describing which JESD204B transport layer settings are valid for a given chip mode.

Example 1: Full Bandwidth Mode

The chip application mode is full bandwidth mode (see Figure 78), and includes the following:

- Two 14-bit converters at 1250 MSPS
- Full bandwidth application layer mode
- No decimation

The JESD204B output configuration includes the following:

- Two virtual converters required (see Table 25)
- Output sample rate (f_{OUT}) = 1250/1 = 1250 MSPS

The JESD204B supported output configurations (see Table 25) include

- N′ = 16 bits
- N = 14 bits
- L = 8, M = 2, and F = 1, or L = 4, M = 2, and F = 1 (quick configuration = 0xC8 or 0x88)
- CS = 0 to 2
- K = 32
- Output serial lane rate = 6.25 Gbps per lane for L = 8; output serial lane rate = 12.5 Gbps per lane for L = 4; low lane rate mode disabled

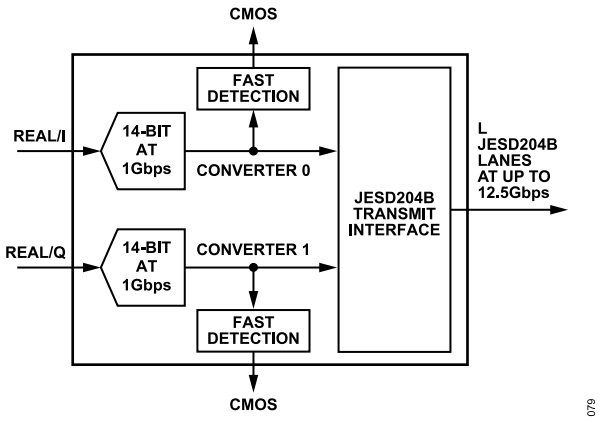

Figure 78. Full Bandwidth Mode

Example 2: ADC With DDC Option (Two ADCs Plus Two DDCs)

The chip application mode is two-DDC mode (see Figure 79), and includes the following:

- Two 14-bit converters at 1.25 GSPS
- Two-DDC application layer mode with complex outputs (I/Q)
- Chip decimation ratio = 2

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- DDC decimation ratio = 2 (see Table 35)

The JESD204B output configuration includes the following:

- Virtual converters required = 4 (see Table 25)
- Output sample rate (f_{OUT}) = 1250/2 = 625 MSPS

The JESD204B supported output configurations include (see Table 25)

- N′ = 16 bits
- N = 14 bits
- L = 4, M = 4, and F = 2 (quick configuration = 0x91)
- CS = 0 to 1
- K = 32
- Output serial lane rate = 10 Gbps per lane (L = 4)
- Low lane rate mode is disabled (0x56E = 0x00)

Example 2 shows the flexibility in the digital and lane configurations for the AD9691. The sample rate is 1.25 GSPS, but the outputs are all combined in either one or two lanes, depending on the input/output speed capability of the receiving device.

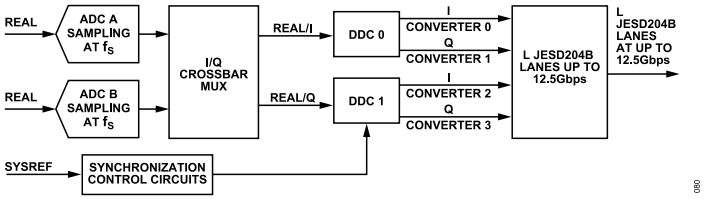

Figure 79. Two-ADC Plus Two-DDC Mode

MULTICHIP SYNCHRONIZATION

The AD9691 has a SYSREF± input that allows flexible options for synchronizing the internal blocks. The SYSREF± input is a source synchronous system reference signal that enables multichip synchronization. The input clock divider, DDCs, signal monitor block, and JESD204B link can be synchronized using the SYSREF± input. For the highest level of timing accuracy, SYSREF± must meet setup and hold requirements relative to the CLK± input.

The flowchart in Figure 80 describes the internal mechanism by which multichip synchronization can be achieved in the AD9691.

The AD9691 supports several features that aid users in meeting the requirements for capturing a SYSREF± signal. The SYSREF± sample event can be defined as either a synchronous low to high transition, or synchronous high to low transition. Additionally, the AD9691 allows the SYSREF± signal to be sampled using either the rising edge or falling edge of the CLK± input. The AD9691 also can ignore a programmable number (up to 16) of SYSREF± events. The SYSREF± control options can be selected using Register 0x120 and Register 0x121.

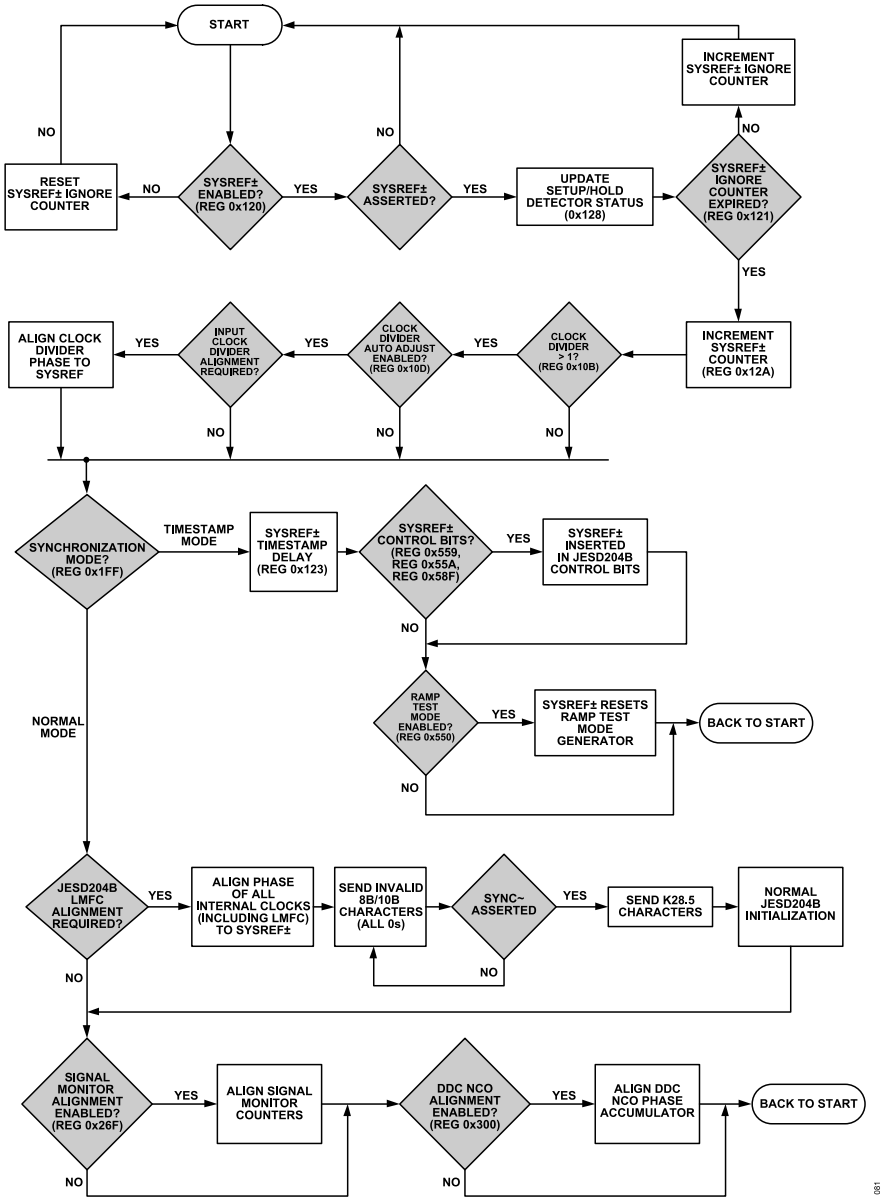

Figure 80. Multichip Synchronization

MULTICHIP SYNCHRONIZATION

SYSREF± SETUP/HOLD WINDOW MONITOR

To assist in ensuring a valid SYSREF± signal capture, the AD9691 has a SYSREF± setup/hold window monitor. This feature allows the system designer to determine the location of the SYSREF± signals relative to the CLK± signals by reading back the amount of setup/hold margin on the interface through the memory map.

Figure 81 and Figure 82 show the setup and hold status values for different phases of SYSREF±. The setup detector returns the status of the SYSREF± signal before the CLK± edge and the hold detector returns the status of the SYSREF± signal after the CLK± edge. Register 0x128 stores the status of SYSREF± and alerts the user if the SYSREF± signal is captured by the ADC.

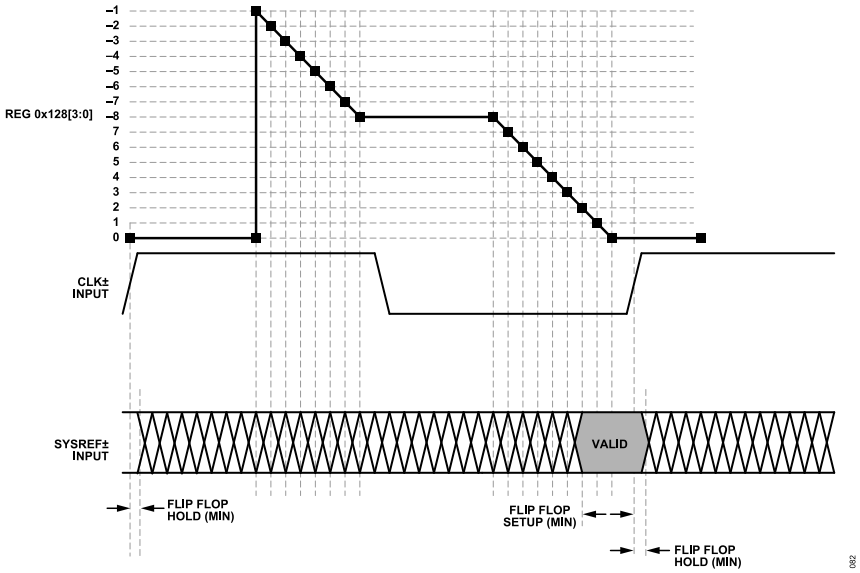

Figure 81. SYSREF± Setup Detector

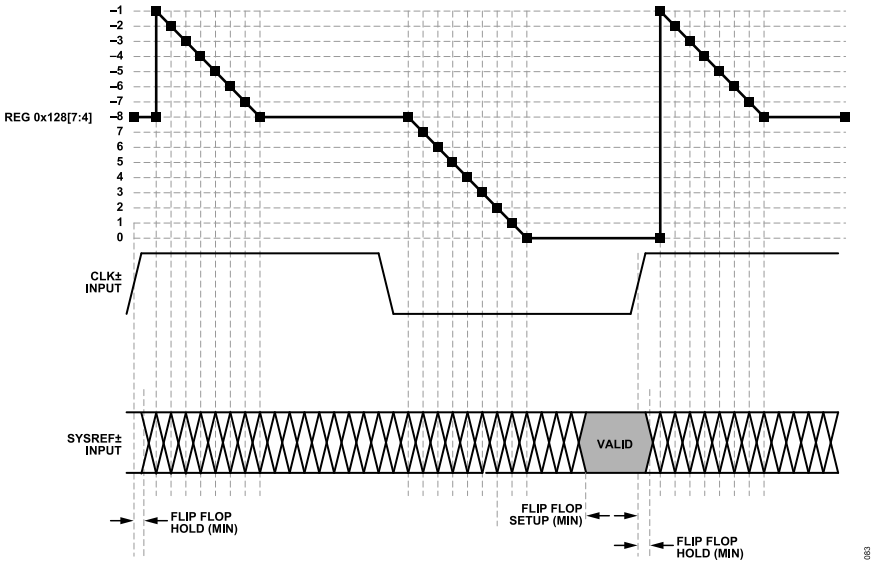

Figure 82. SYSREF± Hold Detector

Table 27 shows the description of the contents of Register 0x128 and how to interpret them.

MULTICHIP SYNCHRONIZATION

Table 27. SYSREF± Setup/Hold Monitor, Register 0x128

Register 0x128, Bits[7:4], Hold Status	Register 0x128, Bits[3:0], Setup Status	Description
0x0	0x0 to 0x7	Possible setup error. The smaller this number, the smaller the setup margin.
0x0 to 0x8	0x8	No setup or hold error (best hold margin).
0x8	0x9 to 0xF	No setup or hold error (best setup and hold margin).
0x8	0x0	No setup or hold error (best setup margin).
0x9 to 0xF	0x0	Possible hold error. The larger this number, the smaller the hold margin.
0x0	0x0	Possible setup or hold error.

TEST MODES

ADC TEST MODES

The AD9691 has various test options that aid in the system level implementation. The AD9691 has ADC test modes that are available in Register 0x550. These test modes are described in Table 28. When an output test mode is enabled, the analog section of the ADC is disconnected from the digital back-end blocks and the test pattern is run through the output formatting block. Some of the test patterns are subject to output formatting, and some are not. The PN generators from the PN sequence tests can be reset by setting Bit 4 or Bit 5 of Register 0x550. These tests can be performed with or without an analog signal (if present, the analog signal is ignored), but they do require an encode clock.

If the application mode has been set to select a DDC mode of operation, the test modes must be enabled for each DDC enabled. The test modes can be enabled via Bit 2 and Bit 0 of Register 0x327, Register 0x347, and Register 0x367, depending on which DDCs are selected. The I data uses the test patterns selected for Channel A, and the Q data uses the test patterns selected for Channel B. For DDC 3, only the I data uses the test patterns from Channel A. The Q data does not output test patterns. Bit 0 of Register 0x387 selects the Channel A test patterns for the I data. For more information, see the AN-877 Application Note, *Interfacing to High Speed ADCs via SPI*.

JESD204B BLOCK TEST MODES

In addition to the ADC test modes, the AD9691 also has flexible test modes in the JESD204B block. These test modes are listed in Register 0x573 and Register 0x574. These test patterns can be inserted at various points along the output data path. These test insertion points are shown in Figure 71. Table 29 describes the various test modes available in the JESD204B block. For the AD9691, a transition from the test modes (Register 0x573 ≠ 0x00) to normal mode (Register 0x573 = 0x00) require a SPI soft reset. This is done by writing 0x81 to Register 0x00 (self cleared).

Transport Layer Sample Test Mode

The transport layer samples are implemented in the AD9691 as defined by Section 5.1.6.3 in the JEDEC JESD204B specification. These tests are enabled via Register 0x571, Bit 5. The test pattern is equivalent to the raw samples from the ADC.

Interface Test Modes

The interface test modes are described in Register 0x573, Bits[3:0]. These test modes are also explained in Table 29. The interface tests can be inserted at various points along the data. See Figure 71 for more information on the test insertion points. Register 0x573, Bits[5:4], selects where these tests are inserted.

Table 30, Table 31, and Table 32 show examples of some of the test modes when inserted at the JESD204B sample input, physical layer (PHY) 10-bit input, and scrambler 8-bit input. UP in Table 30 to Table 32 represents the user pattern control bits from the memory map register table (see Table 35).

Data Link Layer Test Modes

The data link layer test modes are implemented in the AD9691 as defined by Section 5.3.3.8.2 in the JEDEC JESD204B specification. These tests are shown in Register 0x574, Bits[2:0]. Test patterns inserted at this point are useful for verifying the functionality of the data link layer. When the data link layer test modes are enabled, disable SYNCINB± by writing 0xC0 to Register 0x572.

Table 28. ADC Test Modes

Output Test Mode Bit Sequence	Pattern Name	Expression	Default/Seed Value	Sample (N, N + 1, N + 2, …)
0000	Off (default)	Not applicable	Not applicable	Not applicable
0001	Midscale short	00 0000 0000 0000	Not applicable	Not applicable
0010	+Full-scale short	01 1111 1111 1111	Not applicable	Not applicable
0011	−Full-scale short	10 0000 0000 0000	Not applicable	Not applicable
0100	Alternating checkerboard	10 1010 1010 1010	Not applicable	0x1555, 0x2AAA, 0x1555, 0x2AAA, 0x1555
0101	PN sequence, long	$x^{23} + x^{18} + 1$	0x3AFF	0x3FD7, 0x0002, 0x26E0, 0x0A3D, 0x1CA6
0110	PN sequence, short	$x^9 + x^5 + 1$	0x0092	0x125B, 0x3C9A, 0x2660, 0x0c65, 0x0697
0111	One-/zero word toggle	11 1111 1111 1111	Not applicable	0x0000, 0x3FFF, 0x0000, 0x3FFF, 0x0000
1000	User input	Register 0x551 to Register 0x558	Not applicable	For repeat mode: User Pattern 1[15:2], User Pattern 2[15:2], User Pattern 3[15:2], User Pattern 4[15:2], User Pattern 1[15:2]… For single mode: User Pattern 1[15:2], User Pattern 2[15:2], User Pattern 3[15:2], User Pattern 4[15:2], 0x0000…
1111	Ramp output	$(x) \% 2^{14}$	Not applicable	$(x) \% 2^{14}$, $(x + 1) \% 2^{14}$, $(x + 2) \% 2^{14}$, $(x + 3) \% 2^{14}$

TEST MODES

Table 29. JESD204B Interface Test Modes

Output Test Mode Bit Sequence	Pattern Name	Expression	Default
0000	Off (default)	Not applicable	Not applicable
0001	Alternating checkerboard	0x5555, 0xAAAA, 0x5555…	Not applicable
0010	One-/zero-word toggle	0x0000, 0xFFFF, 0x0000…	Not applicable
0011	31-bit PN sequence	$x^{31} + x^{28} + 1$	0x0003AFFF
0100	23-bit PN sequence	$x^{23} + x^{18} + 1$	0x003AFF
0101	15-bit PN sequence	$x^{15} + x^{14} + 1$	0x03AF
0110	9-bit PN sequence	$x^{9} + x^{5} + 1$	0x092
0111	7-bit PN sequence	$x^{7} + x^{6} + 1$	0x07
1000	Ramp output	$(x) \% 2^{16}$	Ramp size depends on test insertion point
1110	Continuous/repeat user test	Register 0x551 to Register 0x558	User Pattern 1 to User Pattern 4, then repeat
1111	Single user test	Register 0x551 to Register 0x558	User Pattern 1 to User Pattern 4, then zeros

Table 30. JESD204B Sample Input for M = 2, S = 2, N' = 16 (Register 0x573, Bits[5:4] = 'b00)

Frame No.	Converter No.	Sample No.	Alternating Checkerboard	One-/Zero- Word Toggle	Ramp	PN9	PN23	User Repeat	User Single
0	0	0	0x5555	0x0000	$(x) \% 2^{16}$	0x496F	0xFF5C	UP1[15:0]	UP1[15:0]
0	0	1	0x5555	0x0000	$(x) \% 2^{16}$	0x496F	0xFF5C	UP1[15:0]	UP1[15:0]
0	1	0	0x5555	0x0000	$(x) \% 2^{16}$	0x496F	0xFF5C	UP1[15:0]	UP1[15:0]
0	1	1	0x5555	0x0000	$(x) \% 2^{16}$	0x496F	0xFF5C	UP1[15:0]	UP1[15:0]
1	0	0	0xAAAA	0xFFFF	$(x + 1) \% 2^{16}$	0xC9A9	0x0029	UP2[15:0]	UP2[15:0]
1	0	1	0xAAAA	0xFFFF	$(x + 1) \% 2^{16}$	0xC9A9	0x0029	UP2[15:0]	UP2[15:0]
1	1	0	0xAAAA	0xFFFF	$(x + 1) \% 2^{16}$	0xC9A9	0x0029	UP2[15:0]	UP2[15:0]
1	1	1	0xAAAA	0xFFFF	$(x + 1) \% 2^{16}$	0xC9A9	0x0029	UP2[15:0]	UP2[15:0]
2	0	0	0x5555	0x0000	$(x + 2) \% 2^{16}$	0x980C	0xB80A	UP3[15:0]	UP3[15:0]
2	0	1	0x5555	0x0000	$(x + 2) \% 2^{16}$	0x980C	0xB80A	UP3[15:0]	UP3[15:0]
2	1	0	0x5555	0x0000	$(x + 2) \% 2^{16}$	0x980C	0xB80A	UP3[15:0]	UP3[15:0]
2	1	1	0x5555	0x0000	$(x + 2) \% 2^{16}$	0x980C	0xB80A	UP3[15:0]	UP3[15:0]
3	0	0	0xAAAA	0xFFFF	$(x + 3) \% 2^{16}$	0x651A	0x3D72	UP4[15:0]	UP4[15:0]
3	0	1	0xAAAA	0xFFFF	$(x + 3) \% 2^{16}$	0x651A	0x3D72	UP4[15:0]	UP4[15:0]
3	1	0	0xAAAA	0xFFFF	$(x + 3) \% 2^{16}$	0x651A	0x3D72	UP4[15:0]	UP4[15:0]
3	1	1	0xAAAA	0xFFFF	$(x + 3) \% 2^{16}$	0x651A	0x3D72	UP4[15:0]	UP4[15:0]
4	0	0	0x5555	0x0000	$(x + 4) \% 2^{16}$	0x5FD1	0x9B26	UP1[15:0]	0x0000
4	0	1	0x5555	0x0000	$(x + 4) \% 2^{16}$	0x5FD1	0x9B26	UP1[15:0]	0x0000
4	1	0	0x5555	0x0000	$(x + 4) \% 2^{16}$	0x5FD1	0x9B26	UP1[15:0]	0x0000
4	1	1	0x5555	0x0000	$(x + 4) \% 2^{16}$	0x5FD1	0x9B26	UP1[15:0]	0x0000

Table 31. Physical Layer 10-Bit Input (Register 0x573, Bits[5:4] = 'b01)

10-Bit Symbol No.	Alternating Checkerboard	One-/Zero- Word Toggle	Ramp	PN9	PN23	User Repeat	User Single
0	0x155	0x000	$(x) \% 2^{10}$	0x125	0x3FD	UP1[15:6]	UP1[15:6]
1	0x2AA	0x3FF	$(x + 1) \% 2^{10}$	0x2FC	0x1C0	UP2[15:6]	UP2[15:6]
2	0x155	0x000	$(x + 2) \% 2^{10}$	0x26A	0x00A	UP3[15:6]	UP3[15:6]
3	0x2AA	0x3FF	$(x + 3) \% 2^{10}$	0x198	0x1B8	UP4[15:6]	UP4[15:6]
4	0x155	0x000	$(x + 4) \% 2^{10}$	0x031	0x028	UP1[15:6]	0x000
5	0x2AA	0x3FF	$(x + 5) \% 2^{10}$	0x251	0x3D7	UP2[15:6]	0x000
6	0x155	0x000	$(x + 6) \% 2^{10}$	0x297	0x0A6	UP3[15:6]	0x000
7	0x2AA	0x3FF	$(x + 7) \% 2^{10}$	0x3D1	0x326	UP4[15:6]	0x000
8	0x155	0x000	$(x + 8) \% 2^{10}$	0x18E	0x10F	UP1[15:6]	0x000

TEST MODES

Table 31. Physical Layer 10-Bit Input (Register 0x573, Bits[5:4] = 'b01) (Continued)

10-Bit Symbol No.	Alternating Checkerboard	One-/Zero- Word Toggle	Ramp	PN9	PN23	User Repeat	User Single
9	0x2AA	0x3FF	$(x + 9) \% 2^{10}$	0x2CB	0x3FD	UP2[15:6]	0x000
10	0x155	0x000	$(x + 10) \% 2^{10}$	0x0F1	0x31E	UP3[15:6]	0x000
11	0x2AA	0x3FF	$(x + 11) \% 2^{10}$	0x3DD	0x008	UP4[15:6]	0x000

Table 32. Scrambler 8-Bit Input (Register 0x573, Bits[5:4] = 'b10)

8-Bit Octet No.	Alternating Checkerboard	One-/Zero- Word Toggle	Ramp	PN9	PN23	User Repeat	User Single
0	0x55	0x00	$(x) \% 2^{8}$	0x49	0xFF	UP1[15:9]	UP1[15:9]
1	0xAA	0xFF	$(x + 1) \% 2^{8}$	0x6F	0x5C	UP2[15:9]	UP2[15:9]
2	0x55	0x00	$(x + 2) \% 2^{8}$	0xC9	0x00	UP3[15:9]	UP3[15:9]
3	0xAA	0xFF	$(x + 3) \% 2^{8}$	0xA9	0x29	UP4[15:9]	UP4[15:9]
4	0x55	0x00	$(x + 4) \% 2^{8}$	0x98	0xB8	UP1[15:9]	0x00
5	0xAA	0xFF	$(x + 5) \% 2^{8}$	0x0C	0x0A	UP2[15:9]	0x00
6	0x55	0x00	$(x + 6) \% 2^{8}$	0x65	0x3D	UP3[15:9]	0x00
7	0xAA	0xFF	$(x + 7) \% 2^{8}$	0x1A	0x72	UP4[15:9]	0x00
8	0x55	0x00	$(x + 8) \% 2^{8}$	0x5F	0x9B	UP1[15:9]	0x00
9	0xAA	0xFF	$(x + 9) \% 2^{8}$	0xD1	0x26	UP2[15:9]	0x00
10	0x55	0x00	$(x + 10) \% 2^{8}$	0x63	0x43	UP3[15:9]	0x00
11	0xAA	0xFF	$(x + 11) \% 2^{8}$	0xAC	0xFF	UP4[15:9]	0x00

SERIAL PORT INTERFACE

The AD9691 SPI allows the user to configure the converter for specific functions or operations through a structured register space provided inside the ADC. The SPI gives the user added flexibility and customization, depending on the application. Addresses are accessed via the serial port and can be written to or read from via the port. Memory is organized into bytes that can be further divided into fields. These fields are documented in the Memory Map section. For detailed operational information, see the Serial Control Interface Standard (Rev. 1.0).

CONFIGURATION USING THE SPI

Three pins define the SPI of this ADC: the SCLK pin, the SDIO pin, and the CSB pin (see Table 33). The SCLK (serial clock) pin synchronizes the read and write data presented from/to the ADC. The SDIO (serial data input/output) pin is a dual-purpose pin that allows data to be sent and read from the internal ADC memory map registers. The CSB (chip select bar) pin is an active low control that enables or disables the read and write cycles.

Table 33. Serial Port Interface Pins

Pin	Function
SCLK	Serial clock. The serial shift clock input that synchronizes serial interface reads and writes.
SDIO	Serial data input/output. A dual-purpose pin that typically serves as an input or an output, depending on the instruction being sent and the relative position in the timing frame.
CSB	Chip select bar. An active low control that gates the read and write cycles.

The falling edge of CSB, in conjunction with the rising edge of SCLK, determines the start of the framing. An example of the serial timing and its definitions can be found in Figure 3 and Table 5.

Other modes involving the CSB pin are available. The CSB pin can be held low indefinitely, which permanently enables the device; this is called streaming. The CSB pin can stall high between bytes to allow additional external timing. When CSB is tied high, SPI functions are placed in a high impedance mode. This mode turns on any SPI pin secondary functions.

All data is composed of 8-bit words. The first bit of each individual byte of serial data indicates whether a read or write command is issued. This allows the SDIO pin to change direction from an input to an output.

In addition to word length, the instruction phase determines whether the serial frame is a read or write operation, allowing the serial port to be used both to program the chip and to read the contents of the on-chip memory. If the instruction is a readback operation, performing a readback causes the SDIO pin to change direction from an input to an output at the appropriate point in the serial frame.

Data can be sent in MSB first mode or in LSB first mode. MSB first is the default on power-up and can be changed via the SPI port configuration register. For more information about this and other features, see the Serial Control Interface Standard (Rev. 1.0).

HARDWARE INTERFACE

The pins described in Table 33 compose the physical interface between the user programming device and the serial port of the AD9691. The SCLK pin and the CSB pin function as inputs when using the SPI. The SDIO pin is bidirectional, functioning as an input during write phases and as an output during readback.

The SPI is flexible enough to be controlled by either FPGAs or microcontrollers. One method for SPI configuration is described in detail in the AN-812 Application Note, *Microcontroller-Based Serial Port Interface (SPI) Boot Circuit*.

Do not activate the SPI port during periods when the full dynamic performance of the converter is required. Because the SCLK signal, the CSB signal, and the SDIO signal are typically asynchronous to the ADC clock, noise from these signals can degrade converter performance. If the on-board SPI bus is used for other devices, it may be necessary to provide buffers between this bus and the AD9691 to prevent these signals from transitioning at the converter inputs during critical sampling periods.

SPI ACCESSIBLE FEATURES

Table 34 provides a brief description of the general features that are accessible via the SPI. These features are described in detail in the Serial Control Interface Standard (Rev. 1.0). The AD9691 device specific features are described in the Memory Map section.

Table 34. Features Accessible Using the SPI

Feature Name	Description
Mode	Allows the user to set either power-down mode or standby mode.
Clock	Allows the user to access the clock divider via the SPI.
DDC	Allows the user to set up decimation filters for different applications.
Test Input/Output	Allows the user to set test modes to have known data on output bits.
Output Mode	Allows the user to set up outputs.
SERDES Output Setup	Allows the user to vary SERDES settings such as swing and emphasis.

MEMORY MAP

READING THE MEMORY MAP REGISTER TABLE

Each row in the memory map register table has eight bit locations. The memory map is divided into four sections: the Analog Devices SPI registers (Register 0x000 to Register 0x00D), the ADC function registers (Register 0x015 to Register 0x27A), The DDC function registers (Register 0x300 to Register 0x387), and the digital outputs and test modes registers (Register 0x550 to Register 0x5C5).

Table 35 (see the Memory Map section) documents the default hexadecimal value for each hexadecimal address shown. The column with the heading Bit 7 (MSB) is the start of the default hexadecimal value given. For example, Address 0x561, the output mode register, has a hexadecimal default value of 0x01. This means that Bit 0 = 1, and the remaining bits are 0s. This setting is the default output format value, which is twos complement. For more information on this function and others, see Table 35.

Unassigned and Reserved Locations

All address and bit locations that are not included in Table 35 are not currently supported for this device. Write unused bits of a valid address location with 0s unless the default value is set otherwise. Writing to these locations is required only when part of an address location is unassigned (for example, Address 0x561). If the entire address location is unassigned (for example, Address 0x013), do not write to this address location.

Default Values

After the AD9691 is reset, critical registers are loaded with default values. The default values for the registers are given in Table 35.

Logic Levels

An explanation of logic level terminology follows:

- "Bit is set" is synonymous with "bit is set to Logic 1" or "writing Logic 1 for the bit."
- "Clear a bit" is synonymous with "bit is set to Logic 0" or "writing Logic 0 for the bit."
- X denotes a don't care bit.

Channel-Specific Registers

Some channel setup functions, such as input termination (Register 0x016), can be programmed to a different value for each channel. In these cases, channel address locations are internally duplicated for each channel. These registers and bits are designated in Table 35 as local. These local registers and bits can be accessed by setting the appropriate Channel A or Channel B bits in Register 0x008. If both bits are set, the subsequent write affects the registers of both channels. In a read cycle, set only Channel A or Channel B to read one of the two registers. If both bits are set during an SPI read cycle, the device returns the value for Channel A. Registers and bits designated as global in Table 35 affect the entire device and the channel features for which independent settings are not allowed between channels. The settings in Register 0x004 and Register 0x005 do not affect the global registers and bits.

SPI Soft Reset

After issuing a soft reset by programming 0x81 to Register 0x000, the AD9691 requires 5 ms to recover. When programming the AD9691 for application setup, ensure that an adequate delay is programmed into the firmware after asserting the soft reset and before starting the device setup.

MEMORY MAP

MEMORY MAP REGISTER TABLE

All address locations that are not included in Table 35 are not currently supported for this device and must not be written.

Table 35. Memory Map Registers

Reg Addr (Hex)	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default	Notes
Analog Devices SPI Registers											
0x000	INTERFACE_ CONFIG_A	Soft reset (self clearing)	LSB first 0 = MSB 1 = LSB	Address ascension	0	0	Address ascension	LSB first 0 = MSB 1 = LSB	Soft reset (self clearing)	0x00	
0x001	INTERFACE_ CONFIG_B	Single instruction	0	0	0	0	0	Datapath soft reset (self clearing)	0	0x00	
0x002	DEVICE_ CONFIG (local)	0	0	0	0	0	0	00 = normal operation 10 = standby 11 = power-down		0x00	
0x003	CHIP_TYPE	0	0	0	0	011 = high speed ADC				0x03	Read only
0x004	CHIP_ID (low byte)	1	1	0	1	0	0	0	1	0xD1	Read only
0x005	CHIP_ID (high byte)	0	0	0	0	0	0	0	0	0x00	Read only
0x006	CHIP_GRADE	1	0	1	0	X	X	X	X	0xAX	Read only
0x008	Device index	0	0	0	0	0	0	Channel B	Channel A	0x03	
0x00A	Scratch pad	0	0	0	0	0	0	0	0	0x00	
0x00B	SPI revision	0	0	0	0	0	0	0	1	0x01	
0x00C	Vendor ID (low byte)	0	1	0	1	0	1	1	0	0x56	Read only
0x00D	Vendor ID (high byte)	0	0	0	0	0	1	0	0	0x04	Read only
ADC Function Registers											
0x015	Analog input (local)	0	0	0	0	0	0	0	Input disable 0 = normal operation 1 = input disabled	0x00	
0x016	Input termination (local)	Analog input differential termination 0000 = 400 Ω (default) 0001 = 200 Ω 0010 = 100 Ω 0110 = 50 Ω				0	0	1	1	0x03	
0x018	Input buffer current control (local)	0000 = 1.0× buffer current 0001 = 1.5× buffer current 0010 = 2.0× buffer current 0011 = 2.5× buffer current (default) 0100 = 3.0× buffer current 0101 = 3.5× buffer current … 1111 = 8.5× buffer current				0	0	0	0	0x30	

MEMORY MAP

Table 35. Memory Map Registers (Continued)

Reg Addr (Hex)	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default	Notes
0x935	Buffer Control 2	0	0	0	0	0	Low frequency operation 0 = off 1 = on (default)	0	0	0x04	
0x024	V_1P0 control	0	0	0	0	0	0	0	1.0 V reference select 0 = internal 1 = external	0x00	
0x028	Temperature diode (local)	0	0	0	0	0	0	0	Diode selection 0 = no diode selected 1 = temperature diode selected	0x00	Used in conjunction with Reg. 0x040
0x03F	PDWN/STBY pin control (local)	0 = PDWN/STBY enabled1 = disabled	0	0	0	0	0	0	0	0x00	Used in conjunction with Reg. 0x040
0x040	Chip pin control	PDWN/STBY function 00 = power down 01 = standby 10 = disabled		Fast Detect B (FD_B) 000 = Fast Detect B output 001 = JESD204B LMFC output 010 = JESD204B internal SYNC~ output 111 = disabled			Fast Detect A (FD_A) 000 = Fast Detect A output 001 = JESD204B LMFC output 010 = JESD204B internal SYNC~ output 011 = temperature diode 111 = disabled			0x3F	
0x10B	Clock divider	0	0	0	0	0	000 = divide by 1 001 = divide by 2 011 = divide by 4 111 = divide by 8			0x00	
0x10C	Clock divider phase (local)	0	0	0	0	Independently controls Channel A and Channel B clock divider phase offset 0000 = 0 input clock cycles delayed 0001 = ½ input clock cycles delayed 0010 = 1 input clock cycles delayed 0011 = 1½ input clock cycles delayed 0100 = 2 input clock cycles delayed 0101 = 2½ input clock cycles delayed … 1111 = 7½ input clock cycles delayed				0x00	
0x10D	Clock divider and SYSREF± control	Clock divider auto phase adjust 0 = disabled 1 = enabled	0	0	0	Clock divider negative skew window 00 = no negative skew 01 = 1 device clock of negative skew 10 = 2 device clocks of negative skew 11 = 3 device clocks of negative skew		Clock divider positive skew window 00 = no positive skew 01 = 1 device clock of positive skew 10 = 2 device clocks of positive skew 11 = 3 device clocks of positive skew		0x00	Clock divider must be >1

MEMORY MAP

Table 35. Memory Map Registers (Continued)

Reg Addr (Hex)	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default	Notes
0x117	Clock delay control	0	0	0	0	0	0	0	Clock fine delay adjust enable 0 = disabled 1 = enabled	0x00	Enabling the clock fine delay adjust causes a datapath reset
0x118	Clock fine delay (local)	Clock fine delay adjust, Bits[7:0], twos complement coded control to adjust the fine sample clock skew in 1.7 ps steps ≤ −88 = −151.7 ps skew −87 = −150 ps skew … 0 = 0 ps skew … ≥ +87 = +150 ps skew								0x00	Used in conjunction with Reg. 0x117
0x11C	Clock status	0	0	0	0	0	0	0	0 = no input clock detected 1 = input clock detected	Read only	
0x120	SYSREF± Control 1	0	SYSREF± flag reset 0 = normal operation 1 = flags held in reset	0	SYSREF± transition select 0 = low to high 1 = high to low	CLK± edge select 0 = rising 1 = falling	SYSREF± mode select 00 = disabled 01 = continuous 10 = N-shot		0	0x00	
0x121	SYSREF± Control 2	0	0	0	0	SYSREF± N-shot ignore counter select 0000 = next SYSREF± only 0001 = ignore the first SYSREF± transitions 0010 = ignore the first two SYSREF± transitions … 1111 = ignore the first 16 SYSREF± transitions				0x00	Mode select, Reg. 0x120, Bits[2:1], must be N-shot
0x123	SYSREF± timestamp delay control	0	SYSREF± timestamp delay, Bits[6:0] 0x00 = no delay 0x01 = 1 clock delay … 0x7F = 127 clocks delay							0x00	Ignored when Reg. 0x1FF = 0x00
0x128	SYSREF± Status 1	SYSREF± hold status, see Table 27				SYSREF± setup status, see Table 27				Read only	
0x129	SYSREF± and clock divider status	0	0	0	0	Clock divider phase when SYSREF± was captured 0000 = in-phase 0001 = SYSREF± is ½ cycle delayed from clock 0010 = SYSREF± is 1 cycle delayed from clock 0011 = 1½ input clock cycles delayed 0100 = 2 input clock cycles delayed 0101 = 2½ input clock cycles delayed … 1111 = 7½ input clock cycles delayed				Read only	
0x12A	SYSREF± counter	SYSREF± counter, Bits[7:0] increments when a SYSREF± signal is captured								Read only	
0x1FF	Chip sync mode	0	0	0	0	0	0	Synchronization mode 00 = normal 01 = timestamp		0x00	

MEMORY MAP

Table 35. Memory Map Registers (Continued)

Reg Addr (Hex)	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default	Notes
0x200	Chip application mode	0	0	Chip Q ignore 0 = normal (I/Q) 1 = ignore (I only)	0	0	0	Chip operating mode 00 = full bandwidth mode 01 = DDC 0 on 10 = DDC 0 and DDC 1		0x00	
0x201	Chip decimation ratio	0	0	0	0	0	Chip decimation ratio select 000 = full sample rate (decimate = 1) 001 = decimate by 2			0x00	
0x228	Customer offset	Offset adjust in LSBs from +127 to −128 (twos complement format)								0x00	
0x245	Fast detect (FD) control (local)	0	0	0	0	Force FD_A/ FD_B pins 0 = normal function 1 = force to value	Force value of FD_A/ FD_B pins if force pins is true, this value is output on FD pins	0	Enable fast detect output	0x00	
0x247	FD upper threshold LSB (local)	Fast detect upper threshold, Bits[7:0]								0x00	
0x248	FD upper threshold MSB (local)	0	0	0	Fast detect upper threshold, Bits[12:8]					0x00	
0x249	FD lower threshold LSB (local)	Fast detect lower threshold, Bits[7:0]								0x00	
0x24A	FD lower threshold MSB (local)	0	0	0	Fast detect lower threshold, Bits[12:8]					0x00	
0x24B	FD dwell time LSB (local)	Fast detect dwell time, Bits[7:0]								0x00	
0x24C	FD dwell time MSB (local)	Fast detect dwell time, Bits[15:8]								0x00	
0x26F	Signal monitor synchronization control	0	0	0	0	0	0	Synchronization mode 00 = disabled 01 = continuous 11 = one-shot		0x00	See the Signal Monitor section
0x270	Signal monitor control (local)	0	0	0	0	0	0	Peak detector 0 = disabled 1 = enabled	0	0x00	
0x271	Signal Monitor Period Register 0 (local)	Signal monitor period, Bits[7:0]								0x80	In decimated output clock cycles
0x272	Signal Monitor Period Register 1 (local)	Signal monitor period, Bits[15:8]								0x00	In decimated output clock cycles

MEMORY MAP

Table 35. Memory Map Registers (Continued)

Reg Addr (Hex)	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default	Notes
0x273	Signal Monitor Period Register 2 (local)	Signal monitor period, Bits[23:16]								0x00	In decimated output clock cycles
0x274	Signal monitor result control(local)	0	0	0	Result update 1 = update results (self clear)	0	0	0	Result selection 0 = reserved 1 = peak detector	0x01	
0x275	Signal Monitor Result Register 0 (local)	Signal monitor result, Bits[7:0] When Register 0x274, Bit 0 = 1, result Bits[19:7] = peak detector absolute value, Bits[12:0]; result Bits[6:0] = 0								Read only	Updated based on Reg. 0x274, Bit 4
0x276	Signal Monitor Result Register 1 (local)	Signal monitor result, Bits[15:8]								Read only	Updated based on Reg. 0x274, Bit 4
0x277	Signal Monitor Result Register 1 (local)	0	0	0	0	Signal monitor result, Bits[19:16]				Read only	Updated based on Reg. 0x274, Bit 4
0x278	Signal monitor period counter result (local)	Period count result, Bits[7:0]								Read only	Updated based on Reg. 0x274, Bit 4
0x279	Signal monitor SPORT over JESD204B control (local)	0	0	0	0	0	0	00 = reserved 11 = enable		0x00	
0x27A	SPORT over JESD204B input selection (local)	0	0	0	0	0	0	Peak detector 0 = disabled 1 = enabled	0	0x00	
DDC Function Registers (See the Digital Downconverters (DDCs) Section)											
0x300	DDC sync control	0	0	0	DDC NCO soft reset 0 = normal operation 1 = reset	0	0	Synchronization mode (triggered by SYSREF±) 00 = disabled 01 = continuous 11 = one-shot			
0x310	DDC 0 control	Mixer select 0 = real mixer 1 = complex mixer	Gain select 0 = 0 dB gain 1 = 6 dB gain	IF (intermediate frequency) mode 00 = variable IF mode (mixers and NCO enabled) 01 = 0 Hz IF mode (mixer bypassed, NCO disabled) 10 = $f_S/4$ Hz IF mode ($f_S/4$ downmixing mode) 11 = test mode (mixer inputs forced to +FS, NCO enabled)		Complex to real enable 0 = disabled 1 = enabled	0	Decimation rate select (complex to real disabled) 11 = decimate by 2 00 = decimate by 4 01 = decimate by 8 10 = decimate by 16 (complex to real enabled) 11 = decimate by 1 00 = decimate by 2 01 = decimate by 4 10 = decimate by 8		0x00	
0x311	DDC 0 input selection	0	0	0	0	0	Q input select 0 = Ch. A 1 = Ch. B	0	I input select 0 = Ch. A 1 = Ch. B	0x00	

MEMORY MAP

Table 35. Memory Map Registers (Continued)

Reg Addr (Hex)	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default	Notes
0x314	DDC 0 frequency LSB	DDC 0 NCO FTW, Bits[7:0], twos complement								0x00	
0x315	DDC 0 frequency MSB	X	X	X	X	DDC 0 NCO FTW, Bits[11:8], twos complement				0x00	
0x320	DDC 0 phase LSB	DDC 0 NCO POW, Bits[7:0], twos complement								0x00	
0x321	DDC 0 phase MSB	X	X	X	X	DDC 0 NCO POW, Bits[11:8], twos complement				0x00	
0x327	DDC 0 output test mode selection	0	0	0	0	0	Q output test mode enable 0 = disabled 1 = enabled from Channel B	0	I output test mode enable 0 = disabled 1 = enabled from Channel A	0x00	
0x330	DDC 1 control	Mixer select 0 = real mixer 1 = complex mixer	Gain select 0 = 0 dB gain 1 = 6 dB gain	IF (intermediate frequency) mode 00 = variable IF mode (mixers and NCO enabled) 01 = 0 Hz IF mode (mixer bypassed, NCO disabled) 10 = $f_S/4$ Hz IF mode ($f_S/4$ downmixing mode) 11 = test mode (mixer inputs forced to +FS, NCO enabled)		Complex to real enable 0 = disabled 1 = enabled	0	Decimation rate select (complex to real disabled) 11 = decimate by 2 00 = decimate by 4 01 = decimate by 8 10 = decimate by 16 (complex to real enabled) 11 = decimate by 1 00 = decimate by 2 01 = decimate by 4 10 = decimate by 8		0x00	
0x331	DDC 1 input selection	0	0	0	0	0	Q input select 0 = Ch. A 1 = Ch. B	0	I input select 0 = Ch. A 1 = Ch. B	0x00	
0x334	DDC 1 frequency LSB	DDC 1 NCO FTW, Bits[7:0], twos complement								0x00	
0x335	DDC 1 frequency MSB	X	X	X	X	DDC 1 NCO FTW, Bits[11:8], twos complement				0x00	
0x340	DDC 1 phase LSB	DDC 1 NCO POW, Bits[7:0], twos complement								0x00	
0x341	DDC 1 phase MSB	X	X	X	X	DDC 1 NCO POW, Bits[11:8], twos complement				0x00	
0x347	DDC 1 output test mode selection	0	0	0	0	0	Q output test mode enable 0 = disabled 1 = enabled from Channel B	0	I output test mode enable 0 = disabled 1 = enabled from Channel A	0x00	
0x350	DDC 2 control	Mixer select 0 = real mixer 1 = complex mixer	Gain select 0 = 0 dB gain 1 = 6 dB gain	IF (intermediate frequency) mode 00 = variable IF mode (mixers and NCO enabled) 01 = 0 Hz IF mode (mixer bypassed, NCO disabled) 10 = $f_S/4$ Hz IF mode ($f_S/4$ downmixing mode)		Complex to real enable 0 = disabled 1 = enabled	0	Decimation rate select (complex to real disabled) 11 = decimate by 2 00 = decimate by 4 01 = decimate by 8 10 = decimate by 16 (complex to real enabled) 11 = decimate by 1		0x00	

MEMORY MAP

Table 35. Memory Map Registers (Continued)

Reg Addr (Hex)	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default	Notes
				11 = test mode (mixer inputs forced to +FS, NCO enabled)				00 = decimate by 2 01 = decimate by 4 10 = decimate by 8			
0x351	DDC 2 input selection	0	0	0	0	0	Q input select 0 = Ch. A 1 = Ch. B	0	I input select 0 = Ch. A 1 = Ch. B	0x00	
0x354	DDC 2 frequency LSB	DDC 2 NCO FTW, Bits[7:0], twos complement								0x00	
0x355	DDC 2 frequency MSB	X	X	X	X	DDC 2 NCO FTW, Bits[11:8], twos complement				0x00	
0x360	DDC 2 phase LSB	DDC 2 NCO POW, Bits[7:0], twos complement								0x00	
0x361	DDC 2 phase MSB	X	X	X	X	DDC 2 NCO POW, Bits[11:8], twos complement				0x00	
0x367	DDC 2 output test mode selection	0	0	0	0	0	Q output test mode enable 0 = disabled 1 = enabled from Channel B	0	I output test mode enable 0 = disabled 1 = enabled from Channel A	0x00	
0x370	DDC 3 control	Mixer select 0 = real mixer 1 = complex mixer	Gain select 0 = 0 dB gain 1 = 6 dB gain	IF (intermediate frequency) mode 00 = variable IF mode (mixers and NCO enabled) 01 = 0 Hz IF mode (mixer bypassed, NCO disabled) 10 = $f_S/4$ Hz IF mode ($f_S/4$ downmixing mode) 11 = test mode (mixer inputs forced to +FS, NCO enabled)		Complex to real enable 0 = disabled 1 = enabled	0	Decimation rate select (complex to real disabled) 11 = decimate by 2 00 = decimate by 4 01 = decimate by 8 10 = decimate by 16 (complex to real enabled) 11 = decimate by 1 00 = decimate by 2 01 = decimate by 4 10 = decimate by 8		0x00	
0x371	DDC 3 input selection	0	0	0	0	0	Q input select 0 = Ch. A 1 = Ch. B	0	I input select 0 = Ch. A 1 = Ch. B	0x00	
0x374	DDC 3 frequency LSB	DDC 3 NCO FTW, Bits[7:0], twos complement								0x00	
0x375	DDC 3 frequency MSB	X	X	X	X	DDC 3 NCO FTW, Bits[11:8], twos complement				0x00	
0x380	DDC3 phase LSB	DDC 3 NCO POW, Bits[7:0], twos complement								0x00	
0x381	DDC 3 phase MSB	X	X	X	X	DDC 3 NCO POW, Bits[11:8], twos complement				0x00	
0x387	DDC 3 output test mode selection	0	0	0	0	0	0	0	I output test mode enable 0 = disabled 1 = enabled from Channel A	0x00	

MEMORY MAP

Table 35. Memory Map Registers (Continued)

Reg Addr (Hex)	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default	Notes
Digital Outputs and Test Modes											
0x550	ADC test modes(local)	User pattern selection 0 = continuous repeat 1 = single pattern	0	Reset PN long gen 0 = long PN enable 1 = long PN reset	Reset PN short gen 0 = short PN enable 1 = short PN reset	Test mode selection 0000 = off, normal operation 0001 = midscale short 0010 = positive full scale 0011 = negative full scale 0100 = alternating checker board 0101 = PN sequence, long 0110 = PN sequence, short 0111 = 1/0 word toggle 1000 = the user pattern test mode (used with Register 0x550, Bit 7 and User Pattern 1 through User Pattern 4 registers), 1111 = ramp output				0x00	
0x551	User Pattern 1 LSB	0	0	0	0	0	0	0	0	0x00	Used with Reg. 0x550 and Reg. 0x573
0x552	User Pattern 1 MSB	0	0	0	0	0	0	0	0	0x00	Used with Reg. 0x550 and Reg. 0x573
0x553	User Pattern 2 LSB	0	0	0	0	0	0	0	0	0x00	Used with Reg. 0x550 and Reg. 0x573
0x554	User Pattern 2 MSB	0	0	0	0	0	0	0	0	0x00	Used with Reg. 0x550 and Reg. 0x573
0x555	User Pattern 3 LSB	0	0	0	0	0	0	0	0	0x00	Used with Reg. 0x550 and Reg. 0x573
0x556	User Pattern 3 MSB	0	0	0	0	0	0	0	0	0x00	Used with Reg. 0x550 and Reg. 0x573
0x557	User Pattern 4 LSB	0	0	0	0	0	0	0	0	0x00	Used with Reg. 0x550 and Reg. 0x573
0x558	User Pattern 4 MSB	0	0	0	0	0	0	0	0	0x00	Used with Reg. 0x550 and Reg. 0x573
0x559	Output Mode Control 1	0	Converter control Bit 1 selection 000 = tie low (1'b0) 001 = overrange bit 010 = signal monitor bit 011 = fast detect (FD) bit 101 = SYSREF± Only used when CS			0	Converter control Bit 0 selection 000 = tie low (1'b0) 001 = overrange bit 010 = signal monitor bit 011 = fast detect (FD) bit 101 = SYSREF± Only used when CS			0x00	

MEMORY MAP

Table 35. Memory Map Registers (Continued)

Reg Addr (Hex)	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default	Notes
			(Register 0x58F) = 2 or 3				(Register 0x58F) = 3				
0x55A	Output Mode Control 2	0	0	0	0	0	Converter control Bit 2 selection 000 = tie low (1'b0) 001 = overrange bit 010 = signal monitor bit 011 = fast detect (FD) bit 101 = SYSREF± Used when CS (Register 0x58F) = 1, 2, or 3			0x00	
0x561	Output mode	0	0	0	0	0	Sample invert 0 = normal 1 = sample invert	Data format select 00 = offset binary 01 = twos complement		0x01	
0x562	Output overrange (OR) clear	Virtual Converter 7 OR 0 = OR bit enabled 1 = OR bit cleared	Virtual Converter 6 OR 0 = OR bit enabled 1 = OR bit cleared	Virtual Converter 5 OR 0 = OR bit enabled 1 = OR bit cleared	Virtual Converter 4 OR 0 = OR bit enabled 1 = OR bit cleared	Virtual Converter 3 OR 0 = OR bit enabled 1 = OR bit cleared	Virtual Converter 2 OR 0 = OR bit enabled 1 = OR bit cleared	Virtual Converter 1 OR 0 = OR bit enabled 1 = OR bit cleared	Virtual Converter 0 OR 0 = OR bit enabled 1 = OR bit cleared	0x00	
0x563	Output OR status	Virtual Converter 7 OR 0 = no OR 1 = OR occured	Virtual Converter 6 OR 0 = no OR 1 = OR occured	Virtual Converter 5 OR 0 = no OR 1 = OR occured	Virtual Converter 4 OR 0 = no OR 1 = OR occured	Virtual Converter 3 OR 0 = no OR 1 = OR occured	Virtual Converter 2 OR 0 = no OR 1 = OR occured	Virtual Converter 1 OR 0 = no OR 1 = OR occured	Virtual Converter 0 OR 0 = no OR 1 = OR occured	0x00	Read only
0x564	Output channel select	0	0	0	0	0	0	0	Converter channel swap 0 = normal channel ordering 1 = channel swap enabled	0x00	
0x56E	JESD204B lane rate control	0	0	0	0 = serial lane rate >6.25 Gbps and ≤12.5 Gbps 1 = serial lane rate must be > 3.125 Gbps and ≤ 6.25 Gbps	0	0	0	0	0x10	
0x570	JESD204B quick configuration	JESD204B quick configuration L = number of lanes = $2^{\text{Register 0x570, Bits[7:6]}}$ M = number of converters = $2^{\text{Register 0x570, Bits[5:3]}}$ F = number of octets/frame = $2^{\text{Register 0x570, Bits[2:0]}}$								0x88	See Table 25 and Table 26
0x571	JESD204B Link Mode Control 1	Standby mode 0 = all converter outputs 0 1 = CGS (/K28.5/)	Tail bit (t) PN 0 = disable 1 = enable T = N′ − N − CS	Long transport layer test 0 = disable 1 = enable	Lane synchronization 0 = disable FACI uses /K28.7/	ILAS sequence mode 00 = ILAS disabled 01 = ILAS enabled 11 = ILAS always on test mode		FACI 0 = enabled 1 = disabled	Link control 0 = active 1 = power down	0x14	

MEMORY MAP

Table 35. Memory Map Registers (Continued)

Reg Addr (Hex)	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default	Notes
					1 = enable FACI uses / K28.3/ and / K28.7/						
0x572	JESD204B Link Mode Control 2	SYNCINB± pin control 00 = normal 10 = ignore SYNCINB± (force CGS) 11 = ignore SYNCINB± (force ILAS/user data)		SYNC-INB± pin invert 0 = active low 1 = active high	SYNCINB± pin type 0 = differential 1 = CMOS	0	8B/10B bypass 0 = normal 1 = bypass	8B/10B bit invert 0 = normal 1 = invert the a to j symbols	0	0x00	
0x573	JESD204B Link Mode Control 3	CHKSUM mode 00 = sum of all 8-bit link config registers 01 = sum of individual link config fields 10 = checksum set to zero		Test injection point 00 = N′ sample input 01 = 10-bit data at 8B/10B output (for PHY testing) 10 = 8-bit data at scrambler input		JESD204B test mode patterns 0000 = normal operation (test mode disabled) 0001 = alternating checker board 0010 = 1/0 word toggle 0011 = 31-bit PN sequence—$x^{31} + x^{28} + 1$ 0100 = 23-bit PN sequence—$x^{23} + x^{18} + 1$ 0101 = 15-bit PN sequence—$x^{15} + x^{14} + 1$ 0110 = 9-bit PN sequence—$x^{9} + x^{5} + 1$ 0111 = 7-bit PN sequence—$x^{7} + x^{6} + 1$ 1000 = ramp output 1110 = continuous/repeat user test 1111 = single user test				0x00	
0x574	JESD204B Link Mode Control 4	ILAS delay 0000 = transmit ILAS on first LMFC after SYNCINB± deasserted 0001 = transmit ILAS on second LMFC after SYNCINB± deasserted … 1111 = transmit ILAS on 16th LMFC after SYNCINB± deasserted				0	Link layer test mode 000 = normal operation (link layer test mode disabled) 001 = continuous sequence of /D21.5/ characters 100 = modified RPAT test sequence 101 = JSPAT test sequence 110 = JTSPAT test sequence			0x00	
0x578	JESD204B LMFC offset	0	0	0	LMFC phase offset value, Bits[4:0]					0x00	
0x580	JESD204B DID config	JESD204B Tx device ID (DID) value, Bits[7:0]								0x00	
0x581	JESD204B BID config	0	0	0	0	JESD204B Tx bank ID (BID) value, Bits[3:0]				0x00	
0x583	JESD204B LID Config 1	0	0	0	Lane 0 lane ID (LID) value, Bits[4:0]					0x00	
0x584	JESD204B LID Config 2	0	0	0	Lane 1 LID value, Bits[4:0]					0x01	
0x585	JESD204B LID Config 3	0	0	0	Lane 2 LID value, Bits[4:0]					0x02	
0x586	JESD204B LID Config 4	0	0	0	Lane 3 LID value, Bits[4:0]					0x03	
0x587	JESD204B LID Config 5	0	0	0	Lane 4 LID value, Bits[4:0]					0x04	
0x588	JESD204B LID Config 6	0	0	0	Lane 5 LID value, Bits[4:0]					0x05	
0x589	JESD204B LID Config 7	0	0	0	Lane 6 LID value, Bits[4:0]					0x06	

MEMORY MAP

Table 35. Memory Map Registers (Continued)

Reg Addr (Hex)	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default	Notes
0x58A	JESD204B LID Config 8	0	0	0	Lane 7 LID value, Bits[4:0]					0x07	
0x58B	JESD204B parameters SCR/L	JESD204B scrambling (SCR) 0 = disabled 1 = enabled	0	0	0	0	JESD204B lanes (L) 000 = 1 lane 001 = 2 lanes 011 = 4 lanes 111 = 7 lanes Read only, see Register 0x570			0x8X	
0x58C	JESD204B F config	Number of octets per frame, F = Register 0x58C, Bits[7:0] + 1								0x88	Read only, seeReg. 0x570
0x58D	JESD204B K config	0	0	0	Number of frames per multiframe, K = Register 0x58D, Bits[4:0] + 1 Only values where (F × K) mod 4 = 0 are supported					0x1F	SeeReg. 0x570
0x58E	JESD204B M config	Number of converters per link, Bits[7:0] 0x00 = link connected to one virtual converter (M = 1) 0x01 = link connected to two virtual converters (M = 2) 0x03 = link connected to four virtual converters (M = 4) 0x07 = link connected to eight virtual converters (M = 8)									Read only
0x58F	JESD204B CS/N config	Number of control bits (CS) per sample 00 = no control bits (CS = 0) 01 = 1 control bit (CS = 1); Control Bit 2 only 10 = 2 control bits (CS = 2); Control Bit 2 and Control Bit 1 only 11 = 3 control bits (CS = 3); all control bits (2, 1, 0)		0	ADC converter resolution (N) 0x06 = 7-bit resolution 0x07 = 8-bit resolution 0x08 = 9-bit resolution 0x09 = 10-bit resolution 0x0A = 11-bit resolution 0x0B = 14-bit resolution (default) 0x0C = 13-bit resolution 0x0D = 14-bit resolution 0x0E = 15-bit resolution 0x0F = 16-bit resolution					0x0B	
0x590	JESD204B N′ config	Subclass support (Subclass version) 000 = Subclass 0 (no deterministic latency) 001 = Subclass 1			ADC number of bits per sample (N′) 0x7 = 8 bits 0xF = 16 bits					0x2F	
0x591	JESD204B S config	0	0	1	Samples per converter frame cycle (S) S value = Register 0x591, Bits[4:0] +1						Read only
0x592	JESD204B HD and CF configuration	HD value0 = disabled1 = enabled	0	0	Control words per frame clock cycle per link (CF)CF value = Register 0x592, Bits[4:0]					0x80	Read only
0x5A0	JESD204B CHKSUM 0	CHKSUM value for SERDOUT0±, Bits[7:0]								0xC3	Read only
0x5A1	JESD204B CHKSUM 1	CHKSUM value for SERDOUT1±, Bits[7:0]								0xC4	Read only
0x5A2	JESD204B CHKSUM 2	CHKSUM value for SERDOUT2±, Bits[7:0]								0xC5	Read only
0x5A3	JESD204B CHKSUM 3	CHKSUM value for SERDOUT3±, Bits[7:0]								0xC6	Read only
0x5A4	JESD204B CHKSUM 4	CHKSUM value for SERDOUT4±, Bits[7:0]								0xC7	Read only
0x5A5	JESD204B CHKSUM 5	CHKSUM value for SERDOUT5±, Bits[7:0]								0xC8	Read only
0x5A6	JESD204B CHKSUM 6	CHKSUM value for SERDOUT6±, Bits[7:0]								0xC9	Read only

MEMORY MAP

Table 35. Memory Map Registers (Continued)

Reg Addr (Hex)	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default	Notes
0x5A7	JESD204B CHKSUM 7	CHKSUM value for SERDOUT7±, Bits[7:0]								0xCA	Read only
0x5B0	JESD204B lane power-down	SERD-OUT7± 0 = on 1 = off	SERD-OUT6± 0 = on 1 = off	SERD-OUT5± 0 = on 1 = off	SERDOUT4± 0 = on 1 = off	SERD-OUT3± 0 = on 1 = off	SERD-OUT2± 0 = on 1 = off	SERD-OUT1± 0 = on 1 = off	SERDOUT0± 0 = on 1 = off	0xAA	
0x5B2	JESD204B lane SERDOUT0±/ SERDOUT1± assign	0	SERDOUT1± lane assignment 000 = Logical Lane 0 001 = Logical Lane 1 010 = Logical Lane 2 011 = Logical Lane 3 100 = Logical Lane 4 101 = Logical Lane 5 110 = Logical Lane 6 111 = Logical Lane 7			0	SERDOUT0± lane assignment 000 = Logical Lane 0 001 = Logical Lane 1 010 = Logical Lane 2 011 = Logical Lane 3 100 = Logical Lane 4 101 = Logical Lane 5 110 = Logical Lane 6 111 = Logical Lane 7			0x10	
0x5B3	JESD204B lane SERDOUT2±/ SERDOUT3± assign	0	SERDOUT3± lane assignment 000 = Logical Lane 0 001 = Logical Lane 1 010 = Logical Lane 2 011 = Logical Lane 3 100 = Logical Lane 4 101 = Logical Lane 5 110 = Logical Lane 6 111 = Logical Lane 7			0	SERDOUT2± lane assignment 000 = Logical Lane 0 001 = Logical Lane 1 010 = Logical Lane 2 011 = Logical Lane 3 100 = Logical Lane 4 101 = Logical Lane 5 110 = Logical Lane 6 111 = Logical Lane 7			0x32	
0x5B5	JESD204B lane SERDOUT4±/ SERDOUT5± assign	0	SERDOUT5± lane assignment 000 = Logical Lane 0 001 = Logical Lane 1 010 = Logical Lane 2 011 = Logical Lane 3 100 = Logical Lane 4 101 = Logical Lane 5 110 = Logical Lane 6 111 = Logical Lane 7			0	SERDOUT4± lane assignment 000 = Logical Lane 0 001 = Logical Lane 1 010 = Logical Lane 2 011 = Logical Lane 3 100 = Logical Lane 4 101 = Logical Lane 5 110 = Logical Lane 6 111 = Logical Lane 7			0x54	
0x5B6	JESD204B lane SERDOUT6±/ SERDOUT7± assign	0	SERDOUT7± lane assignment 000 = Logical Lane 0 001 = Logical Lane 1 010 = Logical Lane 2 011 = Logical Lane 3 100 = Logical Lane 4 101 = Logical Lane 5 110 = Logical Lane 6 111 = Logical Lane 7			0	SERDOUT6± lane assignment 000 = Logical Lane 0 001 = Logical Lane 1 010 = Logical Lane 2 011 = Logical Lane 3 100 = Logical Lane 4 101 = Logical Lane 5 110 = Logical Lane 6 111 = Logical Lane 7			0x76	
0x5BF	JESD204B serializer drive adjust	0	0	0	0	Swing voltage 0000 = 237.5 mV 0001 = 250 mV 0010 = 262.5 mV 0011 = 275 mV 0100 = 287.5 mV 0101 = 300 mV (default) 0110 = 312.5 mV 0111 = 325 mV 1000 = 337.5 mV 1001 = 350 mV 1010 = 362.5 mV				0x05	

MEMORY MAP

Table 35. Memory Map Registers (Continued)

Reg Addr (Hex)	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default	Notes
						1011 = 375 mV 1100 = 387.5 mV 1101 = 400 mV 1110 = 412.5 mV 1111 = 425 mV					
0x5C1	De-emphasis select	SERDOUT7± 0 = disable 1 = enable	SERDOUT6± 0 = disable 1 = enable	SERDOUT5± 0 = disable 1 = enable	SERDOUT4± 0 = disable 1 = enable	SERDOUT3± 0 = disable 1 = enable	SERD-OUT2± 0 = disable 1 = enable	SERDOUT1± 0 = disable 1 = enable	SERDOUT0± 0 = disable 1 = enable	0x00	
0x5C2	De-emphasis setting for SERDOUT0±/ SERDOUT1±	0	0	0	0	SERDOUT0±/SERDOUT1± de-emphasis settings 0000 = 0 dB 0001 = 0.3 dB 0010 = 0.8 dB 0011 = 1.4 dB 0100 = 2.2 dB 0101 = 3.0 dB 0110 = 4.0 dB 0111 = 5.0 dB				0x00	
0x5C3	De-emphasis setting for SERDOUT2±/ SERDOUT3±	0	0	0	0	SERDOUT2±/SERDOUT3± de-emphasis settings 0000 = 0 dB 0001 = 0.3 dB 0010 = 0.8 dB 0011 = 1.4 dB 0100 = 2.2 dB 0101 = 3.0 dB 0110 = 4.0 dB 0111 = 5.0 dB				0x00	
0x5C4	De-emphasis setting for SERDOUT4±/ SERDOUT5±	0	0	0	0	SERDOUT4±/SERDOUT5± de-emphasis settings 0000 = 0 dB 0001 = 0.3 dB 0010 = 0.8 dB 0011 = 1.4 dB 0100 = 2.2 dB 0101 = 3.0 dB 0110 = 4.0 dB 0111 = 5.0 dB				0x00	
0x5C5	De-emphasis setting for SERDOUT6±/ SERDOUT7±	0	0	0	0	SERDOUT6±/SERDOUT7± de-emphasis settings 0000 = 0 dB 0001 = 0.3 dB 0010 = 0.8 dB 0011 = 1.4 dB 0100 = 2.2 dB 0101 = 3.0 dB 0110 = 4.0 dB 0111 = 5.0 dB				0x00	

APPLICATIONS INFORMATION

POWER SUPPLY RECOMMENDATIONS

The AD9691 must be powered by the following seven supplies: AVDD1 = 1.25 V, AVDD2 = 2.50 V, AVDD3 = 3.3 V, AVDD1_SR = 1.25 V, DVDD = 1.25 V, DRVDD = 1.25 V, and SPIVDD = 1.8 V. For applications requiring an optimal high power efficiency and low noise performance, it is recommended that the ADP2164 and ADP2370 switching regulators be used to convert the 3.3 V, 5.0 V, or 12 V input rails to an intermediate rail (1.8 V and 3.8 V). These intermediate rails are then postregulated by very low noise, low dropout (LDO) regulators (ADP1741, ADP1740, and ADP125). Figure 83 shows the recommended power supply scheme for AD9691.

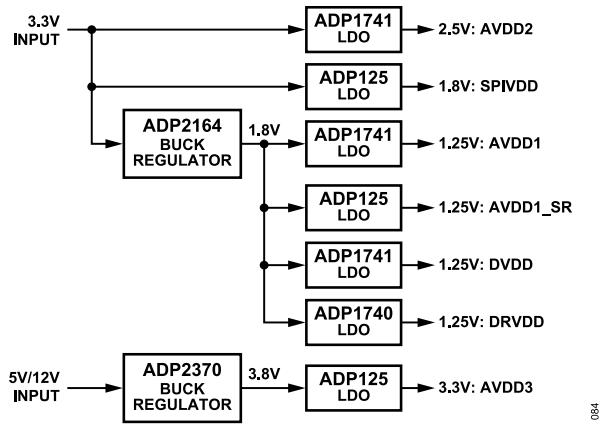

Figure 83. High Efficiency, Low Noise Power Solution for the AD9691

It is not necessary to split all of these power domains in all cases. The recommended solution shown in Figure 83 provides the lowest noise, highest efficiency power delivery system for the AD9691. If only one 1.25 V supply is available, route to AVDD1 first and then tap it off and isolate it with a ferrite bead or a filter choke, preceded by decoupling capacitors for AVDD1_SR, SPIVDD, DVDD, and DRVDD, in that order. The user can employ several different decoupling capacitors to cover both high and low frequencies. These must be located close to the point of entry at the PCB level and close to the devices, with minimal trace lengths.

EXPOSED PAD THERMAL HEAT SLUG RECOMMENDATIONS

It is required that the exposed pad on the underside of the ADC be connected to ground to achieve the best electrical and thermal performance of the AD9691. Connect an exposed continuous copper plane on the PCB to the AD9691 exposed pad, Pin 0. The copper plane must have several vias to achieve the lowest possible resistive thermal path for heat dissipation to flow through the bottom of the PCB. These vias must be solder filled or plugged. The number of vias and the fill determine the resultant θ_{JA} measured on the board. This is shown in Table 7.

To maximize the coverage and adhesion between the ADC and PCB, partition the continuous copper plane by overlaying a silkscreen on the PCB into several uniform sections. This provides several tie points between the ADC and PCB during the reflow process, whereas using one continuous plane with no partitions only guarantees one tie point. See Figure 84 for a recommended PCB layout example. For detailed information on packaging and the PCB layout of chip scale packages, see the AN-772 Application Note, *A Design and Manufacturing Guide for the Lead Frame Chip Scale Package (LFCSP)*.

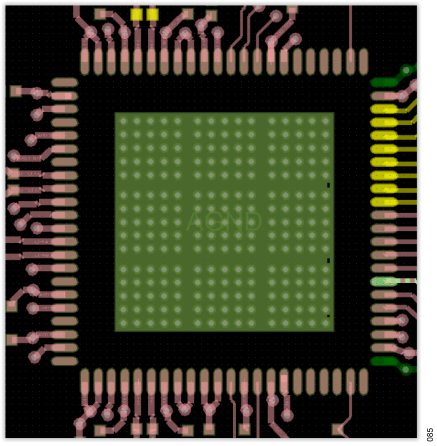

Figure 84. Recommended PCB Layout of Exposed Pad for the AD9691

AVDD1_SR (PIN 78) AND AGND (PIN 77 AND PIN 81)

AVDD1_SR (Pin 78) and AGND (Pin 77 and Pin 81) can be used to provide a separate power supply node to the SYSREF± circuits of AD9691. If running in Subclass 1, the AD9691 can support periodic one-shot or gapped signals. To minimize the coupling of this supply into the AVDD1 supply node, adequate supply bypassing is needed.

OUTLINE DIMENSIONS

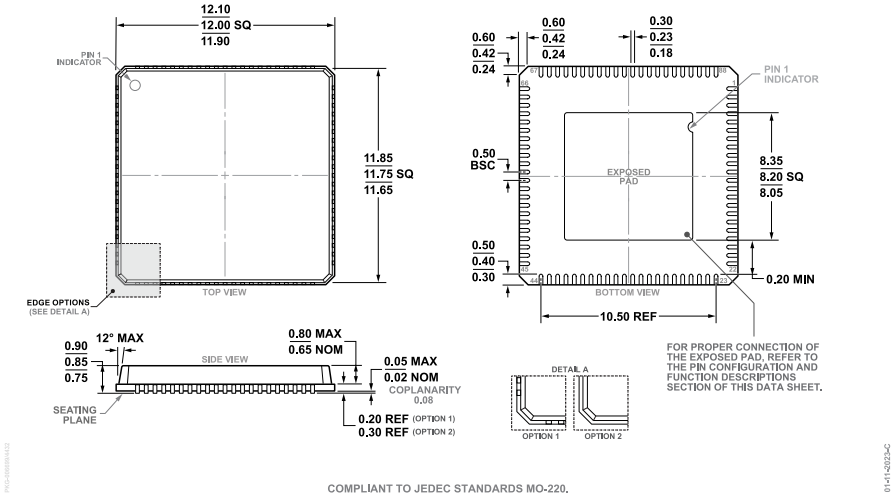

Figure 85. 88-Lead Lead Frame Chip Scale Package [LFCSP]
12 × 12 mm Body and 0.85 mm Package Height
(CP-88-4)
Dimensions shown in millimeters

Updated: December 05, 2023

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Packing Quantity	Package Option
AD9691BCPZ-1250	-40°C to +85°C	88-Lead LFCSP (12mm x 12mm w/ EP)		CP-88-4
AD9691BCPZRL7-1250	-40°C to +85°C	88-Lead LFCSP (12mm x 12mm w/ EP)	Reel, 400	CP-88-4

[1] Z = RoHS Compliant Part.

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