Kevin Duke

TI Precision Designs: Verified Design

Bipolar +/-10V Analog Output from a Unipolar Voltage Output DAC

TI Precision Designs

TI Precision Designs are analog solutions created by TI's analog experts. Verified Designs offer the theory, component selection, simulation, complete PCB schematic & layout, bill of materials, and measured performance of useful circuits. Circuit modifications that help to meet alternate design goals are also discussed.

Circuit Description

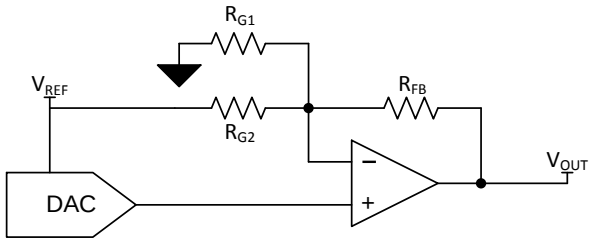
This unipolar to bipolar signal conditioning circuit uses an op amp with negative feedback and three resistors in a modified summing amplifier configuration to generate high-voltage bipolar outputs from a generic single supply unipolar digital-to-analog converter (DAC). This design will take consideration for generating voltage outputs commonly used in industrial process control applications and for driving reactive loads such as long cables also common in industrial applications. The fundamentals of the design can be extended to condition any unipolar DAC to any bipolar range of operation.

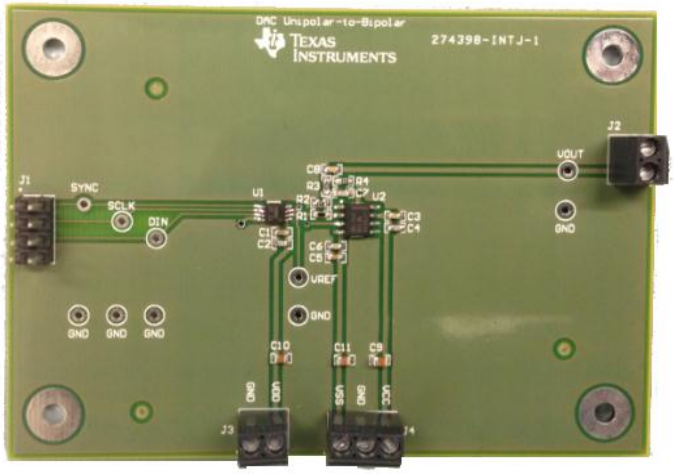
Design Resources

Design Archive	All Design files
TINA-TI™	SPICE Simulator
DAC8560	Product Folder
OPA188	Product Folder

TI E2E™ Community

Ask The Analog Experts
WEBENCH® Design Center
TI Precision Designs Library





1 Design Summary

The design requirements are as follows:

- DAC Supply Voltage: +5 V dc
- Amplifier Supply Voltage: ±15 V dc
- Input: 3-wire, 24-bit SPI
- Output: ±10 V dc

The design goals and performance are summarized in Table 1. Figure 1 depicts the measured transfer function of the design with a triangle wave output.

Table 1: Comparison of Design Goal, Simulation, and Measured Performance

	Goal	Simulated	Measured
Total Unadjusted Error (%FSR)	0.250	0.230	0.0939
Capacitive Drive (nF)	20	20	20

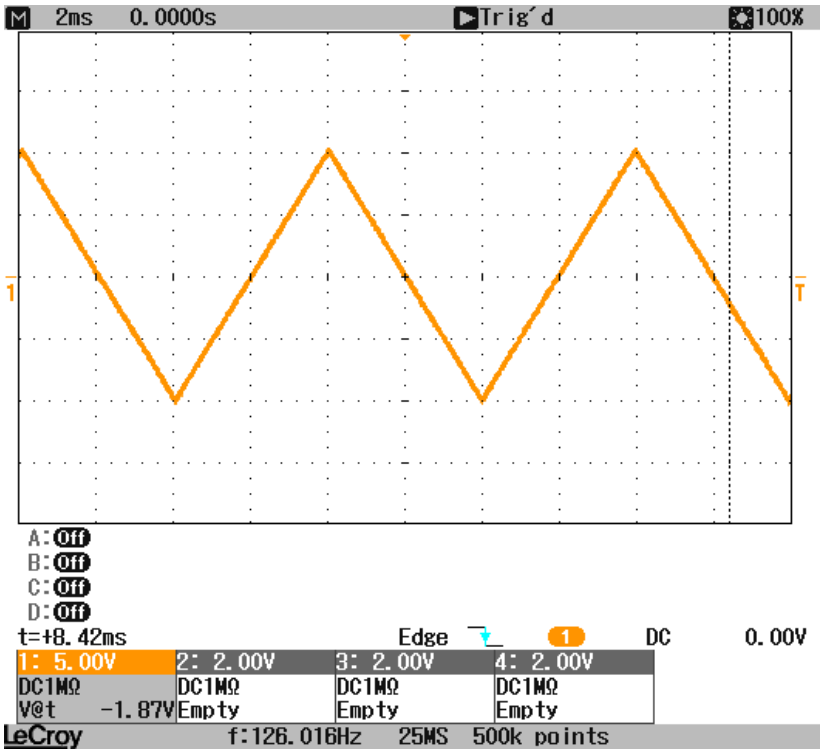


Figure 1: Full-Scale Output of Design

2 Theory of Operation

A more complete schematic for this design, including capacitive load compensation, is shown in Figure 2. The dc transfer function is based on the ratio of the feedback resistor R_{FB} and gain setting resistors R_{G1} and R_{G2}.

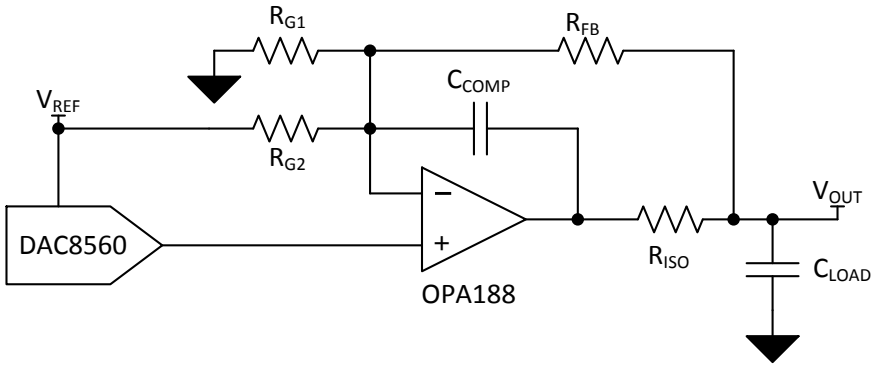


Figure 2: Complete Circuit Schematic

The dc transfer function for this design is defined as:

$$V_{OUT} = \left(1 + \frac{R_{FB}}{R_{G2}} + \frac{R_{FB}}{R_{G1}}\right) V_{DAC} - \frac{R_{FB}}{R_{G2}} V_{REF} \quad (1)$$

2.1 Choosing Resistor Values

The amplifier in this circuit uses negative feedback to ensure that the voltage at the inverting and non-inverting terminals are equal. When the DAC output is at zero-scale (0 V) the inverting terminal is a virtual ground so no current will flow across R_{G1}, this causes the circuit to function as an inverting amplifier with gain equal to R_{FB} / R_{G2}. When the DAC output is full-scale (V_{REF}) the inverting terminal potential is equal to V_{REF} so no current will flow across R_{G2}, this causes the circuit to function as a non-inverting amplifier with gain equal to (1 + R_{FB} / R_{G1}).

A simple three-step process can be used to select the resistor values used to realize any bipolar output range using any generic unipolar DAC. For this design V_{REF} was selected to be 2.5 V, a very common internal reference value for a generic DAC and a readily available external reference value. The desired output range for this design is ±10 V.

First, using the transfer function shown in Equation 1, consider the negative full-scale output case when V_{DAC} is equal to 0 V, V_{REF} is equal to 2.5 V, and V_{OUT} is equal to -10 V. This case is used to calculate the ratio of R_{FB} to R_{G2} and is shown explicitly in Equation 2.

$$-10V = \left(1 + \frac{R_{FB}}{R_{G2}} + \frac{R_{FB}}{R_{G1}}\right)(0) - \frac{R_{FB}}{R_{G2}}(2.5V) \quad (2)$$

$$-10V = -\frac{R_{FB}}{R_{G2}}(2.5V)$$

$$R_{FB} = 4 * R_{G2}$$

Second, consider the positive full-scale output case when V_{DAC} is equal to 2.5 V, V_{REF} is equal to 2.5 V, and V_{OUT} is equal to 10 V. This case is used to calculate the ratio of R_{FB} to R_{G1} and is shown explicitly in Equation 3.

$$10V = \left(1 + \frac{R_{FB}}{R_{G2}} + \frac{R_{FB}}{R_{G1}}\right)(2.5) - \frac{R_{FB}}{R_{G2}}(2.5V) \tag{3}$$

$$10V = \left(1 + \frac{R_{FB}}{R_{G1}}\right)(2.5V)$$

$$R_{G1} = \frac{R_{FB}}{3}$$

Finally, seed the ideal value of R_{G2} to calculate the ideal values of R_{FB} and R_{G2}. The key considerations for seeding the value of R_{G2} should be the drive strength of the reference source as well as choosing small resistor values to minimize noise contributed by the resistor network. For this design R_{G2} was chosen to be 8.25kΩ which will limit the peak current draw from the reference source to ~333µA under nominal conditions, which is well within the 20mA limit of the DAC8560. In this case, the ideal and nearest 0.1% tolerance, 0603 package values for each resistor are identical.

Table 2: Values of Resistor Network

Resistor	Value
R_{G1}	11kΩ
R_{G2}	8.25kΩ
R_{FB}	33kΩ

Standard values for 0.1% resistors can be an obstacle for this design and it may take multiple iterations of seeding the values to find real components or they may not exist. Work-arounds can include utilizing multiple resistors in series and/or parallel, using potentiometers for analog trim calibration, or providing extra gain in the output circuit and applying digital calibration. In systems where the output voltage must reach the design goal end-points (±10 V) it may be desirable to apply additional gain to the circuit. This approach may contribute additional overall system error since the end-point errors will vary from system to system. For this design, the exact values calculated in the design process will be used to keep error analysis easy to follow.

To deliver a “near-universal” cable drive solution, C_{LOAD} is chosen to be relatively large compared to typical cable capacitance such that its capacitance will dominate the reactive load seen by the output amplifier. To drive larger capacitive loads R_{ISO}, C_{COMP}, and C_{LOAD} may need to be adjusted.

3 Component Selection

3.1 DAC Selection

For convenience, devices with an external reference option or devices with accessible internal references are desirable in this application since the reference is used to create an offset. The DAC selection in this design should primarily be based on dc error contributions typically described by offset-error, gain-error, and integral non-linearity error. Occasionally additional specifications are provided that summarize end-point errors of the DAC typically called zero-code error and full-scale error. For ac applications additional consideration may be placed on slew rate and settling time.

3.2 Amplifier Selection

Amplifier input offset voltage (V_{OS}) is a key-consideration for this design. V_{OS} of an operational amplifier is a typical datasheet specification but in-circuit performance is also impacted by drift over temperature, the common-mode rejection ratio (CMRR), and power supply rejection ratio (PSRR) so consideration should be given to these parameters as well. For ac operation additional considerations should be made concerning slew rate and settling time. Input-bias current (I_B) can also be a factor, but typically the resistor network is implemented with sufficiently small resistor values that the effects of input-bias current are negligible.

3.3 Passive Component Selection

Resistor matching for the op amp resistor network is critical for the success of this design and components should be chosen with tight tolerances. For this design 0.1% resistor values are implemented but this constraint may be adjusted based on application specific design goals. Resistor matching will contribute to both offset error and gain error in this design, as shown in the simulation section of this document. The tolerance of stability components R_{ISO} and C_{COMP} is not critical and 1% components are acceptable.

4 Simulation

4.1 DAC DC Transfer Function

The TINA-TI™ schematic shown in Figure 3 implements the circuit using an ideal op amp and the ideal resistor values as obtained in the design process. This model is used to simulate system offset and gain errors that are contributed by the DAC8560. The DAC8560 is modeled by an ideal voltage source sweeping from 0 V to 2.50 V along with a non-inverting amplifier with gain to simulate the effects of the DAC8560 typical gain error of ±0.05% FSR. Additionally, a series voltage source of 5 mV is included to model the typical DAC8560 offset error. Since an INL model is not as straight forward, it will be calculated from the datasheet. This will not mimic the real device behavior since it does not include a zero-code error model, but will be sufficient to estimate performance over the linear region of operation of the DAC.

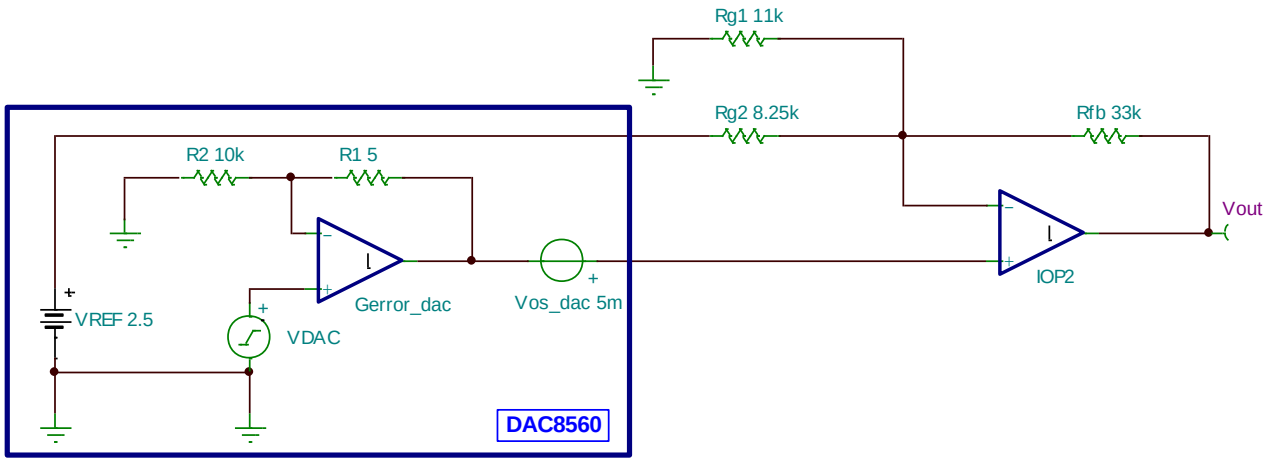


Figure 3: TINA-TI™ - DAC End-Point Error Schematic

The dc transfer function simulation results of the circuit in Figure 3 are shown in Figure 3 and Figure 4. The results will be used along with the simulation results of the op amp and resistor tolerances to determine overall system offset error, gain error, and total unadjusted error (TUE).

Table 3: Simulated DAC Performance

Parameter	Simulated Value
Negative Full-Scale Voltage (V)	-9.96
Zero-Scale Voltage (V)	0.04
Positive Full-Scale Voltage (V)	10.05
Offset Error (% FSR)	0.200
Gain Error (% FSR)	0.050
INL Error (%FSR)	0.006
Total Unadjusted Error (%FSR)	0.206

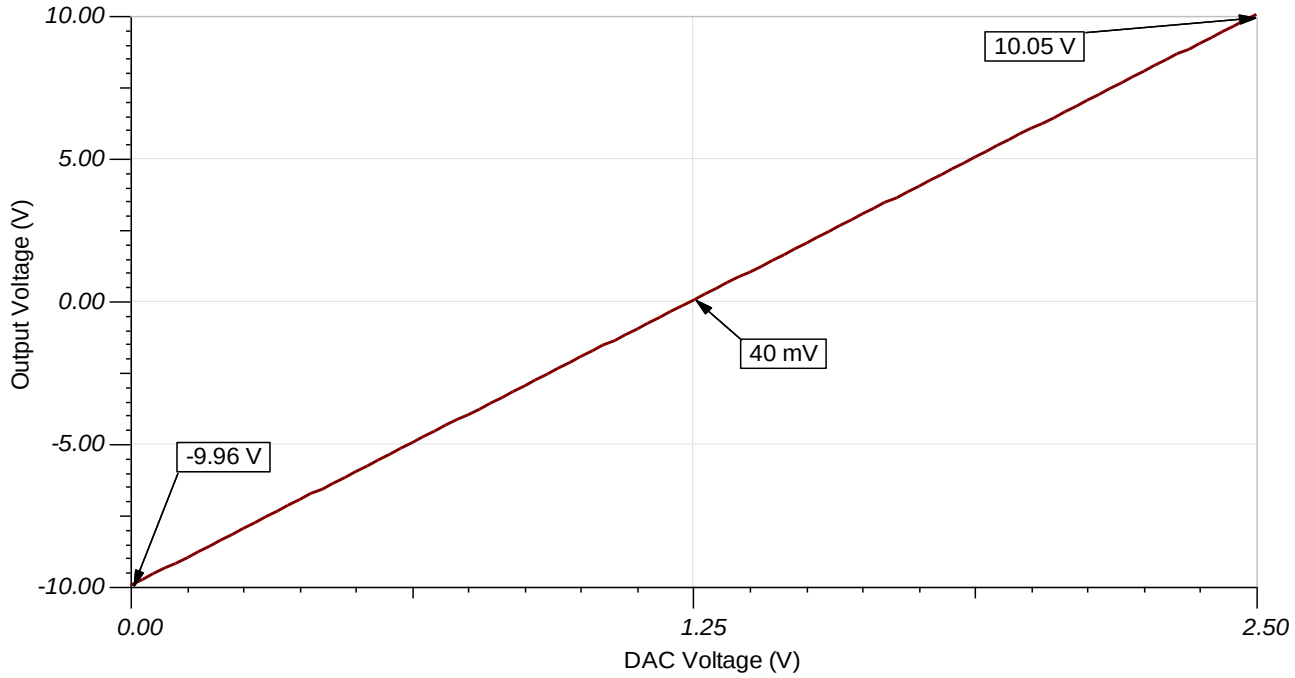


Figure 4: TINA-TI™ - DC Transfer Characteristic

The following equations were used to calculate the error parameters in Table 3 based on the information in Figure 4. The total unadjusted error equation uses a root-sum-squared (RSS) technique to sum uncorrelated error sources.

$$OffsetError_{(\%FSR)} = \left(\frac{V_{OUT\ MidScale}}{V_{OUT\ Ideal(MAX)} - V_{OUT\ Ideal(MIN)}} \right) * 100 \quad (4)$$

$$GainError_{\%FSR} = \frac{\left| \left(V_{OUT_{(MAX)}} - V_{OUT_{(MIN)}} \right) - \left(V_{OUT_{Ideal(MAX)}} - V_{OUT_{Ideal(MIN)}} \right) \right|}{V_{OUT_{Ideal(MAX)}} - V_{OUT_{Ideal(MIN)}}} * 100 \quad (5)$$

$$INLERROR_{(\%FSR)} = \frac{INLERROR_{LSB} * LSB * GAIN}{V_{OUT_{Ideal(MAX)}} - V_{OUT_{Ideal(MIN)}}} * 100 \quad (6)$$

$$TUE_{\%FSR} = \sqrt{OffsetError_{\%FSR}^{\ 2} + GainError_{\%FSR}^{\ 2} + INLERROR_{\%FSR}^{\ 2}} \quad (7)$$

4.2 Op Amp & Passives DC Transfer Function

The TINA-TI™ schematic shown in Figure 5 implements the OPA188 model and Monte-Carlo analysis for the resistor network with 0.1% tolerances and a normal distribution. In this simulation the DAC will be represented by an ideal voltage source sweeping from 0 V to 2.5 V. This model is used to simulate the offset error and gain error contributed by the resistors and op amp. The Monte Carlo dc transfer function is depicted in Figure 6.

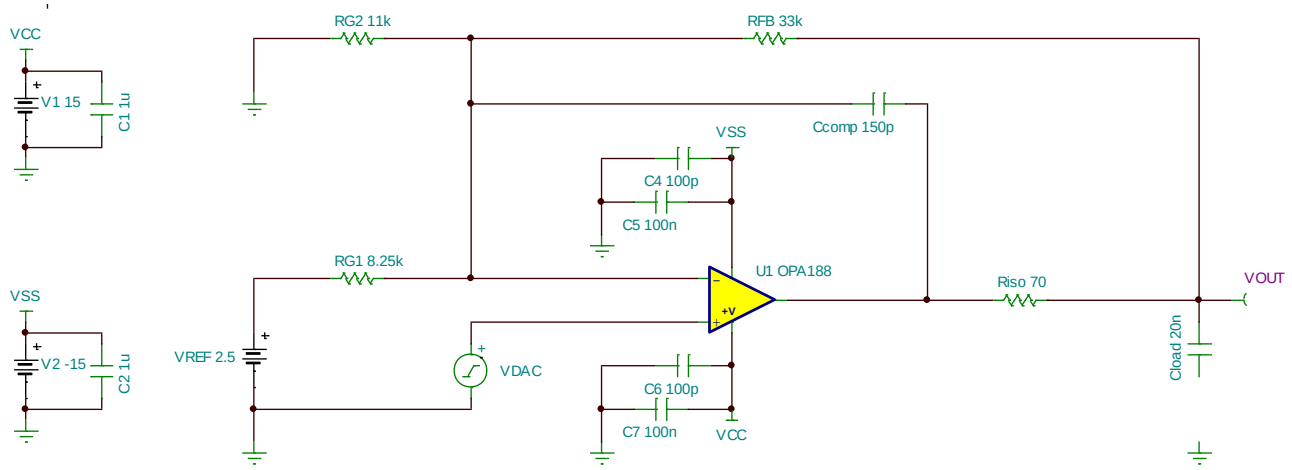


Figure 5: TINA-TI™ - DC Transfer Characteristic

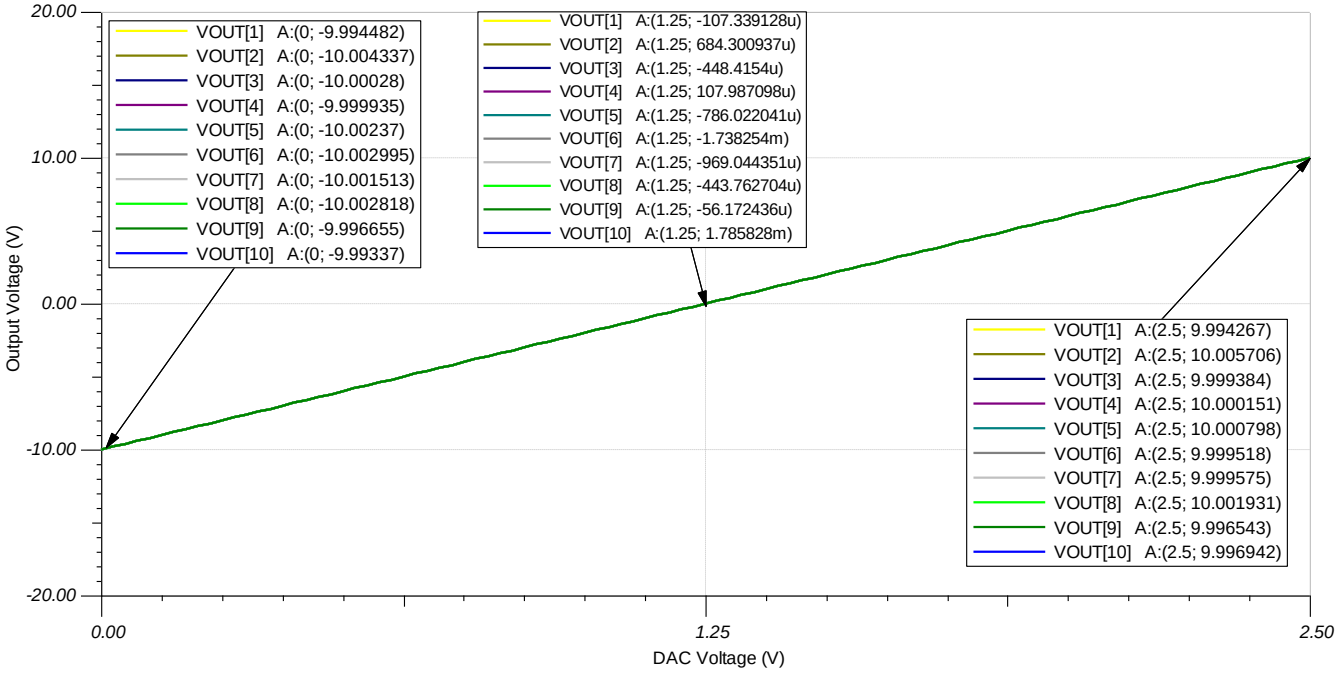


Figure 6: TINA-TI™ - Monte-Carlo Simulation of Output Circuit

The results of a 10 iteration Monte-Carlo simulation of the output circuit are shown in Table 4.

Table 4: Output Circuit Monte-Carlo Results

	Min	Max	Average	Std. Dev. (σ)
Offset Error (mV)	-1.738	1.785	-0.197	0.958
Full-Scale Range (V)	19.988	20.010	19.999	0.006
Full-Scale |Error| (mV)	0.086	11.251	4.972	N/A

The standard deviation of the Monte-Carlo results can be used to generate a more realistic error figure for the system by multiplying the standard deviation by 3, commonly referred to as a 3-σ system. This error figure should encompass 99.7% of the systems, leaving out absolute worst-case resistor mis-matches that are highly unlikely to occur. These errors are summarized in Table 5. The equations used to calculate each error are shown below:

$$OffsetError_{(\%FSR)} = \frac{3*\sigma_{OffsetError}}{V_{OUT_{Ideal(MAX)}} - V_{OUT_{Ideal(MIN)}}} * 100 \quad (8)$$

$$GainError_{(\%FSR)} = \frac{3*\sigma_{GainError}}{V_{OUT_{Ideal(MAX)}} - V_{OUT_{Ideal(MIN)}}} * 100 \quad (9)$$

Table 5: Simulated Output Circuit Performance

Parameter	Simulated Value
Offset Error (% FSR)	0.0143
Gain Error (% FSR)	0.1004
INL Error (%FSR)	0.0000
Total Unadjusted Error (%FSR)	0.1014

4.3 System dc Transfer Function

The combined accuracy of simulation results of the DAC and output circuit are summarized in Table 6. The values were calculated using a RSS technique similar to that shown in Equation 7. The output circuit contributes very low error to the system which allows for the DACs performance to dominate what is seen at the output. In this case the DAC errors are gained up by 8 since the 0-2.5 V range was scaled up to ±10 V. If less gain is applied to the DAC output signal its error contributions will decrease.

Table 6: Simulated Circuit Performance

Parameter	Simulated Value
Offset Error (% FSR)	0.200
Gain Error (% FSR)	0.112
INL Error (%FSR)	0.012
Total Unadjusted Error (%FSR)	0.230

4.4 Step Response

The step response of the design is shown in Figure 7. The results show that the output settles to the proper value with very little overshoot and ringing while driving the 20nF C_{LOAD}, indicating a stable design. The stable response was obtained by manipulating the compensation components, R_{ISO} and C_{COMP}. See Reference 1 more information on stability.

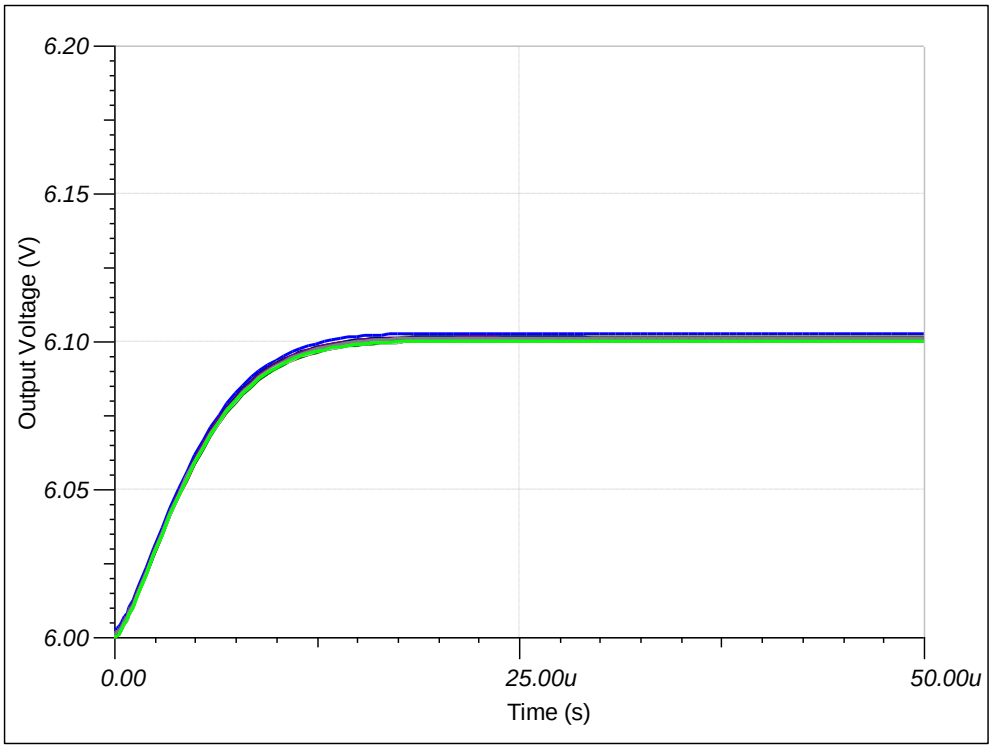


Figure 7: TINA-TI™ - Step Response

5 PCB Design

The PCB schematic and bill of materials can be found in Appendix A.

5.1 PCB Layout

The PCB layout for this design is shown in Figure 8. For this layout follow general PCB layout guidelines. Pay particular attention to placement and routing of the summing node at the inverting input of the op amp. This node should be kept small, placed as close to the inverting input terminal as possible, and a pour cut out should be included on all pours below the inverting node to reduce parasitic capacitance.

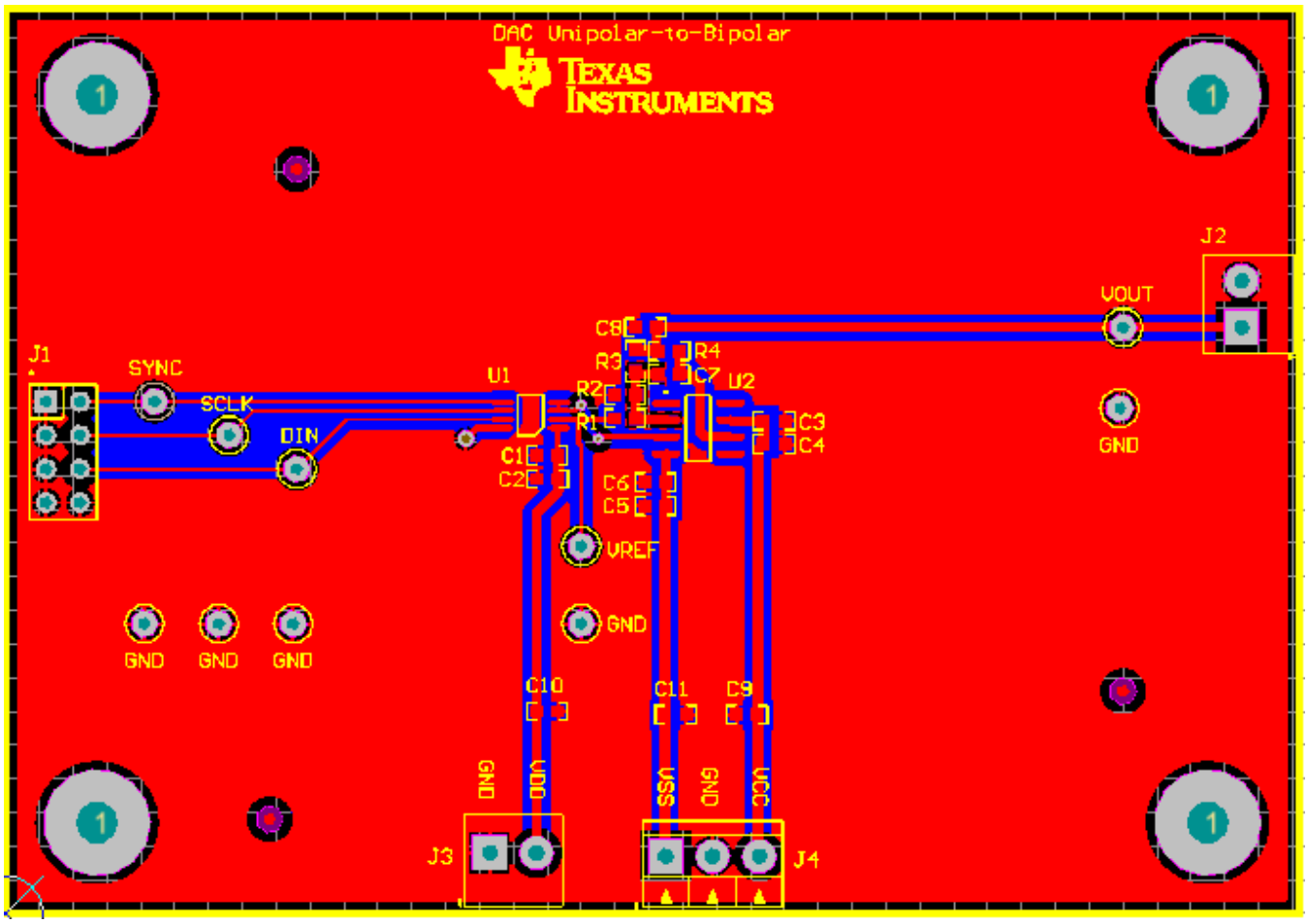


Figure 8: PCB Layout

6 Verification & Measured Performance

6.1 Transfer Function

The graph in Figure 9 was collected by applying input codes ranging from 0 to 65535 to the DAC and measuring the output voltage on a single system.

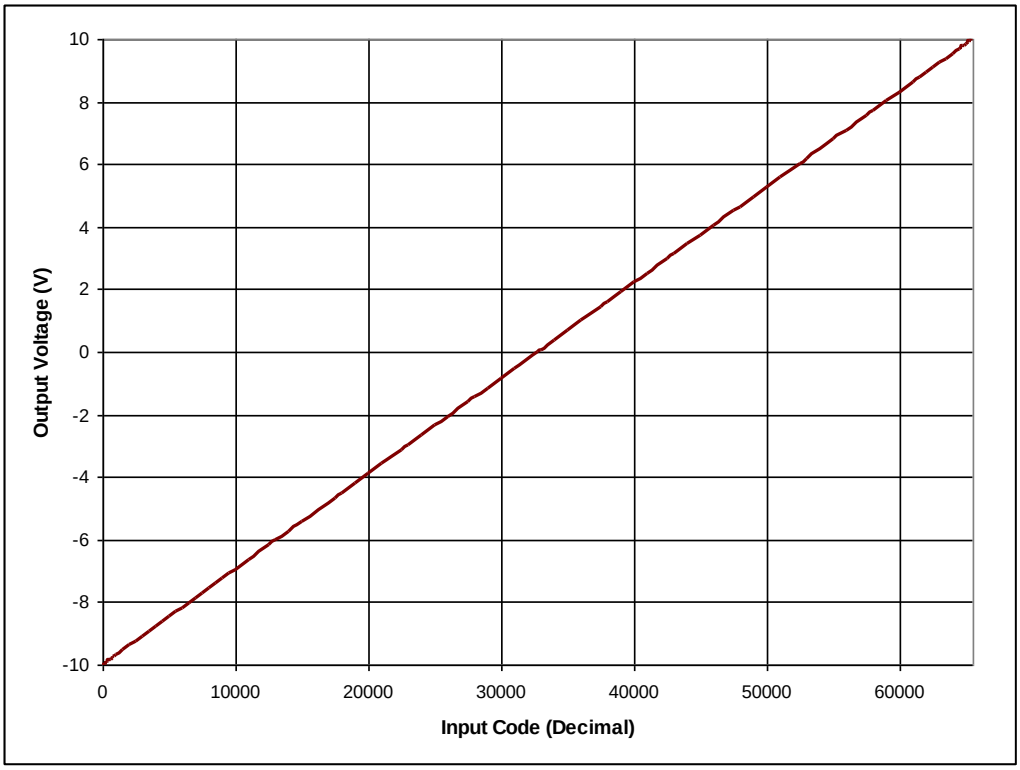


Figure 9: Output Voltage vs. Input Code

To easily visualize the error of the system the difference between the ideal output voltage and measured output voltage of the circuit in %FSR is plotted in Figure 10. The average error across the full-scale range of codes shown in Figure 10 is 0.017%FSR and the two-point line of best fit analysis of the same unit indicates a total unadjusted error of 0.0167%FSR – indicating that the two-point line of best fit is an accurate estimate of typical system accuracy, although there are outliers.

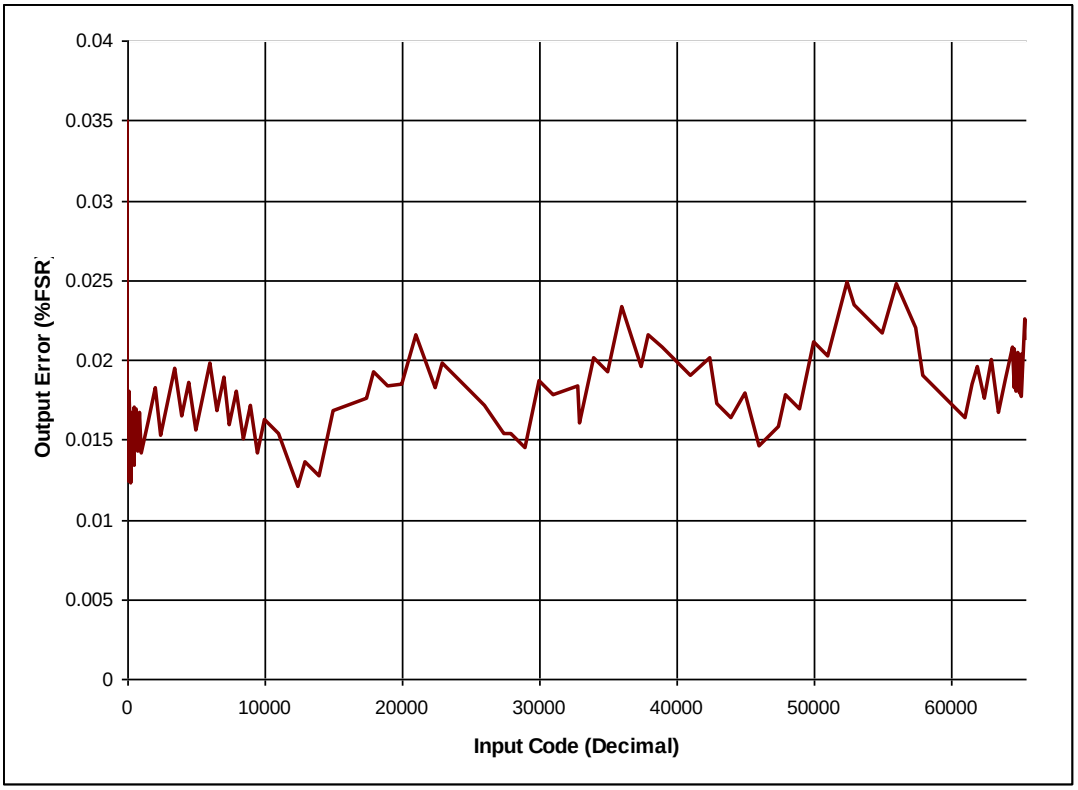


Figure 10: Output Voltage Error vs. Input Code

The average results observed over 8 units are shown in Table 7. These results were measured using a two-point line of best fit measured at codes 485 and 64714 to be consistent with the specifications provided in the DAC8560 datasheet. The equations used to calculate these values are shown in Equations 10 and 11.

Table 7: Measured Circuit Performance

Parameter	Measured Value
Offset Error (% FSR)	0.0705
Gain Error (% FSR)	0.0125
INL Error (%FSR)	0.0060
Total Unadjusted Error (%FSR)	0.0939

$$GainError_{(\%FSR)} = \frac{\left(V_{OUT_{REAL(64714)}} - V_{OUT_{REAL(485)}}\right) - \left(V_{OUT_{IDEAL(64714)}} - V_{OUT_{IDEAL(485)}}\right)}{V_{OUT_{IDEAL(64714)}} - V_{OUT_{IDEAL(485)}}} * 100 \quad (10)$$

$$OffsetError_{(\%FSR)} = \frac{V_{OUT_{REAL(485)}} - \left(\frac{V_{OUT_{REAL(64714)}} - V_{OUT_{REAL(485)}}}{64714 - 485} * 485\right) - 10}{V_{OUT_{IDEAL(MAX)}} - V_{OUT_{IDEAL(MIN)}}} * 100 \quad (11)$$

6.2 Transient Response

To observe a full-scale step response and settling time of the system, a square wave corresponding to the zero-scale code and full-scale code were applied to the digital inputs of the DAC. Figure 11 shows this step response.

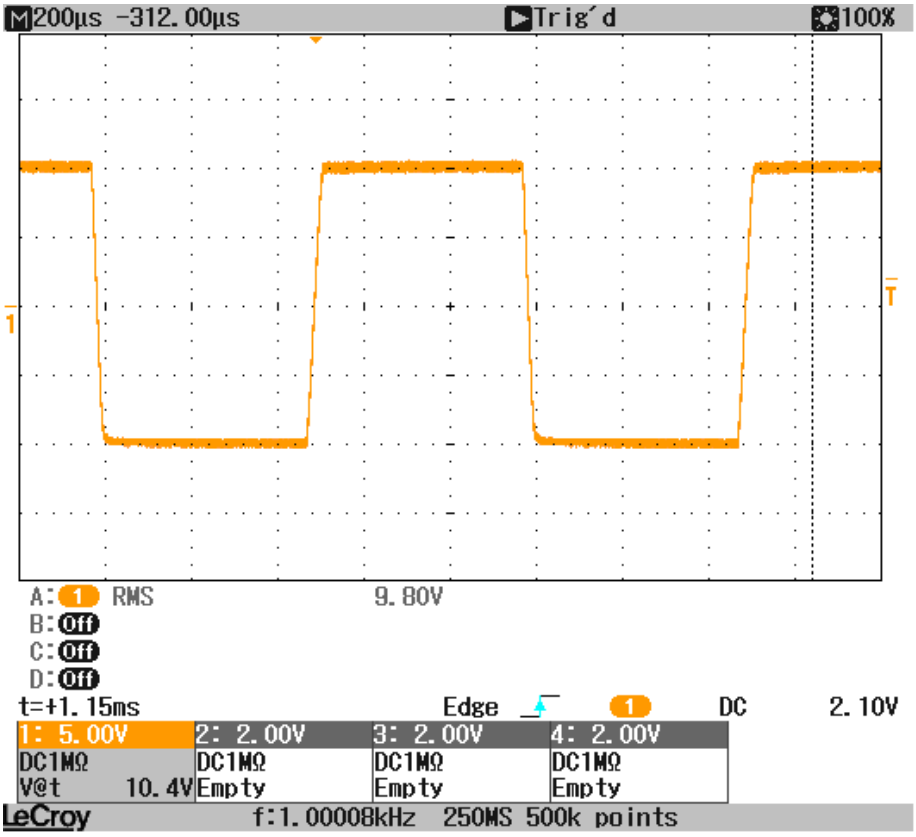


Figure 11: Full-Scale Step Response

To test the small signal stability of the design a digital input corresponding to a 200mV output step response centered about midscale output of the system was applied to the DAC. Figure 12 illustrates the resulting step response that shows a small period of digital feedthrough followed by very little overshoot or ringing, indicating a stable design.

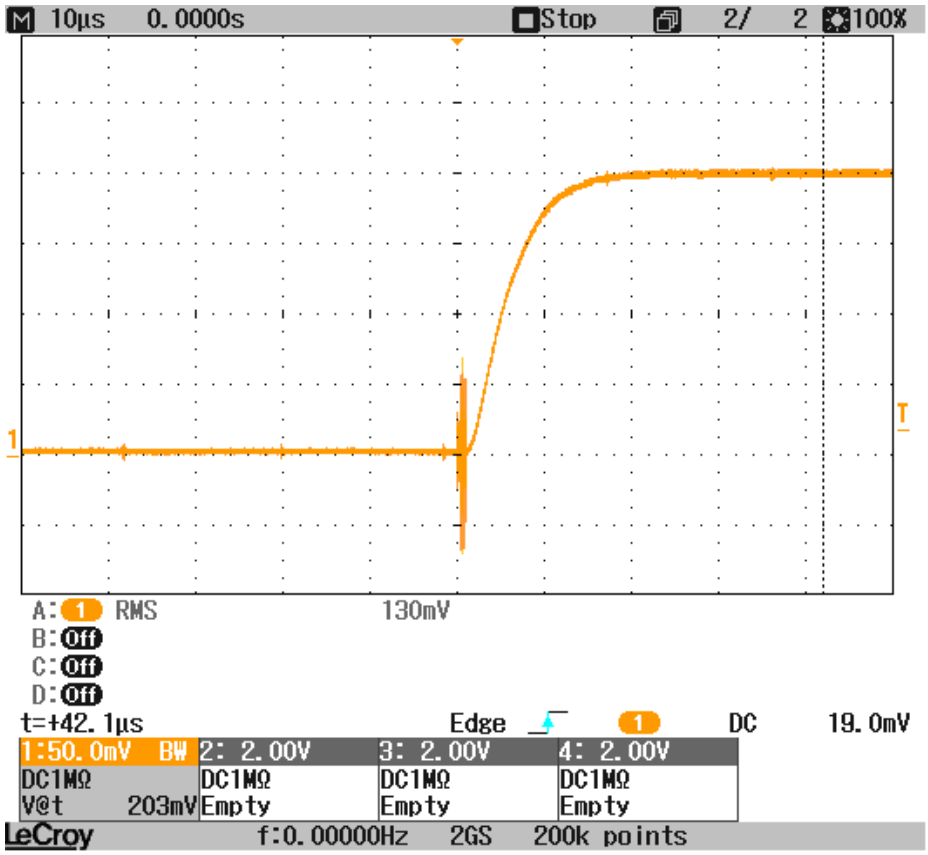


Figure 12: Small-Signal Stability

7 Modifications

The components selected in this design were chosen based on the design goals outlined at the beginning of this document. The DAC selection can be very open since the output circuit is applicable to any device and should be made based on specific design goals. Alternative DACs may provide enhanced linearity, gain error, and offset error as well as alternative interface options, channel count, resolution, and other auxiliary features. Table 7 shows a few DACs that may be used in place of the DAC8560.

Modifications to improve the accuracy of this design are possible by choosing a more precise DAC and by utilizing an external reference source. For this design, delivering a very low-cost solution was a critical parameter and some sacrifices were made. Additionally, the implementation of external calibration can greatly enhance results.

Table 8: Alternate DAC Options

DAC	Gain Error (Typ)	Offset Error (Typ)	INL Error (Typ)	Resolution	Channel Count
DAC8560	±0.05 %FSR	±5 mV	±8 LSB	16 bits	1
DAC8562/3	±0.01 %FSR	±1 mV	±4 LSB	16 bits	2
DAC8564	±0.05 %FSR	±5 mV	±4 LSB	16 bits	4
DAC8568	±0.01 %FSR	±1 mV	±4 LSB	16 bits	8
DAC8411	±0.05 %FSR	±0.05 mV	±1 LSB	16 bits	1
DAC8881	±4 LSB	±4 LSB	±0.5 LSB	16 bits	1

The OPA188 is an excellent wide-supply amplifier with very low input offset voltage and input offset voltage drift due to its chopper topology. Other op amps may be selected that offer lower noise, zero cross-over distortion, or higher bandwidth. Designs that deliver a smaller output range have many more options available since the supply voltage requirements are lowered.

Table 9: Alternate Op Amp Options

Amplifier	Max Supply Voltage	Offset Voltage (Typ)	Offset Drift (Typ)	Bandwidth	Quiescent Current
OPA180	36 V	15 µV	0.1 µV/C	2 MHz	450 µA
OPA188	36 V	6 µV	0.085 µV/C	2 MHz	450 µA
OPA170	36 V	0.25 mV	0.3 µV/C	1.2 MHz	110 µA
OPA211	36 V	30 µV	0.35 µV/C	80 MHz	3.6 µA
OPA227	36 V	10 µV	0.1 µV/C	1 MHz	790 µA
OPA140	36 V	30 µV	0.35 µV/C	11 MHz	1.8 mA
OPA277	36 V	10 µV	0.1 µV/C	1 MHz	790 µA

8 About the Author

Kevin Duke is an applications engineer in the precision digital to analog converters group at Texas Instruments where he supports industrial and catalog products and applications. Kevin received his BSEE from Texas Tech University in 2010.

9 Acknowledgements & References

1. *T. Green (2012).*
Operational Amplifier Stability, Part 10 of 15: Capacitor Loop Stability: Riso with Dual Feedback.
Available: http://www.en-genius.net/site/zones/acquisitionZONE/technical_notes/acqt_050712

Appendix A.

A.1 Electrical Schematic

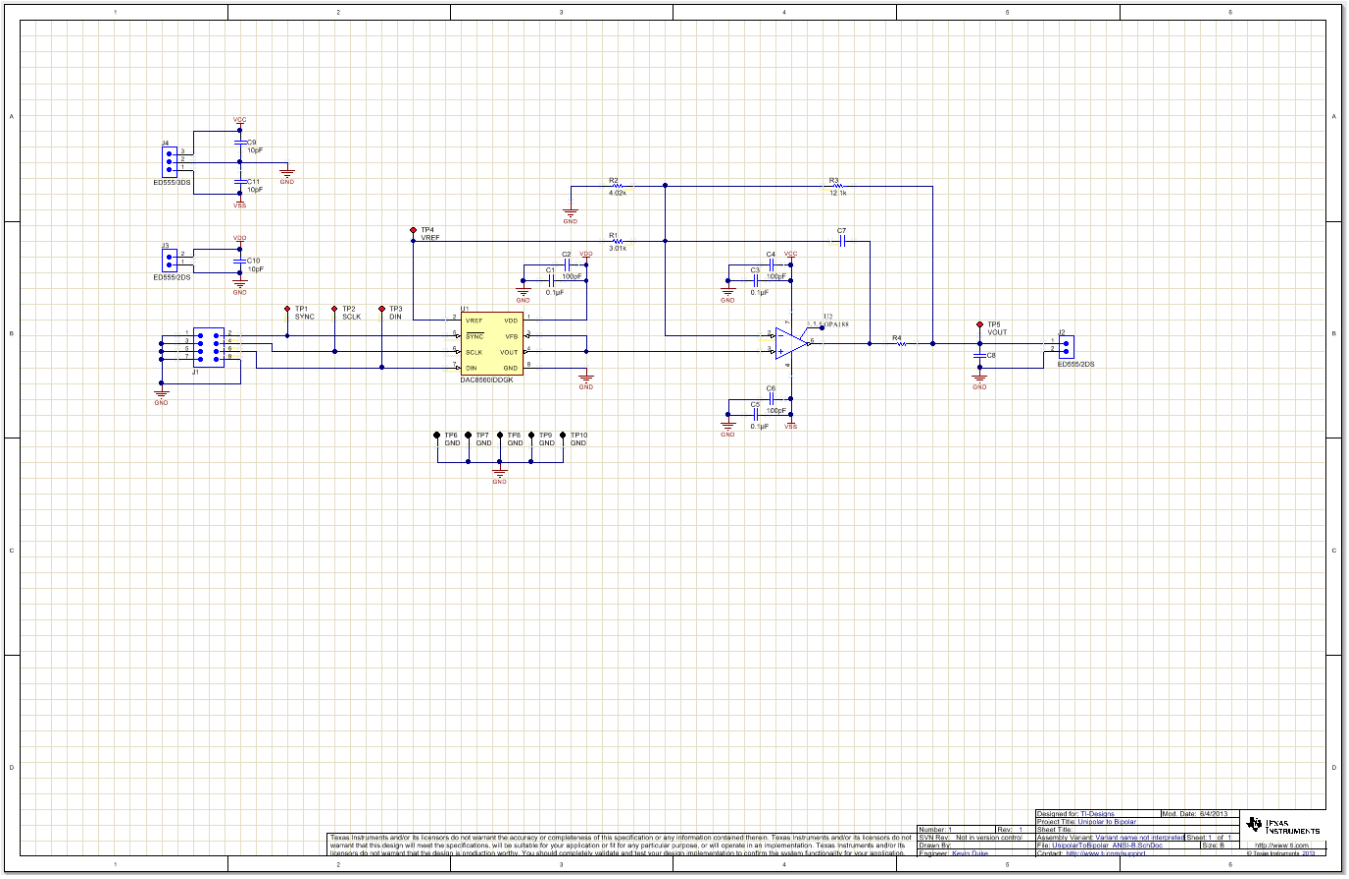


Figure A-1: Electrical Schematic

Passive Name in Text	Passive Name in Schematic
R_{G1}	R1
R_{G2}	R2
R_{FB}	R3
R_{ISO}	R4
C_{COMP}	C7

A.2 Bill of Materials

Texas Instruments

Bill of Materials

TI DESIGNS

TIPD137: ±10V 4-Quadrant Multiplying DAC

Item #	Quantity	Designator	Value	Description	Manufacturer	PartNumber
1	3	C1, C3, C5	0.1uF	CAP, CERM, 0.1uF, 25V, +/-5%, X7R, 0603	AVX	06033C104JAT2A
2	3	C2, C4, C6	100pF	CAP, CERM, 100pF, 50V, +/-5%, C0G/NP0, 0603	AVX	06035A101JAT2A
3	1	C7	150pF	CAP CER 150PF 50V 1% NP0 0603	TDK	C1608C0G1H151F080AA
4	1	C8	20nF	CAP CER 0.02UF 50V 10% X7R 0603	Samsung	CL10B203KB8NNNC
5	1	R4	71.5	RES 71.5 OHM 1/10W 1% 0603 SMD	Panasonic	ERJ-3EKF71R5V
6	3	C9, C10, C11	10pF	CAP, CERM, 10pF, 50V, +/-5%, C0G/NP0, 0603	MuRata	GRM1885C1H100JA01D
7	1	J1		Header, TH, 100mil, 4x2, Gold plated, 230 mil above insulator	Samtec, Inc.	TSW-104-07-G-D
8	2	J2, J3		Terminal Block, 6A, 3.5mm Pitch, 2-Pos, TH	On-Shore Technology, Inc.	ED555/2DS
9	1	J4		Terminal Block, 6A, 3.5mm Pitch, 3-Pos, TH	On-Shore Technology, Inc.	ED555/3DS
10	1	R1	8.25k	RES 8.25K OHM 1/10W .1% 0603 SMD	Susumu	RG1608P-8251-B-T5
11	1	R2	11.0k	RES 11.0K OHM 1/10W .1% 0603 SMD	Susumu	RG1608P-113-B-T5
12	1	R3	33.0k	RES 33.0K OHM 1/10W .1% 0603 SMD	Susumu	RG1608P-333-B-T5
13	1	TP1, TP2, TP3, TP4, TP5	Red	Test Point, Miniature, Red, TH	Keystone	5000
14	5	TP6, TP7, TP8, TP9, TP10	Black	Test Point, Miniature, Black, TH	Keystone	5001
15	1	U1		16-Bit, Ultra-Low Glitch, Voltage Output Digital-to-Analog Converter	Texas Instruments	DAC8560IDDGK
16	1	U2		Wideband, Low-Power Voltage Feedback Operational Amplifier	Texas Instruments	OPA188AIDR

Figure A-2: Bill of Materials

IMPORTANT NOTICE FOR TI REFERENCE DESIGNS

Texas Instruments Incorporated ("TI") reference designs are solely intended to assist designers (“Buyers”) who are developing systems that incorporate TI semiconductor products (also referred to herein as “components”). Buyer understands and agrees that Buyer remains responsible for using its independent analysis, evaluation and judgment in designing Buyer’s systems and products.

TI reference designs have been created using standard laboratory conditions and engineering practices. **TI has not conducted any testing other than that specifically described in the published documentation for a particular reference design.** TI may make corrections, enhancements, improvements and other changes to its reference designs.

Buyers are authorized to use TI reference designs with the TI component(s) identified in each particular reference design and to modify the reference design in the development of their end products. HOWEVER, NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY THIRD PARTY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT, IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI REFERENCE DESIGNS ARE PROVIDED "AS IS". TI MAKES NO WARRANTIES OR REPRESENTATIONS WITH REGARD TO THE REFERENCE DESIGNS OR USE OF THE REFERENCE DESIGNS, EXPRESS, IMPLIED OR STATUTORY, INCLUDING ACCURACY OR COMPLETENESS. TI DISCLAIMS ANY WARRANTY OF TITLE AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, QUIET ENJOYMENT, QUIET POSSESSION, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS WITH REGARD TO TI REFERENCE DESIGNS OR USE THEREOF. TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY BUYERS AGAINST ANY THIRD PARTY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON A COMBINATION OF COMPONENTS PROVIDED IN A TI REFERENCE DESIGN. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, SPECIAL, INCIDENTAL, CONSEQUENTIAL OR INDIRECT DAMAGES, HOWEVER CAUSED, ON ANY THEORY OF LIABILITY AND WHETHER OR NOT TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES, ARISING IN ANY WAY OUT OF TI REFERENCE DESIGNS OR BUYER’S USE OF TI REFERENCE DESIGNS.

TI reserves the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products are sold subject to TI’s terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI’s terms and conditions of sale of semiconductor products. Testing and other quality control techniques for TI components are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers’ products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers’ products and applications, Buyers should provide adequate design and operating safeguards.

Reproduction of significant portions of TI information in TI data books, data sheets or reference designs is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards that anticipate dangerous failures, monitor failures and their consequences, lessen the likelihood of dangerous failures and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in Buyer’s safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI’s goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed an agreement specifically governing such use.

Only those TI components that TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components that have ***not*** been so designated is solely at Buyer's risk, and Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265