NCP360, NCV360

USB Positive Overvoltage Protection Controller with Internal PMOS FET and Status FLAG

The NCP360 disconnects systems at its output when wrong VBUS operating conditions are detected at its input. The system is positive overvoltage protected up to +20 V.

Thanks to an integrated PMOS FET, no external device is necessary, reducing the system cost and the PCB area of the application board.

The NCP360 is able to instantaneously disconnect the output from the input if the input voltage exceeds the overvoltage threshold (OVLO).

The NCP360 provides a negative going flag ($\overline{\text{FLAG}}$) output, which alerts the system that a fault has occurred.

In addition, the device has ESD−protected input (15 kV Air) when bypassed with a 1 μF or larger capacitor.

Features

- Very Fast Protection, Up to 20 V, with 25 μA Current Consumption
- On−chip PMOS Transistor
- Overvoltage Lockout (OVLO)
- Undervoltage Lockout (UVLO)
- Alert $\overline{\text{FLAG}}$ Output
- $\overline{\text{EN}}$ Enable Pin
- Thermal Shutdown
- Compliance to IEC61000−4−2 (Level 4)
  8 kV (Contact)
  15 kV (Air)
- ESD Ratings: Machine Model = B
  Human Body Model = 2
- 6 Lead UDFN 2x2 mm Package
- 5 Lead TSOP 3x3 mm Package
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable
- These are Pb−Free Devices

Applications

- USB Devices
- Mobile Phones
- Peripheral
- Personal Digital Applications
- MP3 Players

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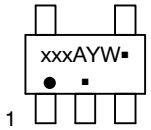
MARKING DIAGRAMS

UDFN6
MU SUFFIX
CASE 517AB

M = Date Code
▪ = Pb−Free Package

TSOP−5
SN SUFFIX
CASE 483



A = Assembly Location
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 11 of this data sheet.

PIN CONNECTIONS

(Top Views)

PIN FUNCTION DESCRIPTION (UDFN6 Package)

Pin No.	Name	Type	Description
1	$\overline{EN}$	INPUT	Enable Pin. The device enters in shutdown mode when this pin is tied to a high level. In this case the output is disconnected from the input. To allow normal functionality, the $\overline{EN}$ pin shall be connected to GND or to a I/O pin. This pin does not have an impact on the fault detection.
2	GND	POWER	Ground
3	IN	POWER	Input Voltage Pin. This pin is connected to the VBUS. A 1 μF low ESR ceramic capacitor, or larger, must be connected between this pin and GND.
4, 5	OUT	OUTPUT	Output Voltage Pin. The output is disconnected from the VBUS power supply when the input voltage is above OVLO threshold or below UVLO threshold. A 1 μF capacitor must be connected to these pins. The two OUT pins must be hardwired to common supply.
6	$\overline{FLAG}$	OUTPUT	Fault Indication Pin. This pin allows an external system to detect a fault on VBUS pin. The $\overline{FLAG}$ pin goes low when input voltage exceeds OVLO threshold. Since the $\overline{FLAG}$ pin is open drain functionality, an external pull up resistor to V_{CC} must be added.
–	PAD1	POWER	Exposed Pad. Can be connected to GND or isolated plane. Must be used to thermal dissipation.

PIN FUNCTION DESCRIPTION (TSOP−5 Package)

Pin No.	Name	Type	Description
1	IN	POWER	Input Voltage Pin. This pin is connected to the VBUS. A 1 μF low ESR ceramic capacitor, or larger, must be connected between this pin and GND.
2	GND	POWER	Ground
3	$\overline{EN}$	INPUT	Enable Pin. The device enters in shutdown mode when this pin is tied to a high level. In this case the output is disconnected from the input. To allow normal functionality, the $\overline{EN}$ pin shall be connected to GND or to a I/O pin. This pin does not have an impact on the fault detection.
4	$\overline{FLAG}$	OUTPUT	Fault Indication Pin. This pin allows an external system to detect a fault on VBUS pin. The $\overline{FLAG}$ pin goes low when input voltage exceeds OVLO threshold. Since the $\overline{FLAG}$ pin is open drain functionality, an external pull up resistor to V_{CC} must be added.
5	OUT	OUTPUT	Output Voltage Pin. The output is disconnected from the VBUS power supply when the input voltage is above OVLO threshold or below UVLO threshold. A 1 μF capacitor must be connected to this pin.

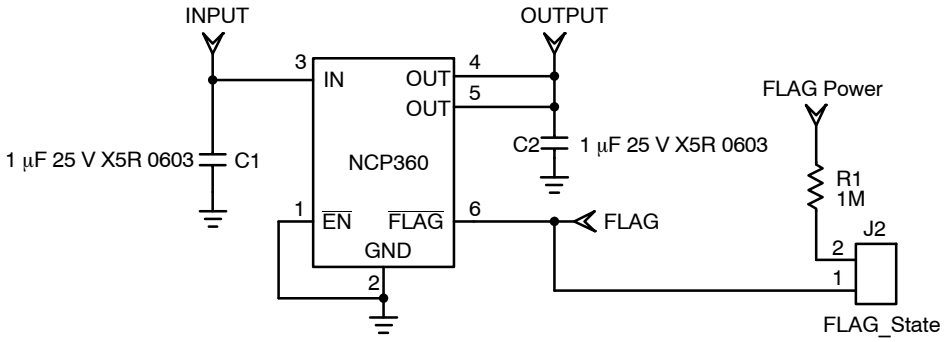


Figure 1. Typical Application Circuit (UDFN Pinout)

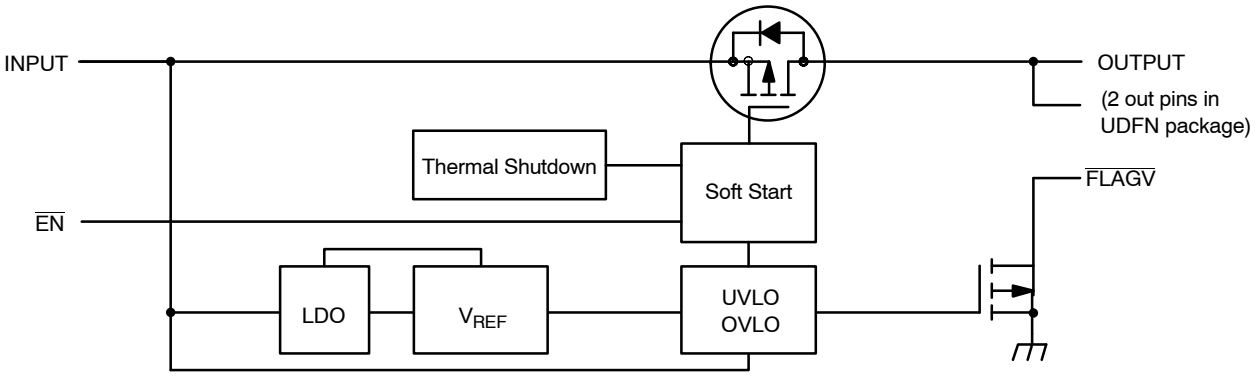


Figure 2. Functional Block Diagram

MAXIMUM RATINGS

Rating		Symbol	Value	Unit
Minimum Voltage (IN to GND)		$Vmin_{in}$	−0.3	V
Minimum Voltage (All others to GND)		Vmin	−0.3	V
Maximum Voltage (IN to GND)		$Vmax_{in}$	21	V
Maximum Voltage (All others to GND)		Vmax	7.0	V
Maximum Current from Vin to Vout (PMOS) (Note 1)		Imax	600	mA
Thermal Resistance, Junction−to−Air (Note 2)	TSOP−5 UDFN	$R_{\theta JA}$	305 260	°C/W
Operating Ambient Temperature Range		T_A	−40 to +85	°C
Storage Temperature Range		T_{stg}	−65 to +150	°C
Junction Operating Temperature		T_J	150	°C
ESD Withstand Voltage (IEC 61000−4−2) Human Body Model (HBM), Model = 2 (Note 3) Machine Model (MM) Model = B (Note 4)		Vesd	15 Air, 8.0 Contact 2000 200	kV V V
Moisture Sensitivity		MSL	Level 1	−

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. With minimum PCB area. By decreasing $R_{\theta JA}$, the current capability increases. See PCB recommendation page 9.
2. $R_{\theta JA}$ is highly dependent on the PCB heat sink area (connected to PAD1, UDFN). See PCB Recommendations.
3. Human Body Model, 100 pF discharged through a 1.5 kΩ resistor following specification JESD22/A114.
4. Machine Model, 200 pF discharged through all pins following specification JESD22/A115.
5. Compliant with JEDEC Latch−up Test, up to maximum voltage range.

ELECTRICAL CHARACTERISTICS

(Min/Max limits values (−40°C < T_A < +85°C) and V_{in} = +5.0 V. Typical values are T_A = +25°C, unless otherwise noted.)

Characteristic	Symbol	Conditions	Min	Typ	Max	Unit
Input Voltage Range	V_{in}		1.2		20	V
Undervoltage Lockout Threshold	UVLO	V_{in} falls below UVLO threshold	2.85	3.0	3.15	V
Undervoltage Lockout Hysteresis	$UVLO_{hyst}$	MU/SN, SNAE SNAF, SNAI	50 30	70 50	90 70	mV
Overvoltage Lockout Threshold	OVLO	V_{in} rises above OVLO threshold MU/SN SNAE SNAF SNAI	5.43 6.0 6.75 7.0	5.675 6.25 7.07 7.2	5.9 6.5 7.4 7.4	V
Overvoltage Lockout Hysteresis	$OVLO_{hyst}$		50	100	125	mV
V_{in} versus V_{out} Dopout	V_{drop}	V_{in} = 5 V, I charge = 500 mA		105	200	mV
Supply Quiescent Current	Idd	No Load, V_{in} = 5.25 V		24	35	μA
OVLO Supply Current	Idd_{ovlo}	V_{in} = 7 V MU/SN, SNAE V_{in} = 8 V SNAF, SNAI		50 50	85 85	μA
Output Off State Current	I_{std}	V_{in} = 5.25 V, EN = 1.2 V		26	37	μA
FLAG Output Low Voltage	Vol_{flag}	V_{in} > OVLO, Sink 1 mA on $\overline{FLAG}$ pin			400	mV
FLAG Leakage Current	$FLAG_{leak}$	$\overline{FLAG}$ level = 5 V		5.0		nA
$\overline{EN}$ Voltage High	V_{ih}	V_{in} from 3.3 V to 5.25 V	1.2			V
$\overline{EN}$ Voltage Low	V_{il}	V_{in} from 3.3 V to 5.25 V			0.4	V
EN Leakage Current	EN_{leak}	EN = 5.5 V or GND		170		nA
TIMINGS						
Start Up Delay	t_{on}	From V_{in}: (0 to (OVLO − 300 mV) < V_{in} < OVLO) to V_{out} = 0.8xV_{in}, Rise time<4μs See Figures 3&9		4.0	15	ms
FLAG going up Delay	t_{start}	From V_{in} > UVLO to $\overline{FLAG}$ = 1.2 V, See Fig 3 & 10		3.0		μs
Output Turn Off Time	t_{off}	From V_{in} > OVLO to V_{out} ≤ 0.3 V, See Fig 4 & 11 V_{in} increasing from normal operation to >OVLO at 1V/μs. No output capacitor.		0.8	1.5	μs
Alert Delay	t_{stop}	From V_{in} > OVLO to $\overline{FLAG}$ ≤ 0.4 V, See Fig 4 & 12 V_{in} increasing from normal operation to >OVLO at 1V/μs		1.0	2.0	μs
Disable Time	t_{dis}	From $\overline{EN}$ 0.4 to 1.2V to V_{out} ≤ 0.3V, See Fig 5 & 13 V_{in} = 4.75 V. No output capacitor.		2.0		μs
Thermal Shutdown Temperature	T_{sd}			150		°C
Thermal Shutdown Hysteresis	T_{sdhyst}			30		°C

NOTE: Thermal Shutdown parameter has been fully characterized and guaranteed by design.

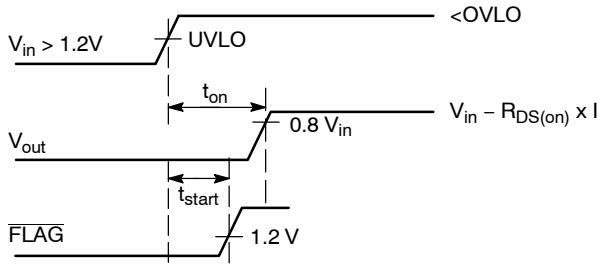


Figure 3. Start Up Sequence

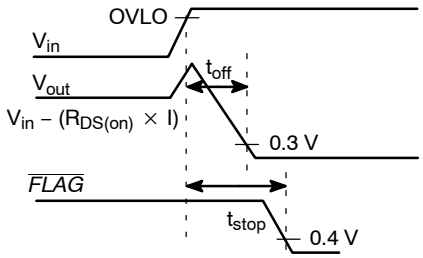


Figure 4. Shutdown on Over Voltage Detection

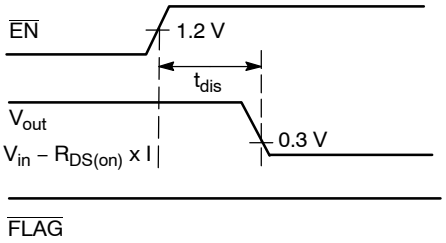


Figure 5. Disable on $\overline{EN}$ = 1

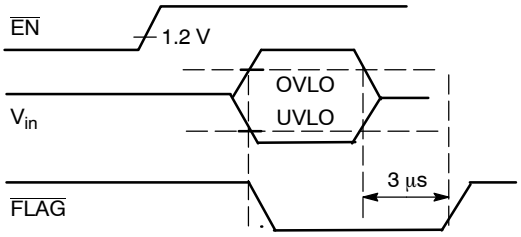


Figure 6. $\overline{FLAG}$ Response with $\overline{EN}$ = 1

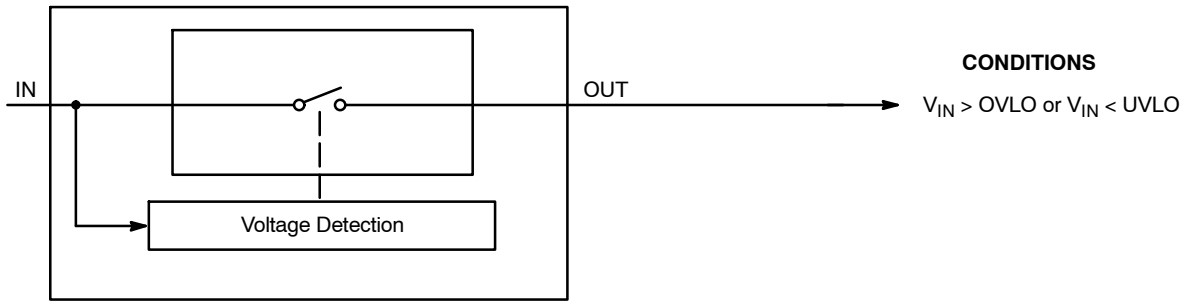


Figure 7.

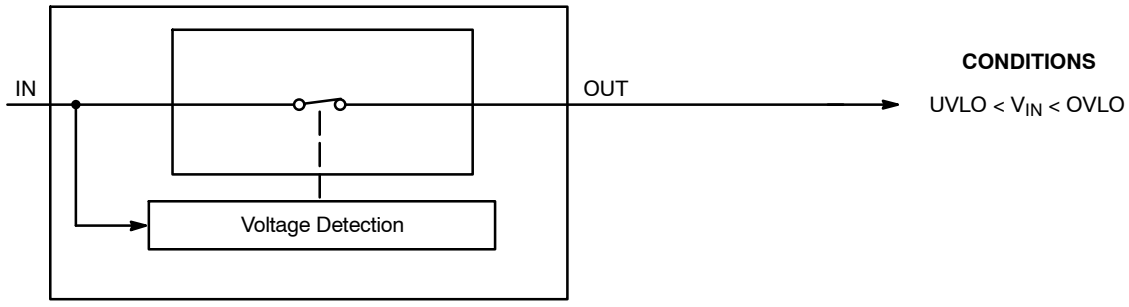


Figure 8.

TYPICAL OPERATING CHARACTERISTICS

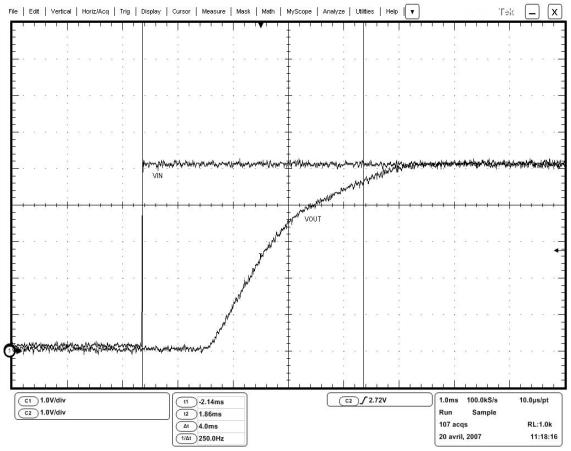


Figure 9. Startup
V_{in} = Ch1, V_{out} = Ch3

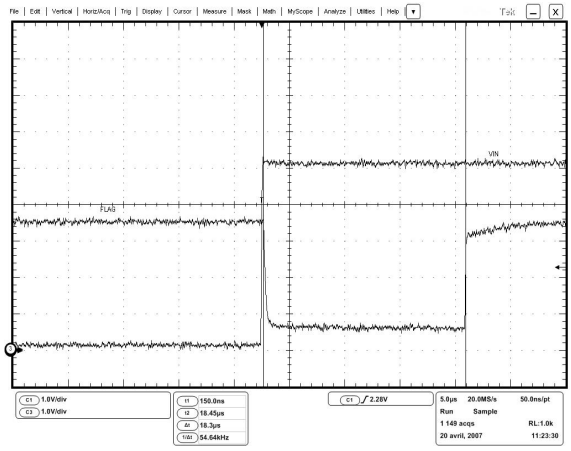


Figure 10. FLAG Going Up Delay
V_{in} = Ch1, FLAG = Ch3

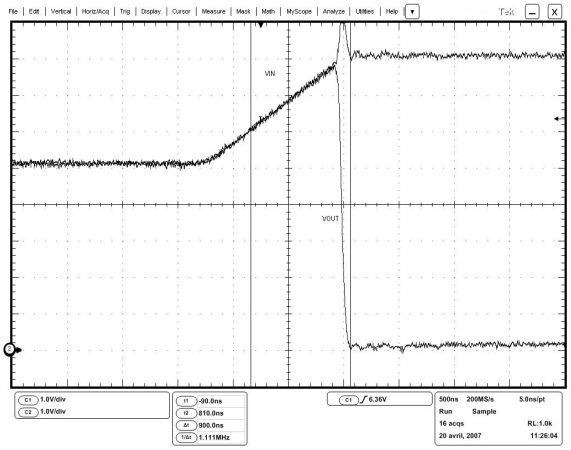


Figure 11. Output Turn Off Time
V_{in} = Ch1, V_{out} = Ch2

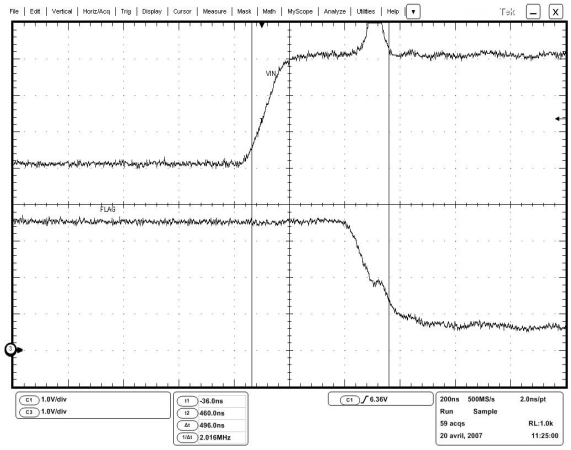


Figure 12. Alert Delay
V_{out} = Ch1, FLAG = Ch3

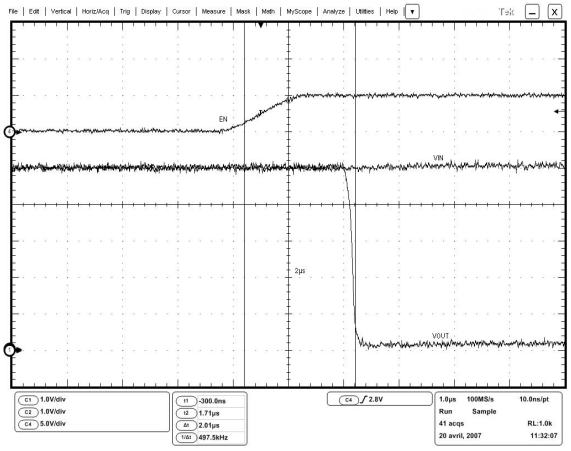


Figure 13. Disable Time
EN = Ch1, V_{out} = Ch2, FLAG = Ch3

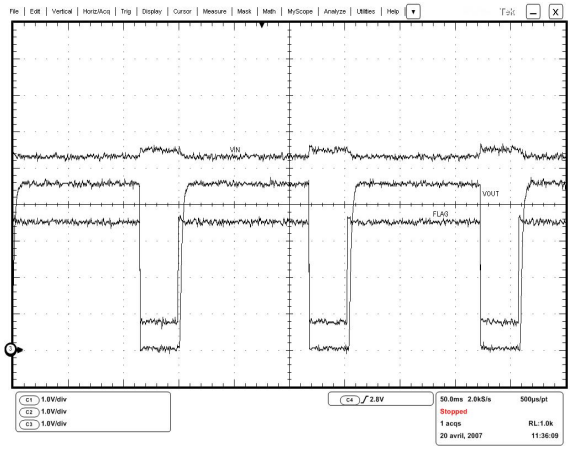


Figure 14. Thermal Shutdown
V_{in} = Ch1, V_{out} = Ch2, FLAG = Ch3

TYPICAL OPERATING CHARACTERISTICS

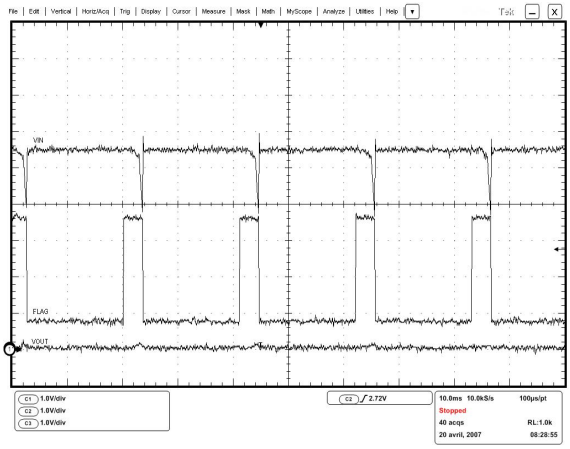


Figure 15. Direct Output Short Circuit

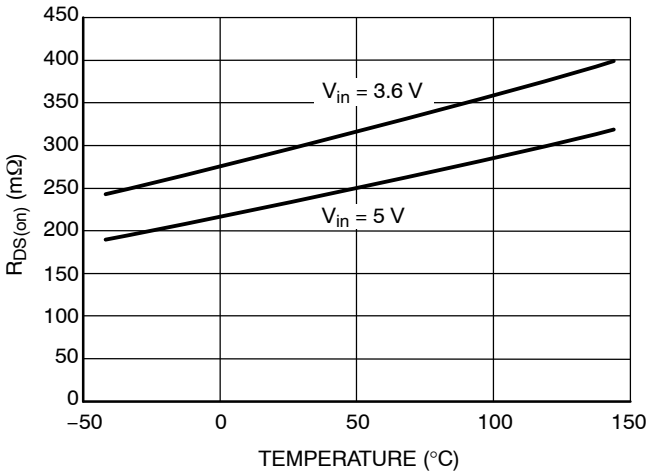


Figure 16. $R_{DS(on)}$ vs. Temperature (Load = 500 mA)

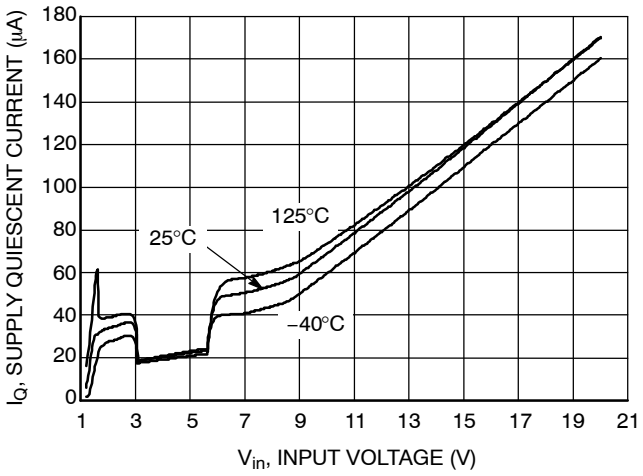


Figure 17. Supply Quiescent Current vs. V_{in}

In Operation

NCP360 provides overvoltage protection for positive voltage, up to 20 V. A PMOS FET protects the systems (i.e.: VBUS) connected on the V_{out} pin, against positive over−voltage. The Output follows the VBUS level until OVLO threshold is overtaken.

Undervoltage Lockout (UVLO)

To ensure proper operation under any conditions, the device has a built−in undervoltage lock out (UVLO) circuit. During V_{in} positive going slope, the output remains disconnected from input until V_{in} voltage is above 3.2 V nominal. The $\overline{FLAGV}$ output is pulled to low as long as V_{in} does not reach UVLO threshold. This circuit has a UVLO hysteresis to provide noise immunity to transient condition.

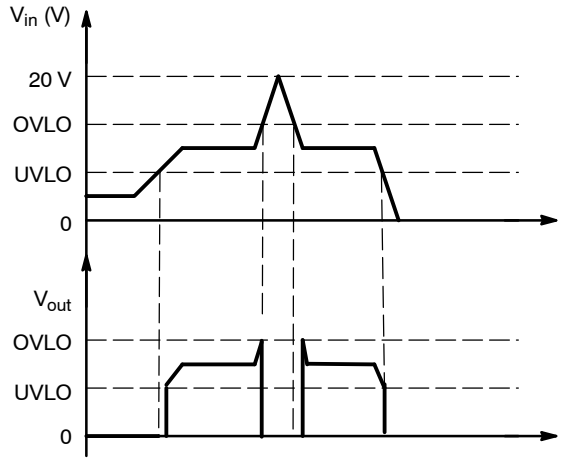


Figure 18. Output Characteristic vs. V_{in}

Overvoltage Lockout (OVLO)

To protect connected systems on V_{out} pin from overvoltage, the device has a built−in overvoltage lock out (OVLO) circuit. During overvoltage condition, the output remains disabled until the input voltage exceeds OVLO − Hysteresis.

$\overline{FLAG}$ output is tied to low until V_{in} is higher than OVLO. This circuit has a OVLO hysteresis to provide noise immunity to transient conditions.

$\overline{FLAG}$ Output

NCP360 provides a $\overline{FLAG}$ output, which alerts external systems that a fault has occurred.

This pin is tied to low as soon the OVLO threshold is exceeded When V_{in} level recovers normal condition, $\overline{FLAG}$ is held high. The pin is an open drain output, thus a pull up resistor (typically 1 MΩ− Minimum 10 kΩ) must be provided to $V_{battery}$. $\overline{FLAG}$ pin is an open drain output.

$\overline{EN}$ Input

To enable normal operation, the $\overline{EN}$ pin shall be forced to low or connected to ground. A high level on the pin disconnects OUT pin from IN pin. $\overline{EN}$ does not overdrive an OVLO or UVLO fault.

Internal PMOS FET

NCP360 includes an internal PMOS FET to protect the systems, connected on OUT pin, from positive overvoltage. Regarding electrical characteristics, the R_{DSon}, during normal operation, will create low losses on V_{out} pin, characterized by V_{in} versus V_{out} dropout. (See Figure 16).

ESD Tests

NCP360 fully support the IEC61000−4−2, level 4 (Input pin, 1 μF mounted on board).

That means, in Air condition, V_{in} has a ±15 kV ESD protected input. In Contact condition, V_{in} has ±8 kV ESD protected input.

Please refer to Fig 19 to see the IEC 61000−4−2 electrostatic discharge waveform.

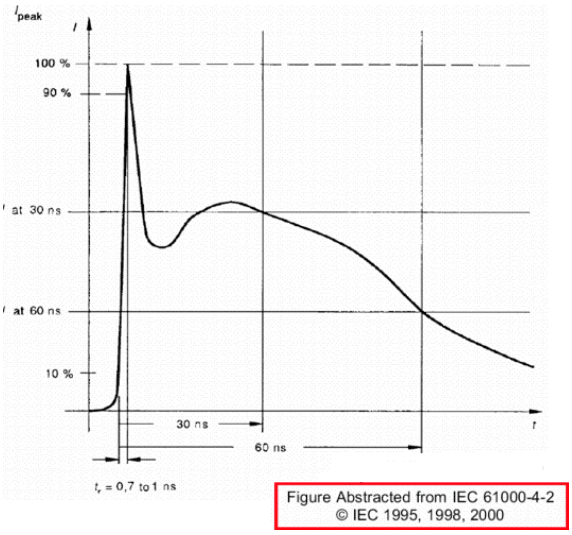


Figure 19.

PCB Recommendations

The NCP360 integrates a 500 mA rated PMOS FET, and the PCB rules must be respected to properly evacuate the heat out of the silicon. The UDFN PAD1 must be connected to ground plane to increase the heat transfer if necessary from an application standpoint. Of course, in any case, this pad shall be not connected to any other potential.

By increasing PCB area, the $R_{\theta JA}$ of the package can be decreased, allowing higher charge current to fill the battery.

Taking into account that internal bondings (wires between package and silicon) can handle up to 1 A (higher than thermal capability), the following calculation shows two different example of current capability, depending on PCB area:

- With 305°C/W (without PCB area), allowing DC current is 500 mA
- With 260°C/W (200 mm^2), the charge DC current allows with a 85°C ambient temperature is:
  $I = \sqrt{(T_J - T_A)/(R_{\theta JA} \times R_{DSON})}$
  I = 625 mA

In every case, we recommend to make thermal measurement on final application board to make sure of the final Thermal Resistance.

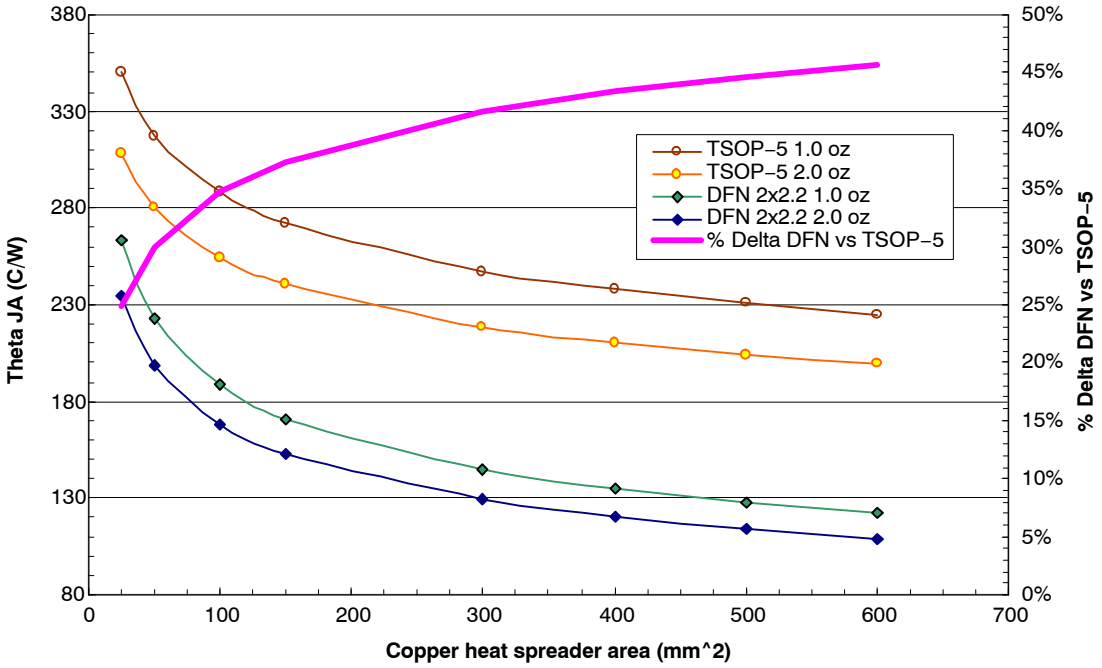


Figure 20. Thermal Resistance of UDFN 2x2 and TSOP Packages as a Function of PCB Area and Thickness

ORDERING INFORMATION

Device	Marking	Package	Shipping†
NCP360MUTBG	ZD	UDFN6 (Pb−Free)	3000 / Tape & Reel
NCP360MUTXG	ZD	UDFN6 (Pb−Free)	10000 / Tape & Reel
NCP360SNT1G	SYA	TSOP−5 (Pb−Free)	3000 / Tape & Reel
NCP360SNAET1G	AAP	TSOP−5 (Pb−Free)	3000 / Tape & Reel
NCP360SNAFT1G	AA5	TSOP−5 (Pb−Free)	3000 / Tape & Reel
NCP360SNAIT1G	ACE	TSOP−5 (Pb−Free)	3000 / Tape & Reel
NCV360SNT1G*	VUE	TSOP−5 (Pb−Free)	3000 / Tape & Reel
NCV360SNAET1G*	VEY	TSOP−5 (Pb−Free)	3000 / Tape & Reel
NCV360SNAFT1G*	VUM	TSOP−5 (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
*NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements

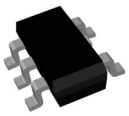
SELECTION GUIDE

The NCP360 can be available in several undervoltage and overvoltage thresholds versions. Part number is designated as follows:

NCP360xxxxTxG

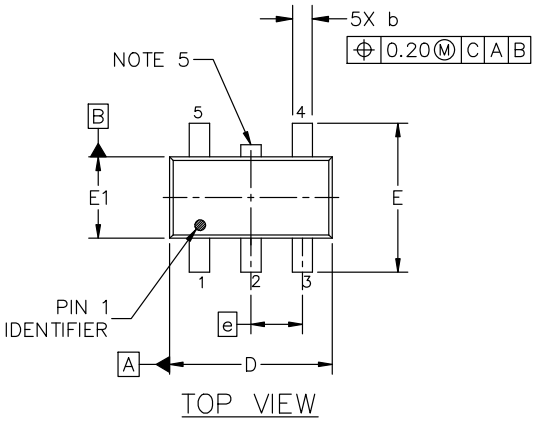
a b c d

Code	Contents
a	Package MU = UDFN SN = TSOP5
b	UVLO Typical Threshold b: − = 3.0 V b: A = 3.0 V
c	OVLO Typical Threshold c: − = 5.675 V c: E = 6.25 V c: F = 7.07 V c: I = 7.2 V
d	Tape & Reel Type (parts per reel) d: 1 = 3000 d: B = 3000 d: X = 10000

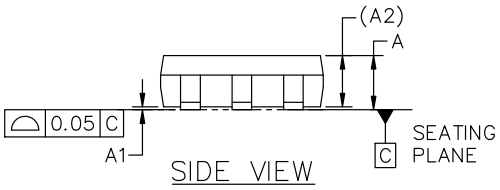


TSOP−5 3.00x1.50x0.95, 0.95P
CASE 483
ISSUE P

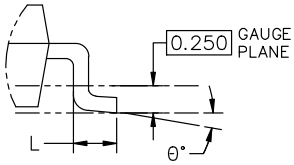
DATE 01 APR 2024



TOP VIEW



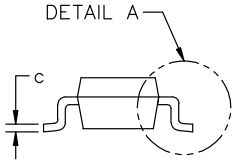
SIDE VIEW



DETAIL "A"
SCALE 2:1

NOTES:

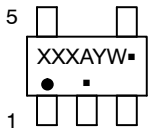
1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5−2018.
2. ALL DIMENSION ARE IN MILLIMETERS (ANGLES IN DEGREES).
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OF GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSION D.
5. OPTIONAL CONSTRUCTION: AN ADDITIONAL TRIMMED LEAD IS ALLOWED IN THIS LOCATION. TRIMMED LEAD NOT TO EXTEND MORE THAN 0.2 FROM BODY.



END VIEW

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.900	1.000	1.100
A1	0.010	0.055	0.100
A2		0.950 REF.	
b	0.250	0.375	0.500
c	0.100	0.180	0.260
D	2.850	3.000	3.150
E	2.500	2.750	3.000
E1	1.350	1.500	1.650
e		0.950 BSC	
L	0.200	0.400	0.600
θ	0°	5°	10°

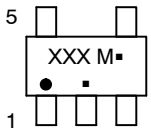
GENERIC
MARKING DIAGRAM*



Analog

XXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
▪ = Pb−Free Package

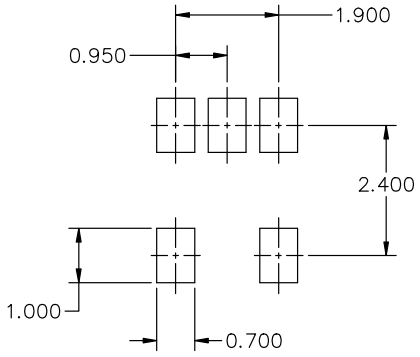
(Note: Microdot may be in either location)



Discrete/Logic

XXX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.



RECOMMENDED MOUNTING FOOTPRINT*

* FOR ADDITIONAL INFORMATION ON OUR Pb−FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

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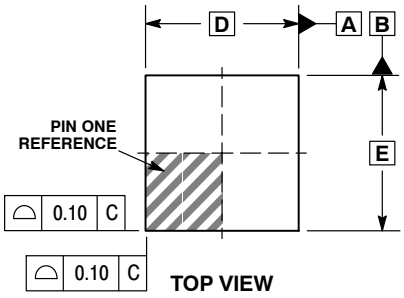
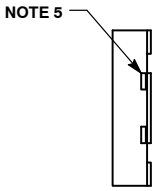
SCALE 4:1

UDFN6 2x2, 0.65P
CASE 517AB
ISSUE C

DATE 10 APR 2013



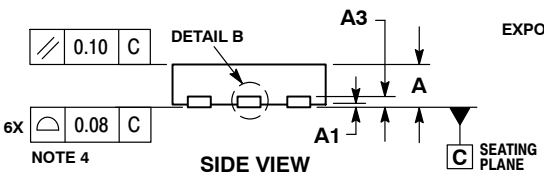
TOP VIEW



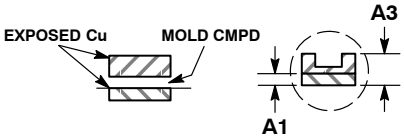
END VIEW

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.25MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. TIE BARS MAY BE VISIBLE IN THIS VIEW AND ARE CONNECTED TO THE THERMAL PAD.

DIM	MILLIMETERS MIN	MAX
A	0.45	0.55
A1	0.00	0.05
A3	0.127 REF	
b	0.25	0.35
D	2.00 BSC	
D2	1.50	1.70
E	2.00 BSC	
E2	0.80	1.00
e	0.65 BSC	
L	0.25	0.35
L1	---	0.15



SIDE VIEW



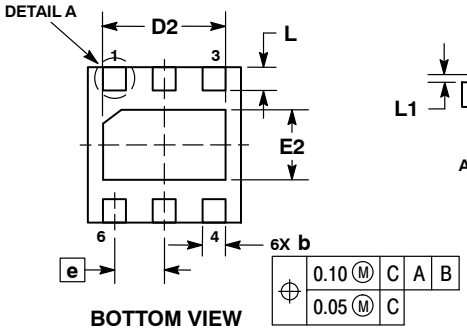
DETAIL B
ALTERNATE CONSTRUCTIONS

GENERIC MARKING DIAGRAM*

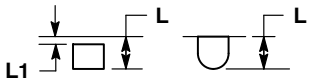
XX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

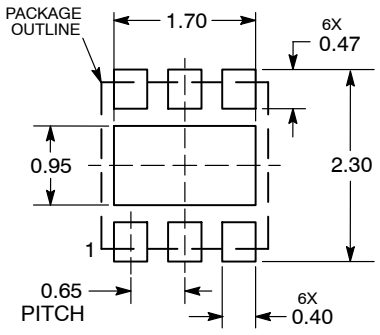


BOTTOM VIEW



DETAIL A
ALTERNATE TERMINAL CONSTRUCTIONS

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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DESCRIPTION:	**UDFN6 2X2, 0.65P**		**PAGE 1 OF 1**

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