TAS3103AEVM

Evaluation Module for the TAS3103A Digital Audio Signal Processor

User's Guide

Literature Number: SLEU087
February 2007

Texas Instruments

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About This Manual

This manual describes the operation of the TAS3103AEVM evaluation module from Texas Instruments.

How to Use This Manual

This document contains the following chapters:

- Chapter 1: Overview
- Chapter 2: Quick Setup Guide
- Chapter 3: System Interfaces
- Chapter 4: Schematics

Information About Cautions and Warnings

This book may contain cautions and warnings.

CAUTION

This is an example of a caution statement.

A caution statement describes a situation that could potentially damage your software or equipment.

WARNING

This is an example of a warning statement.

A warning statement describes a situation that could potentially cause harm to you.

The information in a caution or a warning is provided for your protection. Please read each caution and warning carefully.

Related Documentation From Texas Instruments

The following data manuals have detailed descriptions of the integrated circuits used in the design of the TAS3103AEVM.

PART NUMBER	LITERATURE NUMBER
TAS3103A	SLES166
PCM1802	SLES023
PCM1754	SLES092

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Overview

The TAS3103A is a 48-bit single-chip 3-channel digital audio playback processor with integrated audio processing for speaker equalization, dual-band dynamics processing (compressor/expander/limiter/noise gate), delay compensation, and spatial enhancement. These algorithms can be used to compensate for real-world limitations of speakers, amplifiers, and listening environments, resulting in a dramatic improvement of the reproduced audio quality. The TAS3103A EVM is an evaluation board for the TAS3103A digital audio processor.

The TAS3103A EVM permits evaluation and demonstration of the TAS3103A 3-channel 48-bit digital audio processor.

TAS3103A applications include digital televisions, home theater systems, mini-component audio systems, and professional audio.

A TI PurePath™ digital amplifier EVM can be connected to the TAS3103A EVM digital output, enabling the TAS3103A to drive a loudspeaker. Examples of EVMs that can be connected include, but are not limited to, TAS5508-5142K7EVM, TAS5518-5152K8EVM, TAS5518-5182C8EVM, and TAS5086-5186V6EVM. This system is designed for home theater applications such as A/V receivers, DVD mini component systems, home theater in a box (HTIB), DVD receivers, or plasma display panels (PDP).

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1.1 TAS3103A EVM Features

The TAS3103A EVM contains a TAS3103A processor, a signal input interface, an output signal interface, and a power supply.

The EVM accepts input signals in three formats:

- Two-channel optical S/PDIF format
- Four-channel RCA analog inputs into two PCM1802 ADCs, 102-dB DYR-A weighted
- Four digital serial inputs (eight channels) that support left-justified, right-justified, I^2S, or DSP modes

The TAS3103A EMC provides outputs in three formats:

- Optical S/PDIF format
- Four-channel RCA analog outputs from two PCM1754 DACs, 106-dB DYR-A weighted
- Three digital serial outputs (six channels) that support left-justified, right-justified, I^2S, or DSP modes

The internal signal processing program and parameters of the TAS3103A can be controlled by a computer parallel-port driven I^2C interface, a PC-USB to I^2C interface, or a command-and-control GUI.

Power requirements are 6.5 V to 8 V ± 5% dc. On-board regulators provide separate supplies for the digital and analog sections.

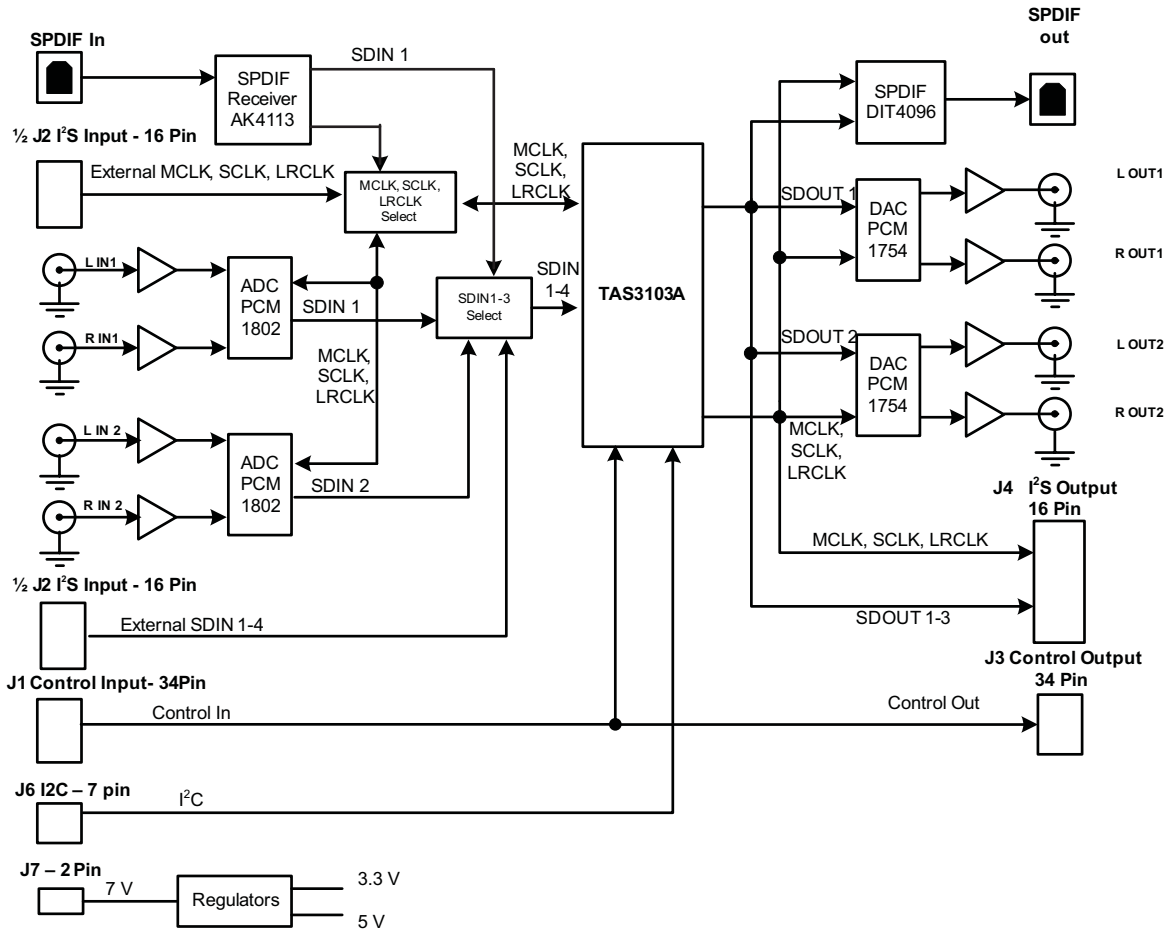

Figure 1-1. TAS3103A EVM Block Diagram

1.2 PCB Configuration

The following components are on the EVM board:

- The TAS3103A device is located at U1 (also labled DAP).
- The EEPROM adjacent to U1 is used for program and coefficient storage.
- LED2 and LED3 are green LEDs that indicate that the power supply voltage is within specification and that the device is out of RESET.
- Blue LED 1 indicates that the board is receiving a valid S/PDIF signal and the S/PDIF lock has been achieved by the AK4113.
- Switch SW1 is a momentary switch that can be used to apply reset to the TSA3103A.
- LED4 is an orange LED that indicates the TAS3103A is receiving an active-low reset.

The following input ports are available on the EVM:

- S/PDIF Input

  TOSLINK input optical connector supporting sampling rates up to 96 kHz.
- Four analog line-in channels

  Two TI Burr-Brown PCM1802 ADCs (24 bit, 96 kHz, stereo) provide the four channels. Each ADC is provided with separate left-channel and right-channel RCA input jacks.
- Digital input header (J2, which contains JP2, JP3, JP4, and JP5)

  Provides the means of inputting four serial data sources (SDIN1, SDIN2, SDIN3, SDIN4) and three clocks (MCLK, SCLK, and LRCLK). J2 is a 16-pin box header that is compatible with most of the PurePath digital amplifier boards.
- USB port for connection to the PC (J1)

  This TUSB3210 provides a translation between the PC-USB interface and the I^2C interface of the TAS3103A.
- Coaxial jack power connector

The following output ports are available on the EVM:

- S/PDIF out

  TOSLINK optical connector providing sample rates as high as 96 kHz. This outputs the TAS3103A SDOUT1 signal. This output is active at all times.
- Four analog line-out channels

  Two TI Burr-Brown PCM1754 DACs (24 bit, 96 kHz, stereo) provide the four channels. Each DAC output is available through separate left-channel and right-channel RCA jacks. These receive inputs from the TAS3103A SDOUT1 and SDOUT2. This output is active at all times.
- Digital output header (J5, which contains MCLKO, SCLO2, LRCLKO, SDOUT1, SDOUT2, SDOUT3)

  This header provides the output of three serial data sources (SDOUT1, SDOUT2, and SDOUT3) and three clocks (MCLK, SCLK, and LRCLK). J5 is a 16-pin box header that is compatible with most PurePath digital amplifier boards. This output is active at all times.
- GPIO header (on underside of board)

  Provides access to the four (4) GPIO ports provided by the TAS3103A. The output header is a 2×4-pin open header.

The board requires only one 7-V to 8-V ± 5% 650-mA power source. The power is supplied though coaxial connector. The center is positive voltage. From this input power source, the EVM provides power to I^2C paddle board via the provided I^2C cable. The paddle board is used as an interface between a PC parallel port and the I^2C port on the EVM. The paddle board is provided with the EVM.

All clocks can be supplied by the board, or the user can choose to input clocks via the I^2S input header.

Internally, all devices are configured to the I^2S data format. When using the S/PDIF receiver or the ADCs to input data, the I^2S output header outputs I^2S formatted data.

When using the I^2S input header to source data to the EVM and using either the S/PDIF transmitter or the DAC to output data, the data on the I^2S output header is I^2S formatted data. However, when using the I^2S input header to source data to the EVM and the I^2S output header to output the data, any of the data formats supported by the TAS3103A can be used.

To support the I^2S input and output 24-bit format, set register F9 to 0x01 0x00 0x01 0x22.

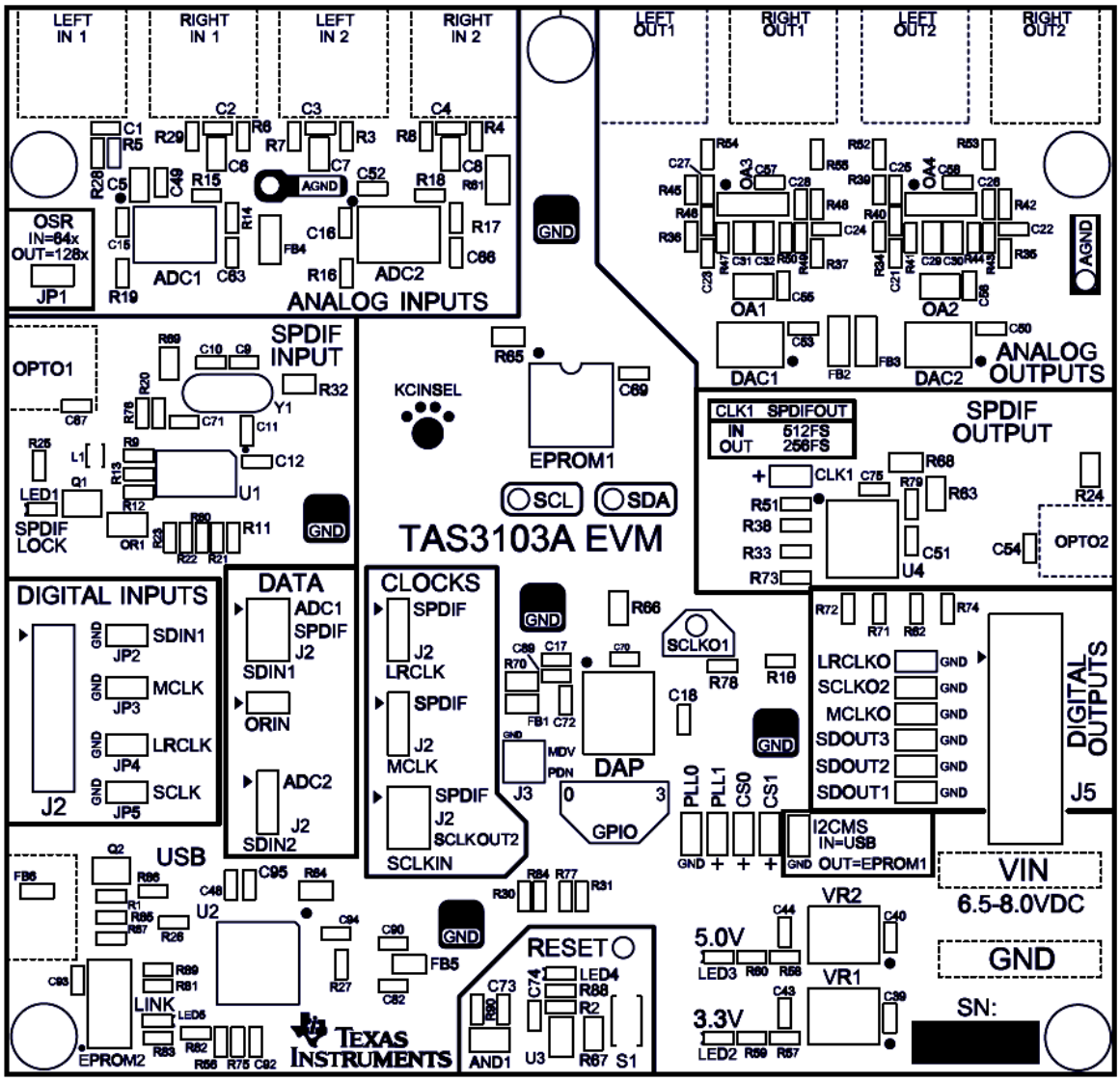

Figure 1-2. TAS3103A EVM Components

Quick Setup Guide

The TAS3103A EVM has several configuration options that permit the user to configure the TAS3103A to meet a variety of system configuration requirements.

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2.1 Electrostatic Discharge Warning

Many of the components on the TAS3103A EVM are susceptible to damage by electrostatic discharge (ESD). Customers are advised to observe proper ESD handling precautions when unpacking and handling the EVM, including the use of a grounded wrist strap at an approved ESD workstation.

CAUTION

Failure to observe ESD handling procedures may result in damage to EVM components.

2.2 Default EVM Configuration

As shipped, the TAS3103A EVM is configured as follows:

- I^2C slave mode (does not obtain configuration from EEPROM)
- I^2S clock slave mode
- MCLK, SCLK, and LRCLK provided by the S/PDIF receiver
- Input data is from S/PDIF receiver on SDIN1
- SPDIFOUT CLK is 256 Fs
- ADC oversampling rate is 128 Fs
- PLL clock is 11 $\times$ MCLK/2
- Device I^2C address is 0x68
- ORIN is low

The TAS3103A analog, S/PDIF, and digital outputs are always enabled.

The default jumper settings are shown in Figure 2-1 (jumpers are shown in red).

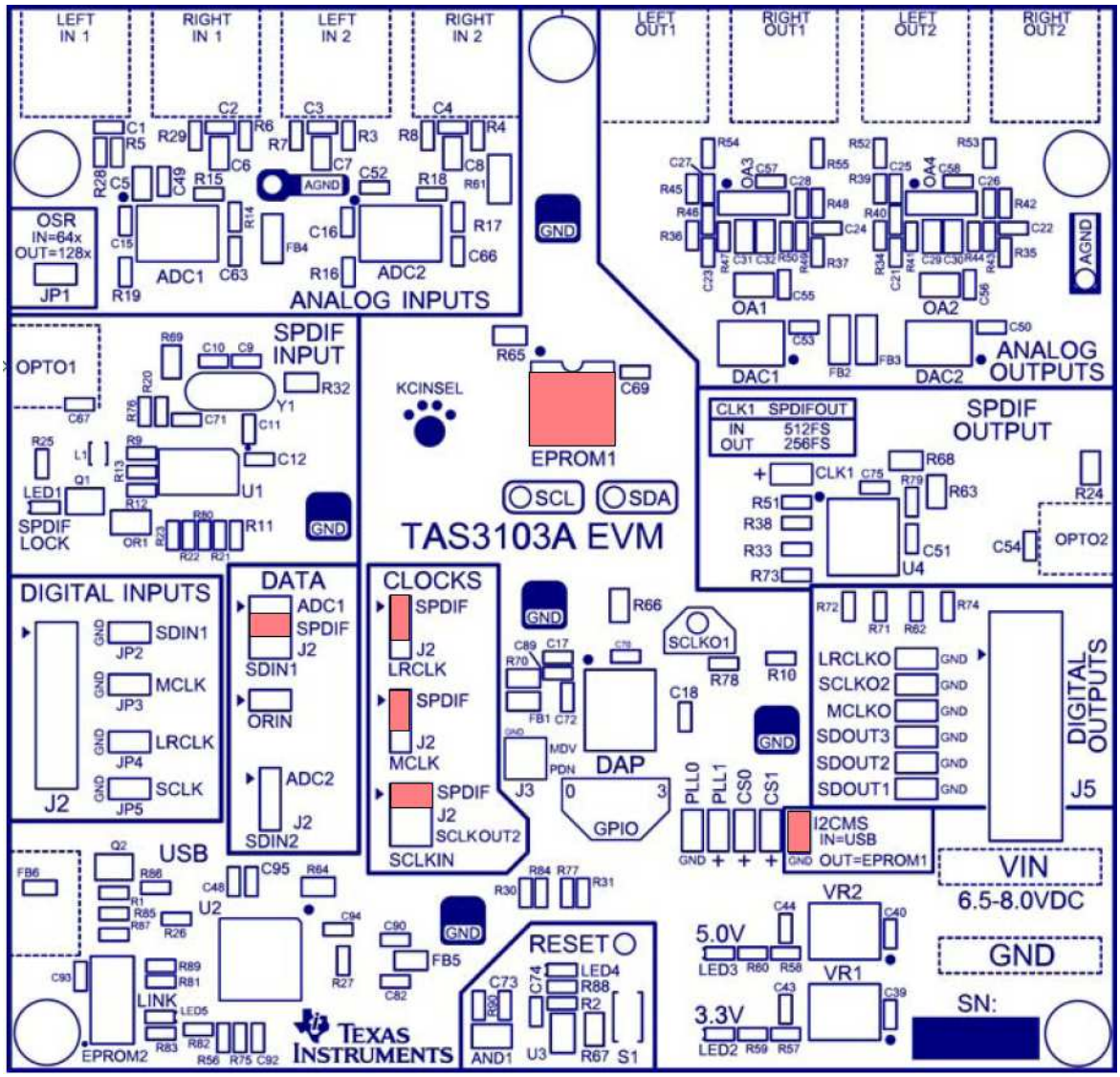

Figure 2-1. Default Configuration

2.3 Load Configuration from EEPROM

The TAS3103A EVM can be configured to boot up in I^2C master mode and input the configuration settings from the EEPROM, using the configuration shown in Figure 2-2.

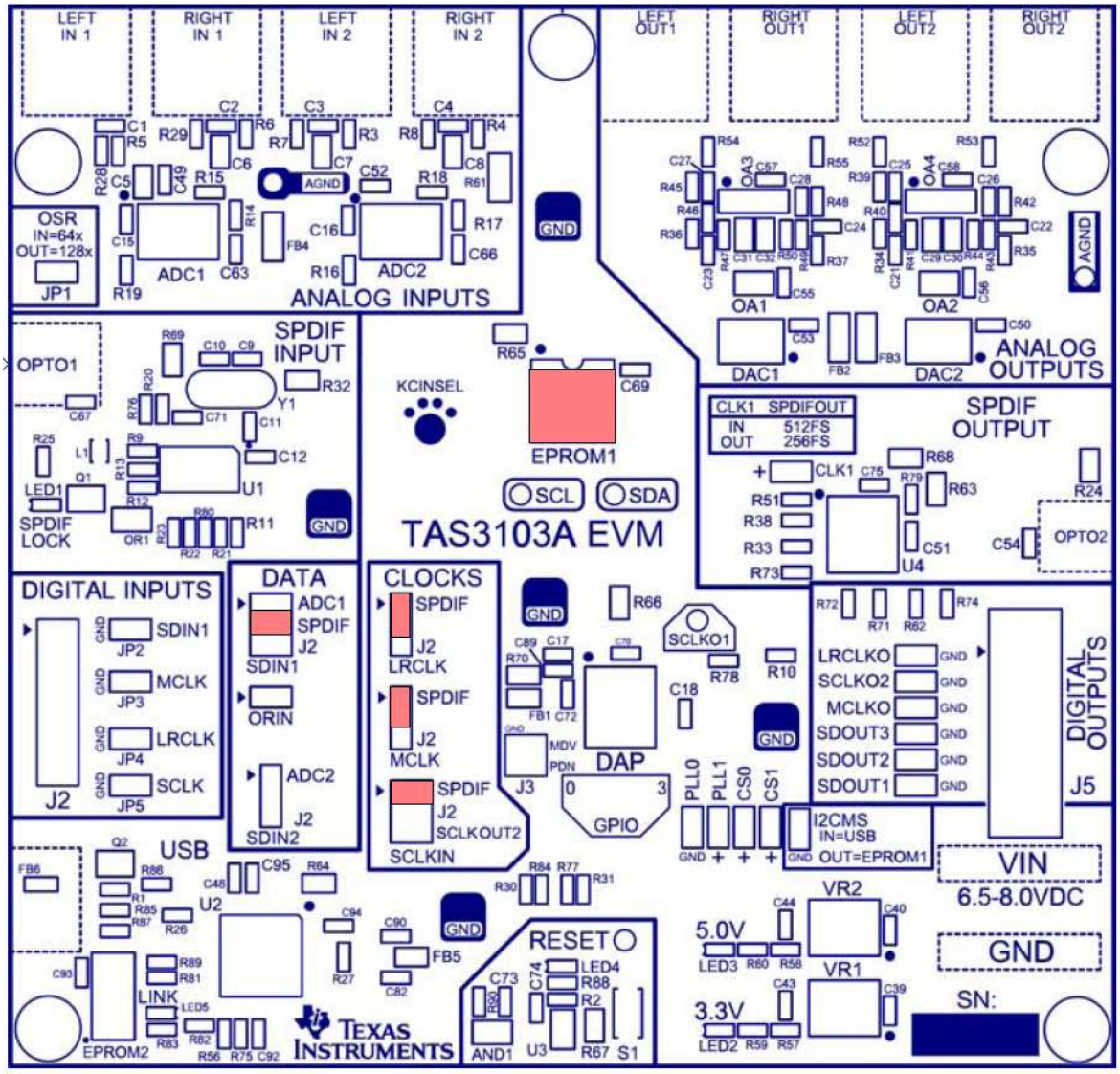

Figure 2-2. Load Configuration Data From EEPROM

2.4 Analog Input Configuration

The TAS3103A EVM can be configured to use the analog inputs and a clock provided by the S/PDIF receiver, using the configuration shown in Figure 2-3.

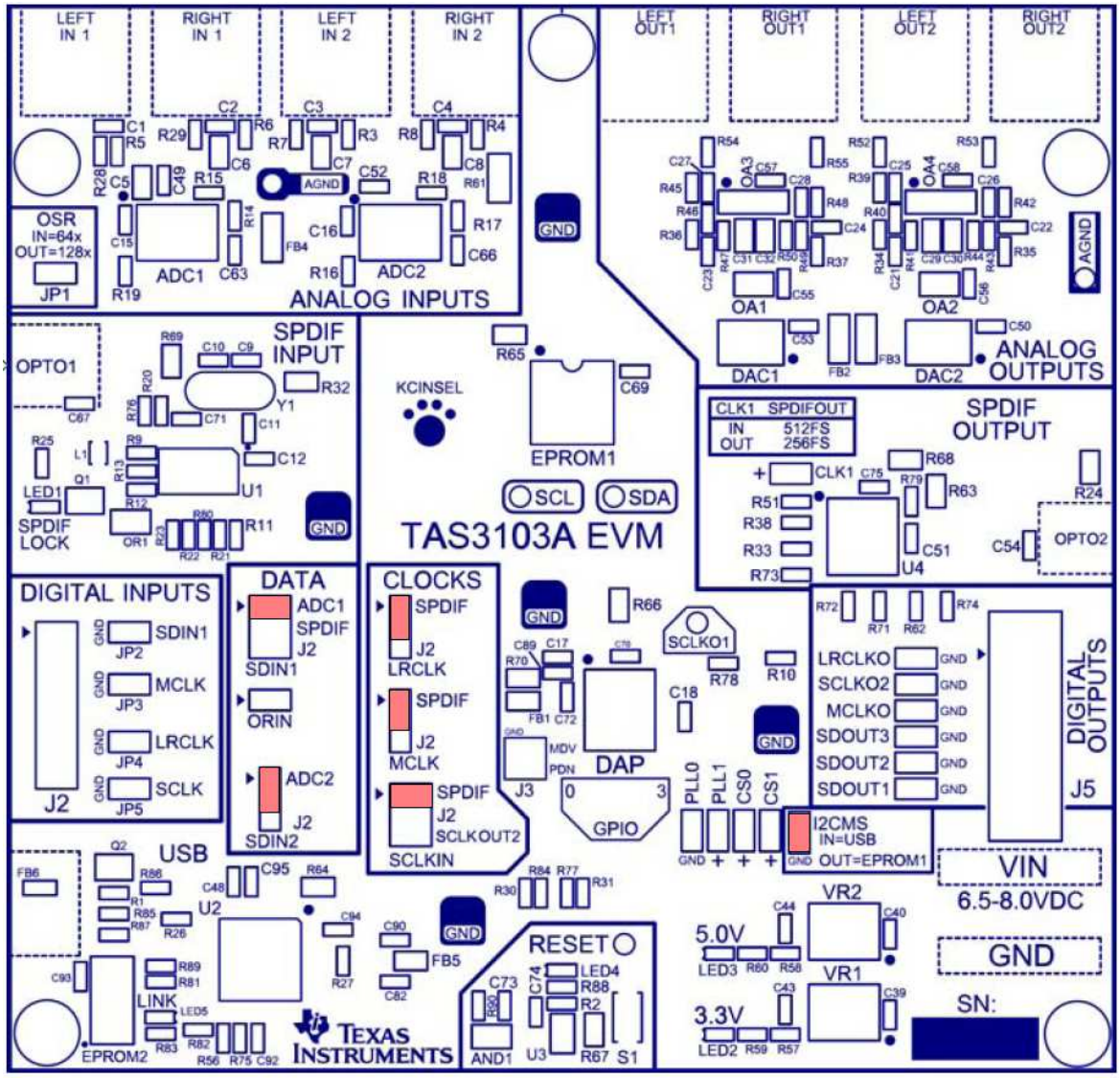

Figure 2-3. Enable Analog Input Configuration

2.5 Initializing the TAS3103A

Upon receiving a reset, the TAS3103A EVM starts operating in clock slave mode. The S/PDIF receiver, on the input board, is the MCLK clock master in this system.

To start up the TAS3103A EVM, use following procedure:

1. Insert the PurePath CD-ROM and, if it does not auto load, run the ReadMe file.
   a. Select Software in the menu on the left.
   b. Select the Digital Audio Processor Configuration Tool (DCT) 4.0 (USB).
   c. Follow the instructions to install the DCT.
2. Turn on all power supplies before connecting the USB interface.
3. Connect the USB interface and press the RESET button.
4. Ensure that blue LED on the EVM is on.
5. Start the DAS DCT software.
6. Load the TAS3103Example.dat file.
7. Ensure that the bottom status indication shows Ready. If not, recheck the power and USB connection.
8. Select Demo GUI or Debug GUI.
9. The EVM is ready to use.

Note: If using the TAS3103A EVM without using the DAS DCT software, the EVM can be set to stream audio from input to output by setting the serial interface format and volume.

To enable the TAS3103A to communicate to the S/PDIF receiver, S/PDIF transmitter, ADC, and DACs, the TAS3103A data interfaces must be set to 24-bit I^2S mode. This is done for the clock slave mode by setting register F9 to 0x01 0x01 0x24 0x33.

After a reset, the default configuration of the TAS3103A sets volume 1, 2, and 3 to mute. The TAS3103A streams audio from SDIN1 to SDOUT1 when the volume at I^2C addresses 0xF2 and 0xF3 are set to a desired gain value. A value of 1 is specified by 0x00 0x80 0x00 0x00.

System Interfaces

This chapter describes the power supplies and system interfaces of the TAS3103A EVM board.

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3.1 Digital Audio Interface: Input (J2), Output (J5)

The digital audio interface contains digital audio signal data (I^2S) and clocks. See the TAS3103A data manual (TI literature number SLES166) for signal timing and details not explained in this document.

Table 3-1. J2 and J5 Pin Descriptions

PIN		DESCRIPTION
NO.	NAME	
1	GND	Ground
2	MCLK	Master clock input
3	GND	Ground
4	SDIN1	I^2S data 1, channels 1 and 2
5	SDIN2	I^2S data 2, channels 3 and 4
6	SDIN3	I^2S data 3, channels 5 and 6
7	SDIN4	I^2S data 4, channels 7 and 8
8	–	Reserved
9	–	Reserved
10	GND	Ground
11	SCLK	I^2S bit clock
12	GND	Ground
13	LRCLK	I^2S left-right clock
14	GND	Ground
15	–	Reserved
16	GND	Ground

3.2 Jumper Settings

3.2.1 Over Sample Rate (JP1)

When jumper JP1 is inserted, the ADC oversample rate is 64 Fs. When jumper JP1 is removed, the ADC oversample rate is 128 Fs.

3.2.2 Clock Jumpers

The sources for MCLK, SCLK, and LRCLK to the TAS3103A are jumper selectable.

3.2.2.1 MCLK

When MCLK pins 1-2 are connected, the MCLK source is the S/PDIF receiver.

When MCLK pins 2-3 are connected, the MCLK source is an external MCLK.

3.2.2.2 SCLKIN

When SCLKIN pins 1-2 are connected, the SCLKIN source is the S/PDIF receiver.

When SCLKIN pins 3-4 are connected, the SCLKIN source is the external SCLK.

When SCLKIN pins 5-6 are connected, the SCLKIN source is SCLKOUT2 (for master clock mode).

3.2.2.3 LRCLK

When LRCLK pins 1-2 are connected, the LRCLK source is the S/PDIF receiver.

When LRCLK pins 3-4 are connected, the LRCLK source is an external LRCLK.

3.2.3 Clk1 Jumper – Master Clock Selection

The master clock rate is selected by jumper CLK1 (see Table 3-2).

Table 3-2. Master Clock Rate

MODE	I2CMS
Master clock rate = 256 Fs (default)	Out
Master clock rate = 512 Fs	In

3.2.4 Data Jumpers

The sources for SDIN1, SDIN2, SDIN4, and ORIN to the TAS3103A are jumper selectable.

3.2.4.1 SDIN1

When SDIN1 pins 1-2 are connected, the SDIN1 source is ADC1.

When SDIN1 pins 3-4 are connected, the SDIN1 source is the S/PDIF receiver.

When SDIN1 pins 5-6 are connected, the SDIN1 source is an external SDIN1.

3.2.4.2 SDIN2

When SDIN2 pins 1-2 are connected, the SDIN1 source is ADC2.

When SDIN2 pins 3-4 are connected, the SDIN2 source is an external SDIN2.

3.2.4.3 ORIN

When ORIN pins 1-2 are connected, the SDIN1 source is ADC2.

3.2.5 Clock Control

The PLL divide ratios are set by PLL0 and PLL1 (see Table 3-3).

Table 3-3. Clock Control

MODE	PLL1	PLL0
11 × MCLK	Out	In
11 × MCLK/2	Out	Out
11 × MCLK/4	In	In
MCLK	In	Out

3.2.6 Device Address

The device address is set by CS0 and CS1 (see Table 3-4).

Table 3-4. Device Address

MODE	CS1	CS0
0x68	Out	Out
0x6A	Out	In
0x6C	In	Out
0x6E	In	In

3.2.7 I^2C Master/Slave

The I^2C mode is set by I2CMS (see Table 3-5).

Table 3-5. I^2C Master/Slave

MODE	I2CMS
Master mode (EEPROM load)	Out
Slave mode (slave load)	In

Schematics

This chapter contains the TAS3103A EVM schematics.

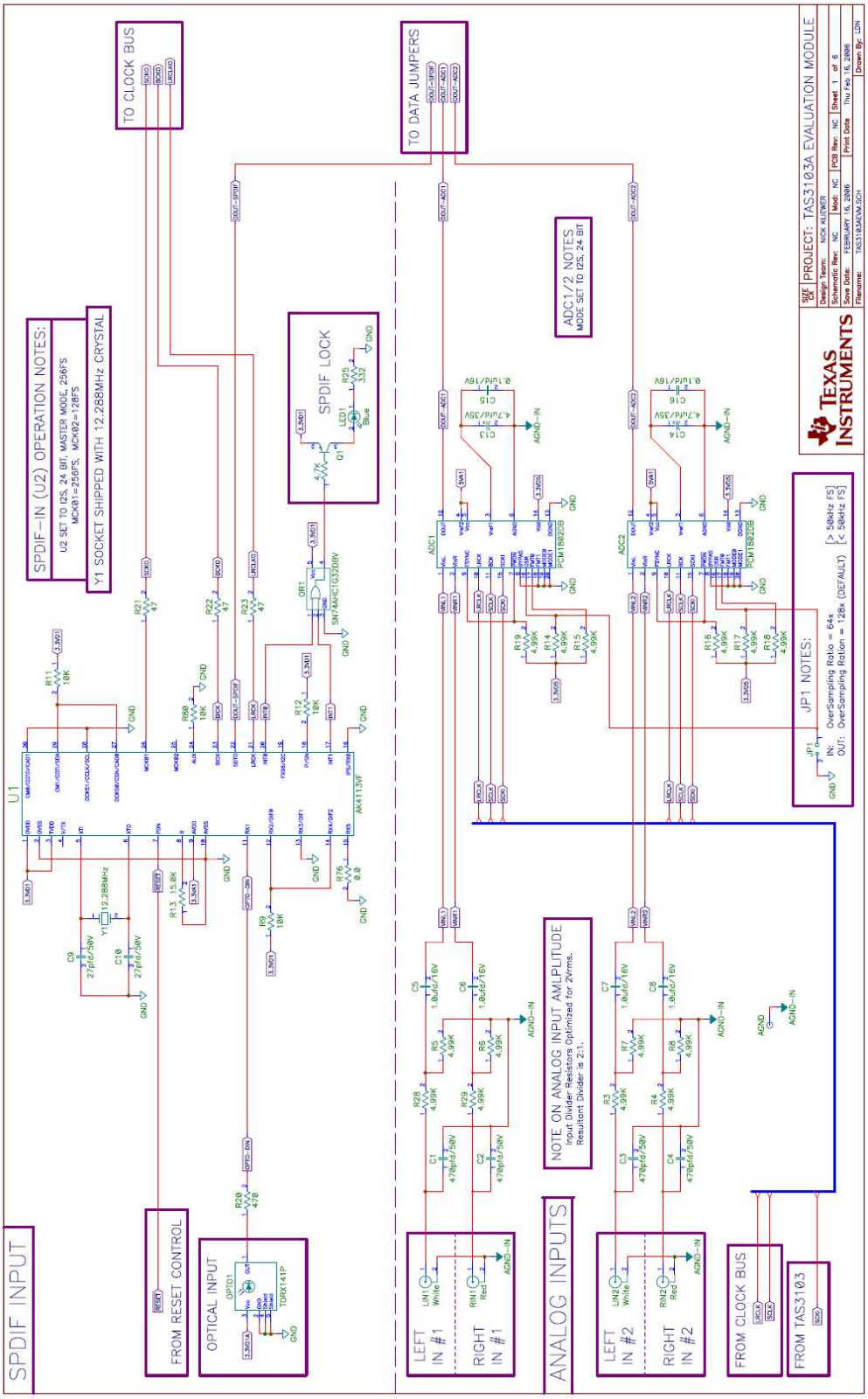

Figure 4-1. TAS3103A EVM Schematic – S/PDIF Input

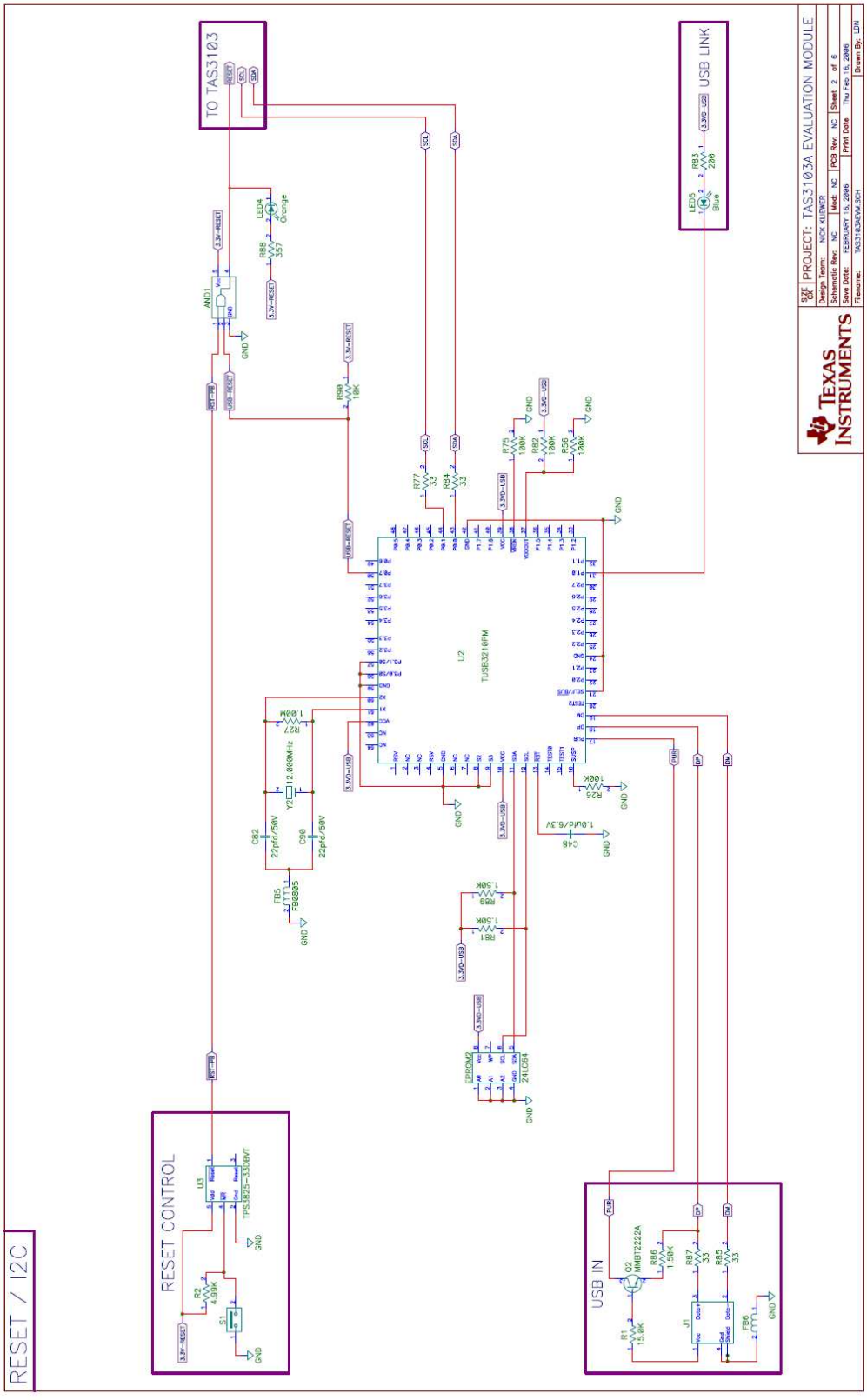

Figure 4-2. TAS3103A EVM Schematic – Reset/I²C

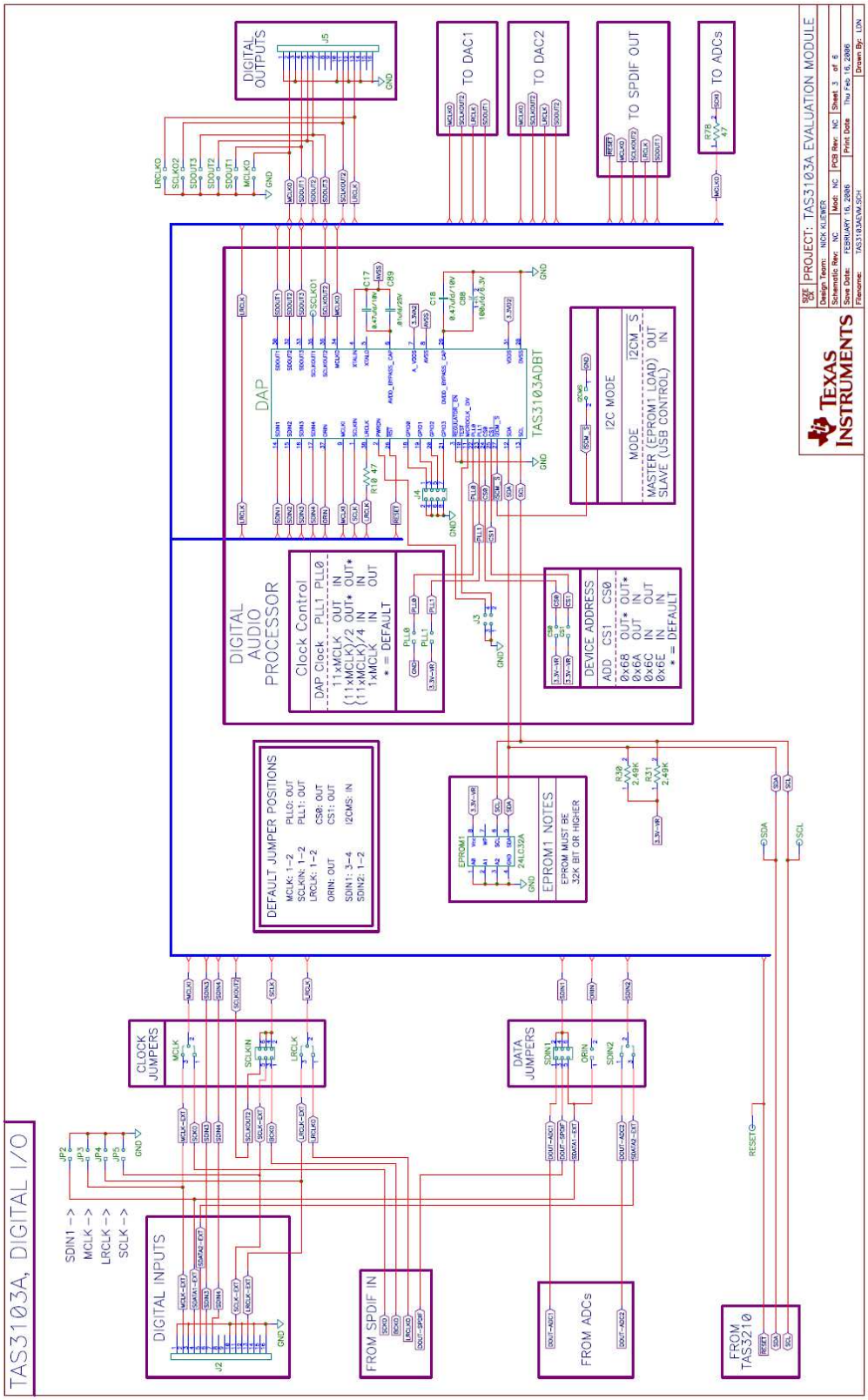

Figure 4-3. TAS3103A EVM Schematic – TAS3103A, Digital I/O

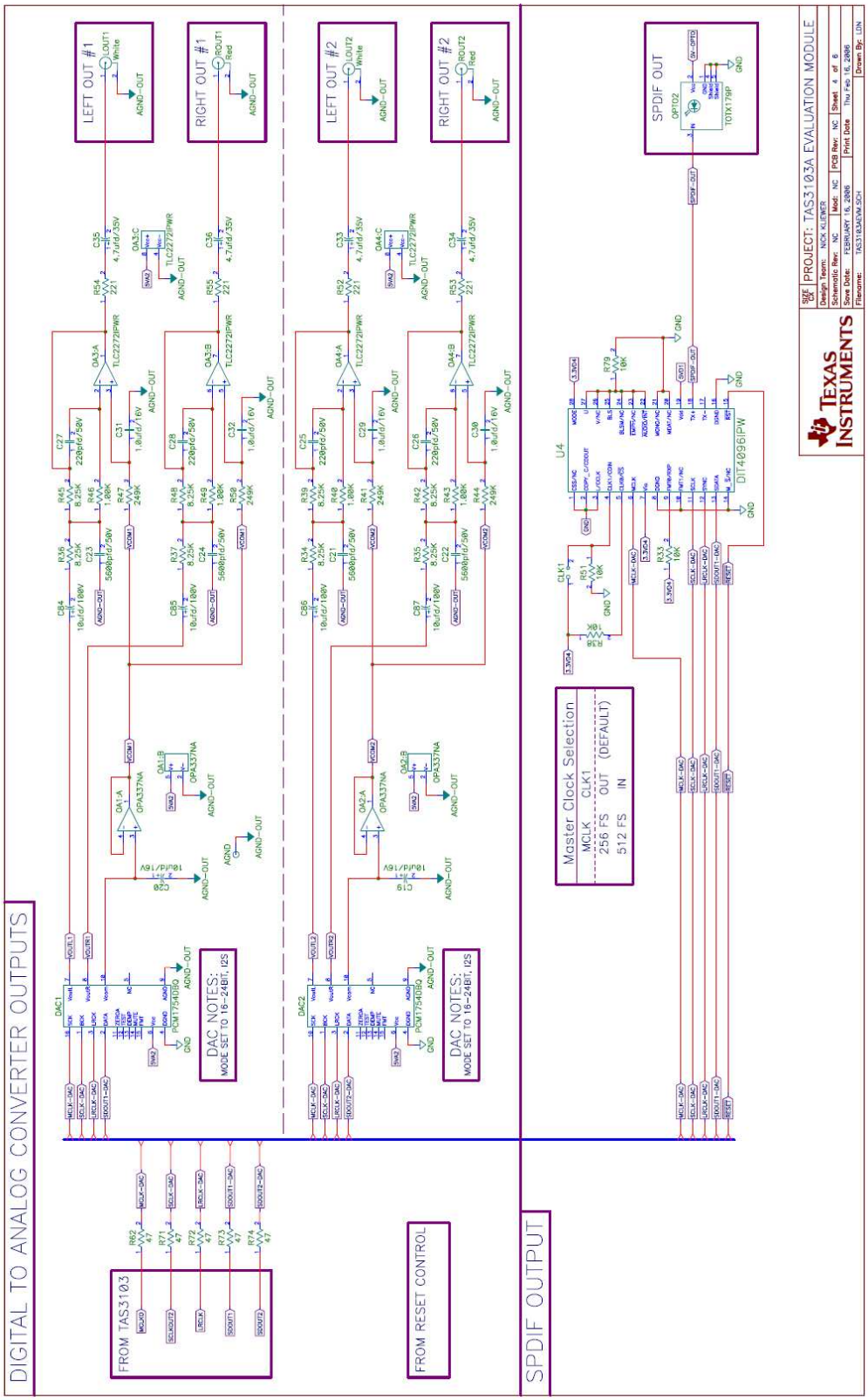

Figure 4-4. TAS3103A EVM Schematic – Digital-to-Analog Converter Outputs

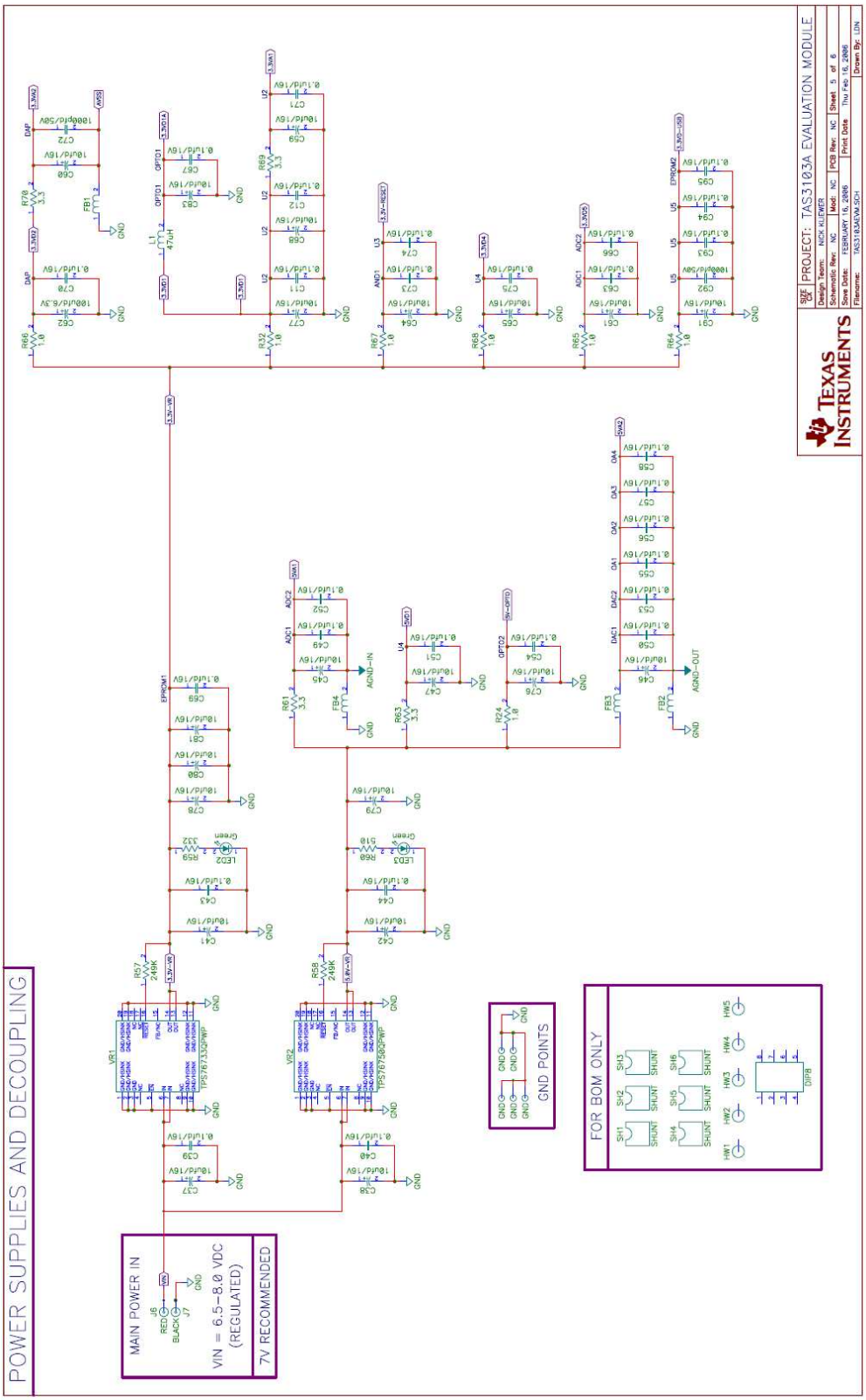

Figure 4-5. TAS3103A EVM Schematic – Power Supplies and Decoupling

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