

# NB3H5150MNGEVB

## NB3H5150MNG Evaluation Board User's Manual



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### Introduction

The NB3H5150MNGEVB evaluation board was developed to provide a flexible and convenient platform to quickly evaluate and verify the operation of the NB3H5150.

This evaluation board manual contains:

- Information on the NB3H5150 Evaluation Board
- Assembly Instructions
- Test and Measurement Setup Procedures
- Board Schematic and Bill of Materials

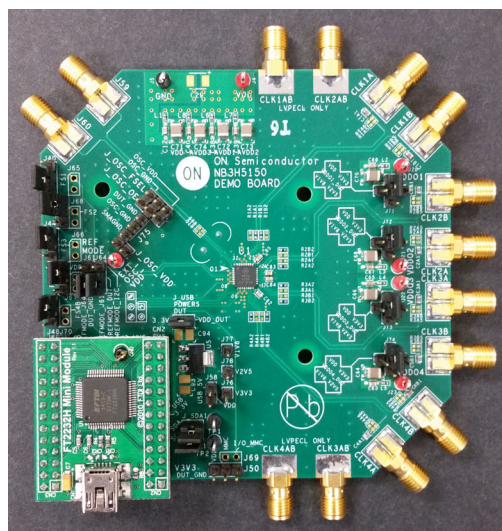
### Board Features

- Accommodates the Electrical Evaluation of the NB3H5150
- Incorporates On-Board I<sup>2</sup>C/SMBus Interface Module Powered via a USB Connection, Minimizing Cabling
- 25 MHz Crystal is Installed (Default Input)
- Differential Inputs/Outputs Signals are Accessed via SMA Connectors or High Impedance Probes
- LVPECL Outputs are DC Loaded and Terminated. Signals then Go through 2:1 Baluns for Direct Connection into Phase Noise Analyzer or High-Z Scope
- LVCMOS Outputs are Series Terminated and Cap Loaded
- Flexible Power Supply Combinations for Device Operation
- Pin-Strap Mode Frequency Select Jumpers
- Convenient and Compact Board Layout

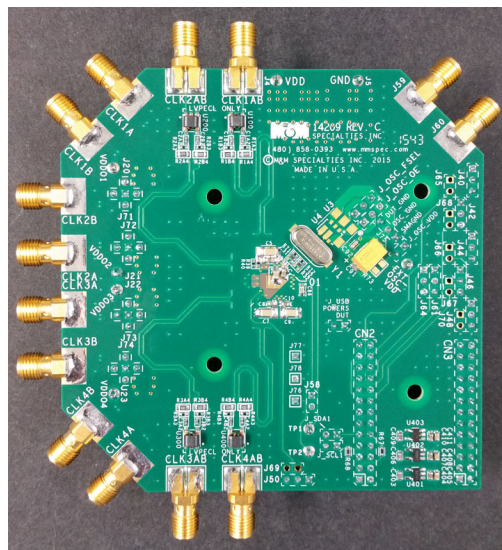
Board must be configured before powering up.

This manual should be used in conjunction with the device data sheet which contains full technical details on the device specifications and operation.

## EVAL BOARD USER'S MANUAL



Top View



Bottom View

Figure 1. NB3H5150MNGEVB Evaluation Board

# NB3H5150MNGEVB

## NB3H5150MNG EVALUATION BOARD – BOARD LAYOUT MAP

Figures 2 & 3 illustrate the locations of major features and components of the NB3H5150MNGEVB. The proceeding

information in this manual will guide the user how to properly configure the NB3H5150 for lab testing.

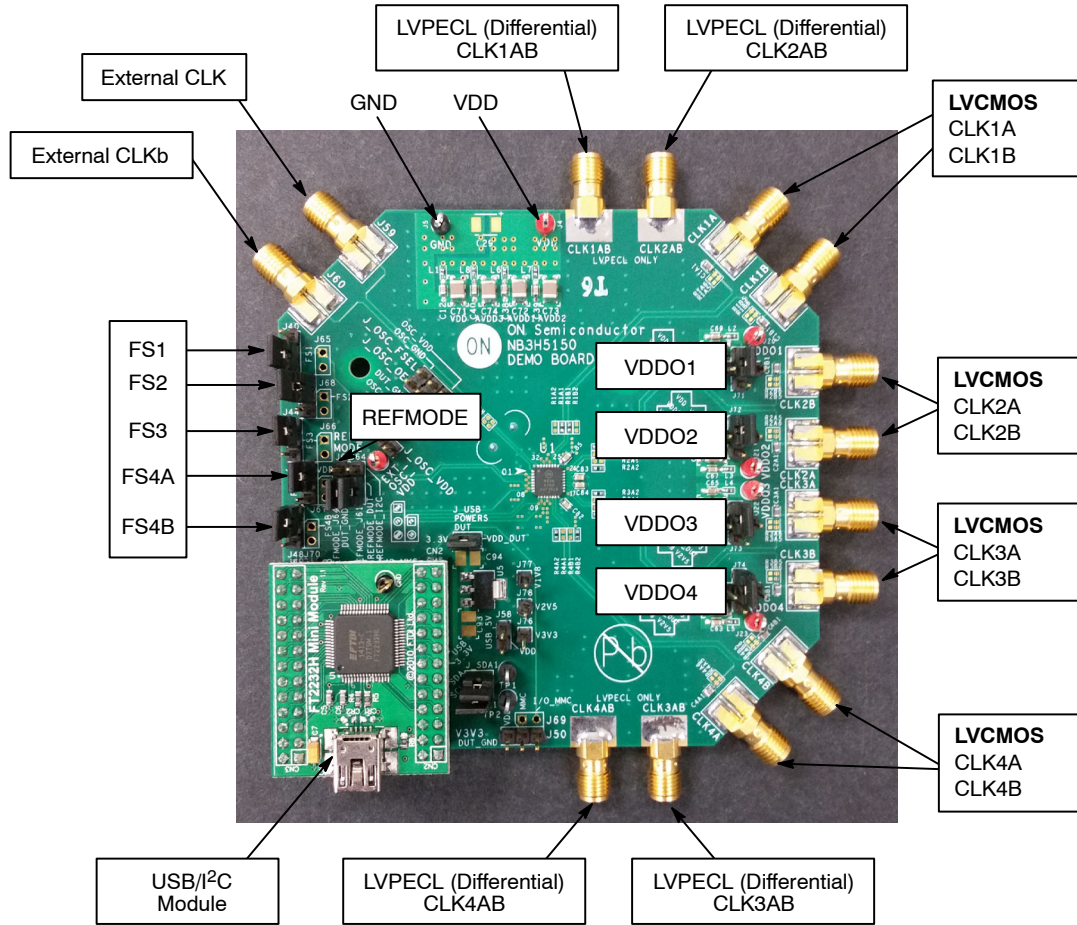


Figure 2. NB3H5150MNGEVB (Top View)

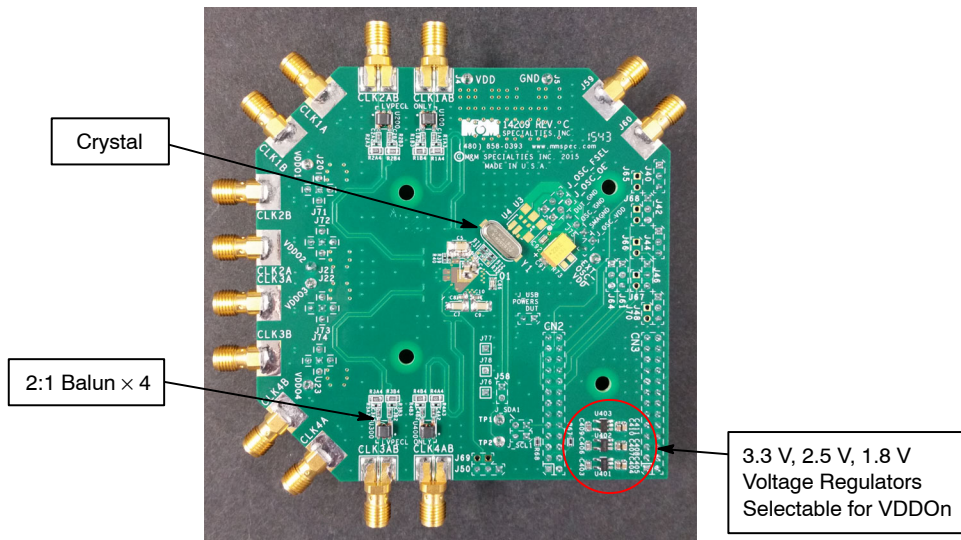


Figure 3. NB3H5150MNGEVB (Bottom View)

# NB3H5150MNGEVB

## STEP 1: POWER SUPPLY FOR EVB

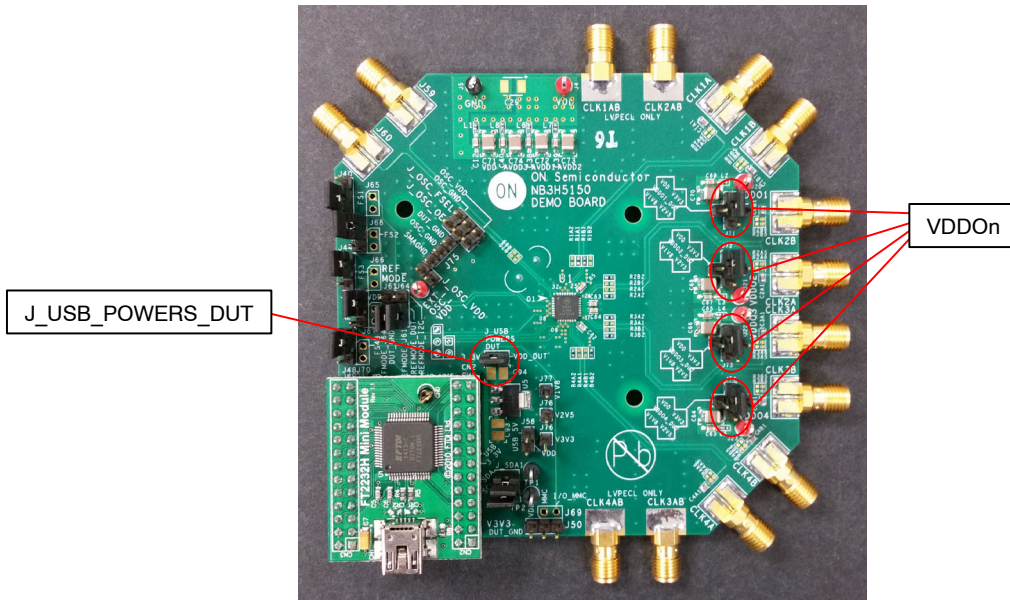
The NB3H5150MNGEVB has the flexibility to be powered either with an external power supply or USB module. Table 1 describes Jumper Setting

J\_USB\_POWERS\_DUT that allows for either configuration.

When USB Powers DUT, VDD = 3.3 V.

**Table 1. NB3H5150MNGEVB DUT POWER JUMPER SETTINGS**

DUT Power	J_USB_POWERS_DUT
External Power Supply	Remove Jumper
USB/I <sup>2</sup> C Module	Install Jumper



**Figure 4. J\_USB\_POWERS\_DUT Board Location**

### Power Supplies

#### VDD, AVDD1, AVDD2 and AVDD3 Power Pins

A single VDD test point connector is connected to the positive power supply and powers each of the VDD and AVDDn power supply pins.

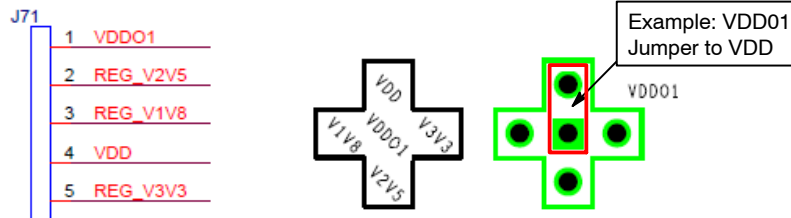
#### VDDOn Power Pins

VDDOn pins can be powered individually:

1. An external power supply connected through J20, J21, J22 and J23. Remove jumpers J71, J72, J73 and J74.

2. VDD of the demo board using jumpers J71, J72, J73 and J74; VDDOn = VDD.
3. Three selectable regulators: **3.3 V** U401, **2.5 V** U402 and **1.8 V** U403, using jumpers J71, J72, J73 and J74; VDDOn = V<sub>REGULATOR</sub>

NOTE: Figure 5 illustrates VDDOn jumper selection options.



**Figure 5. VDDOn Power Supply Options**

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The NB3H5150MNGEVB provides three Voltage Regulators which can be used to power each VDDOn separately. To power these regulators, follow Table 2 for J58 configuration.

J58 enables the optional on-board VDDOn regulators when the device/board is powered by an external power supply.

- When J58 is open, the 3.3 V, 2.5 V and 1.8 V regulators for VDDOn are powered by the USB.
- When J58 is jumpered, the 3.3 V, 2.5 V and 1.8 V regulators are powered by the external VDD power supply.
- When VDD = 2.5 V, VDDOn can not be 3.3 V, only 2.5 V or 1.8 V.

**Table 2. VDDO VOLTAGE REGULATOR POWER**

J58 – VDDO Voltage Regulator Power		
VDDOn Voltage Regulator Power	USB/I <sup>2</sup> C Module	J58
VDD	Do Not Install	Use Jumper
USB/I <sup>2</sup> C Module	Install	No Jumper

**NOTE:** All four VDDOn pins must be connected to a power supply **before** power-up.

**CAUTION:** Neglecting Table 2 configurations may cause damage to USB/I<sup>2</sup>C module.

# NB3H5150MNGEVB

## STEP 2: INPUT CLOCK REFERENCE FOR EVB

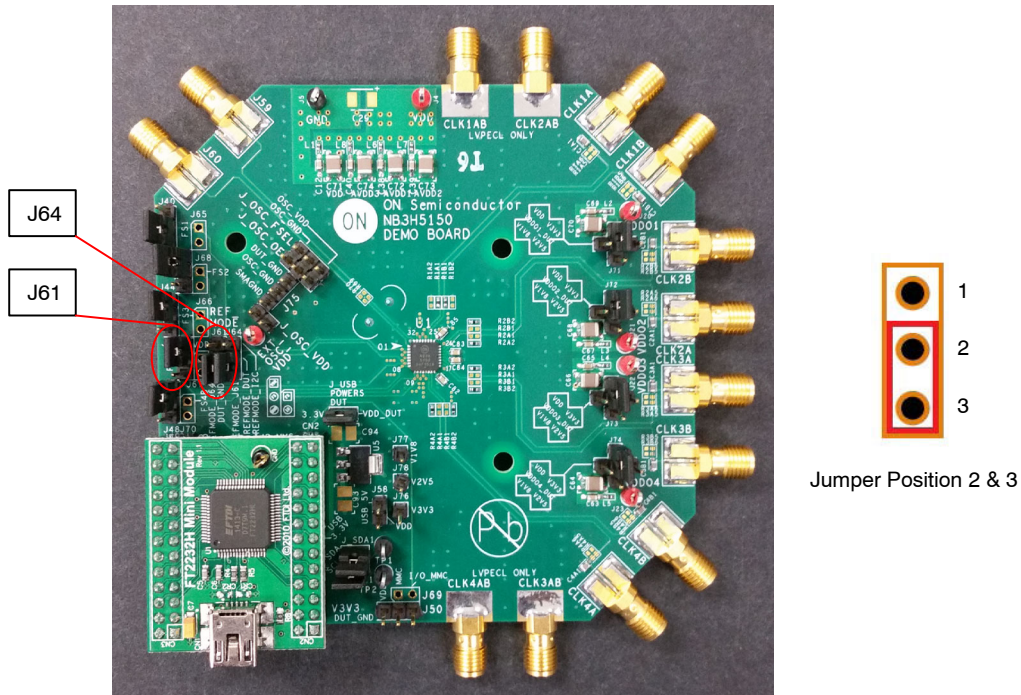
The NB3H5150MNGEVB has the flexibility to accept multiple input clock references, such as: Crystal (mounted on board), Crystal Oscillator, Signal Generator, or separate

clock integrated circuit. Table 3 describes Jumper Settings J64 & J61 that allows for appropriate configuration.

**Table 3. INPUT CLOCK REFERENCE SETTINGS**

Input Clock	REFMODE	
	J61	J64
Crystal	Low	Position 2 & 3 Jumpered
XO	High	Position 2 & 3 Jumpered
Signal Generator	High	Position 2 & 3 Jumpered
IC	High	Position 2 & 3 Jumpered

NOTES: **To use Crystal** – Install R71, R72, C31 & C32 C<sub>LOAD</sub> Capacitors; Remove R69, R70, R31 & R32  
**To use XO** – Install R69 & R70; Remove R71, R72, R31 & R32  
**To use Signal Generator** – Install R69, R70, R31, & R32; Remove R71 & R72



**Figure 6. J61 & J64 Board Location**

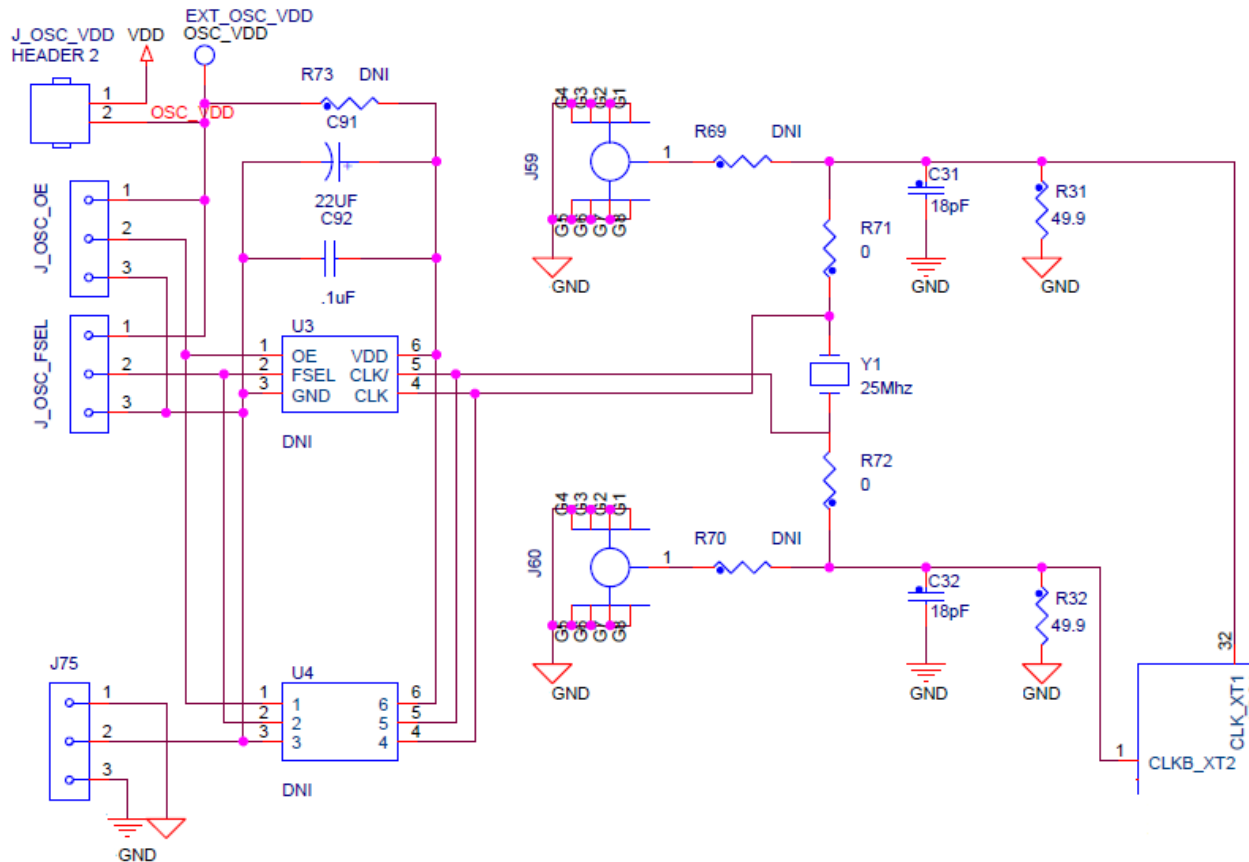
### Crystal Input – (Default Set-Up)

1. Set REFMODE = Low
2. Y1, 25 MHz crystal is installed
3. R31 & R32 are removed; R69 & R70 are not installed.
4. R71 & R72 and C31 & C32 are installed (crystal load capacitors).

### External Clock Source

1. Set REFMODE = High
2. Remove R71 & R72 and C31 & C32
3. R31 & R32 must be installed; and R69 & R70 must be installed.
4. R31 & R32 are 50-Ω to GND and are used to terminate an external signal generator.
5. If CLK\_XTAL1 and CLKb\_XTAL2 pins are driven by another IC device, remove R31 & R32.

## NB3H5150MNGEVB



**Figure 7. Crystal or External Clock Input Configuration Schematic**

### External Crystal Oscillator

The NB3H5150MNGEVB has features to use a 4 or 6-pin XO, U3, in either a  $5 \times 7$  mm or  $3.2 \times 5$  mm package.

1. The XO can be powered separately by:
  - a. VDD of the demo board; connect J\_OSC\_VDD HEADER 2
  - b. An external VDD power supply; connect EXT\_OSC\_VDD at OSC\_VDD.
2. Connect jumper at J75 for the XO GND pin.
3. In either option, install R73, 0- $\Omega$ , to power the XO.
4. C91 & C92 are bypass capacitors for the XO VDD power pin and are installed.
5. If using an XO, J\_OSC\_OE jumper header will control the OE function of the XO, and J\_OSC\_FSEL will control the frequency select option of the XO, if needed.

Also, a crystal in a 4-pin package can be installed over the XO footprint.

### Signal Generator

1. Select Clock Input:
  - a. Differential Input

- i. Connect a signal generator to the J59 & J60 SMA connectors for the CLK\_XTAL1 & CLKb\_XTAL2 inputs.
- ii. Set appropriate input signal levels.
- iii. Install 50- $\Omega$  termination resistors at R31 & R32 for a signal generator termination.
- iv. Remove C31 & C32. Install R69 & R70.
- b. Single-Ended Input:
  - i. Connect a signal generator to the J59 SMA connectors for the CLK\_XTAL1 input.
  - ii. Ground CLKb\_XTAL2.
  - iii. Set appropriate input signal levels.
  - iv. Install 50- $\Omega$  termination resistor at R31 for a signal generator termination.
  - v. Remove C31 & C32. Install R69 & R70.
2. Set REFMODE = High
3. Connect Jumpers to J\_SDA1 and J\_SCL1.
  - a. This will connect SDA & SCL/PD to GND and set the NB3H5150 in Pin-Strap mode.
4. Connect the CLKnA and CLKnB outputs to the appropriate test instrument.
  - a. I.E. Oscilloscope, Phase Noise Analyzer, Frequency Counter, etc.

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## REFMODE

When the REFMODE pin is Low, it selects a crystal for the input.

When the REFMODE pin is High, it selects an external differential or single-ended clock source for the input.

For manual control:

1. J64
  - a. Jumper across pins 2 & 3 to select manual control of REFMODE and then use J61.
2. J61
  - a. 1 & 2 = High (VDD) – For External Clock Source Input
  - b. 2 & 3 = Low (GND) – For Crystal Input

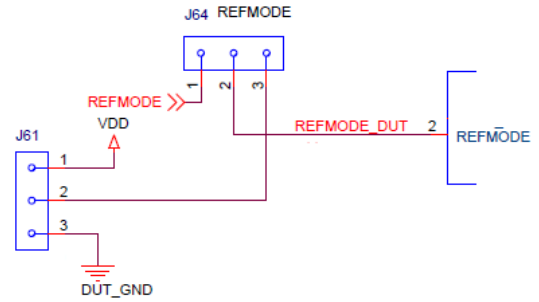


Figure 8. REFMODE Jumper Settings

# NB3H5150MNGEVB

## STEP 3: PIN-STRAP OR I<sup>2</sup>C MODE FOR EVB

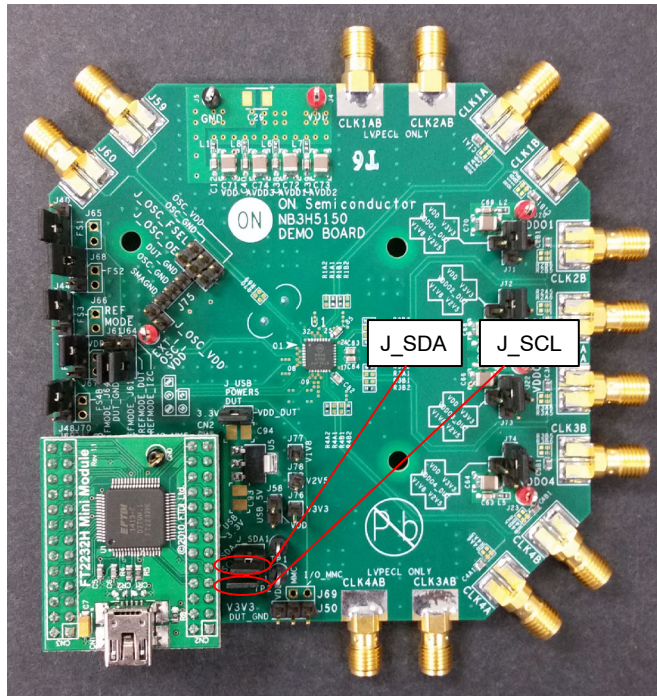
The NB3H5150MNGEVB has the flexibility of two methods of selecting output frequencies and level types. Pin-Strap selections are limited to those described in data sheet. Refer to Tables 3 & 4 of data sheet for selectable frequencies and levels. While using I<sup>2</sup>C with provided USB

module and Software GUI, various frequency and level types' combinations can be generated. Table 4 describes Jumper Settings J\_SDA1, JSCL1 that allow for appropriate configuration.

**Table 4. PIN-STRAP OR I<sup>2</sup>C SETTINGS**

Pin-Strap or I <sup>2</sup> C Mode	J_SDA1 & J_SCL1
Pin-Strap	Install Jumper
I <sup>2</sup> C	Remove Jumper

NOTE: For I<sup>2</sup>C Mode – Install the USB/I<sup>2</sup>C module and power-up with cable from PC, when VDD = 3.3 V.



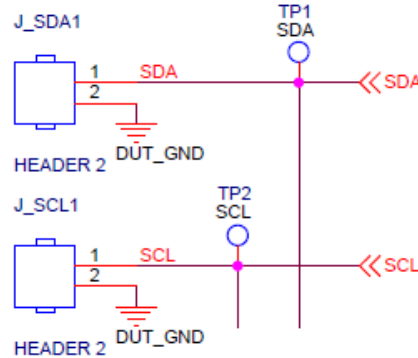
**Figure 9. J\_SDA, J\_SCL Board Location**

### Pin-Strap Operation

1. Connect a jumper across J\_SDA1 and J\_SCL1.
  - a. This will connect both SDA and SCL/PD pins to GND.

### I<sup>2</sup>C Operation

1. Remove jumpers from J\_SDA1 and J\_SCL1.
  - a. The powered I2C module will then connect both SDA and SCL/PD pins to VDD via pull-up resistors.



**Figure 10. SDA and SCL/PD Jumper**



## NB3H5150MNGEVB

### Control Pins

Each control pin can be managed manually with H/L jumper header; H = VDD, L = GND.

### Tri-Level Input Pins – FSn – Frequency Select pins for CLK<sub>n</sub>

The five tri-level input pins, FS1, FS2, FS3, FS4A and FS4B have selectable levels.

Reference Tables 3 & 4 of NB3H5150 data sheet for pin-strap frequency settings.

The logic levels for the FSn pins can be selected manually by using respective Jumpers.

Figure 11 is an example of control pin FS1 controlling logic levels for CLK1.

### Jumper Levels

For a **HIGH** Level – Put Jumper to VDD

For a **LOW** Level – Put Jumper to GND

For a **Mid-Level** – No Jumper or left open; This will enable internal pull-up and pull-down circuits to default to mid-level logic.

FSn pins can also be controlled through the I<sup>2</sup>C and GUI. When controlling FSn pins via I<sup>2</sup>C, do not install jumpers on J65, J66, J67, J68, J69, J70.

### Two-Level Input Pins – REFMODE, SDA, SCL/PD and MMC

The two-level input pins can also be controlled with H/L jumpers.

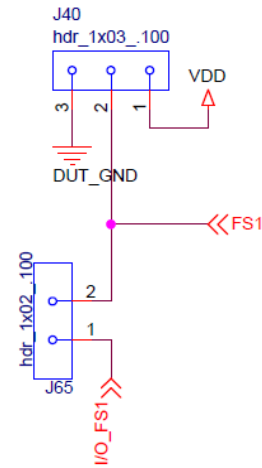


Figure 11. FS1 Jumper Setting

# NB3H5150MNGEVB

## STEP 4: OUTPUT LEVEL SELECTION FOR EVB

The NB3H5150MNGEVB has the flexibility of two output types (LVPECL & LVC MOS) across four output banks. Each output channel has the ability to drive LVC MOS and LVPECL levels. When evaluating LVC MOS, CLKnA & CLKnB are to be used. When

evaluating LVPECL, the NB3H5150MNGEVB has the ability to view signal differentially and single ended. The user must determine the output level and the respective CLKnA, CLKnB, and CLKnAB interface in order to configure the board correctly.

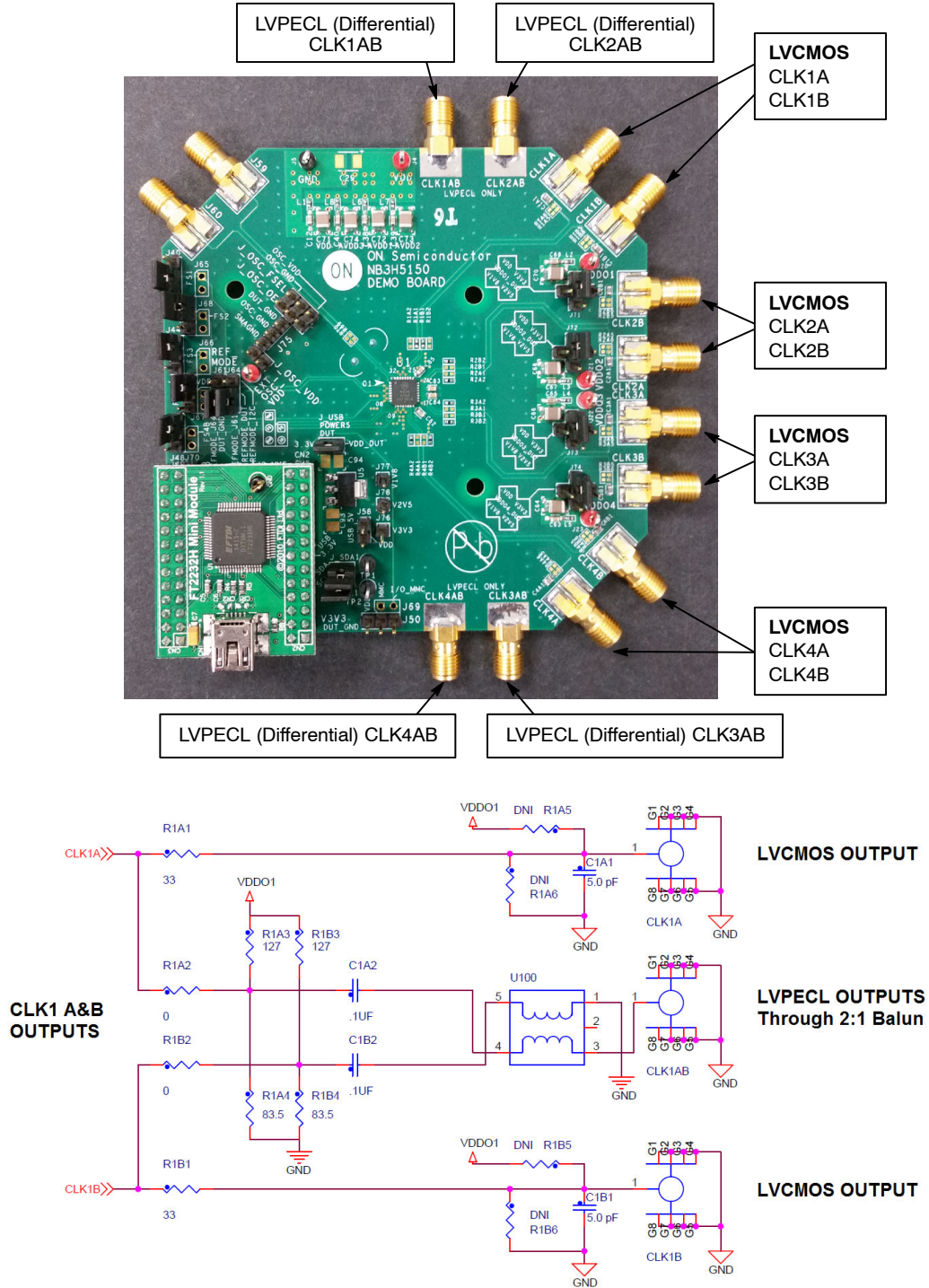


Figure 12. Output Selection Capabilities

CAUTION: \*CLK1, CLK2, CLK3 & CLK4 pairs are configured as both LVC MOS and LVPECL outputs.

## NB3H5150MNGEVB

The user must determine each output type and configure the outputs accordingly by removing the appropriate components to establish one signal output path.

**LVC MOS Output Configuration** – Remove R1A2 and R1B2; R1A1 and R1B1 remain installed; The LVC MOS outputs have provisions for a series  $R_S$  and a  $C_{Load}$ ;  $R_S = 33\text{-}\Omega$  and  $C_{Load} = 5\text{ pF}$  are installed.

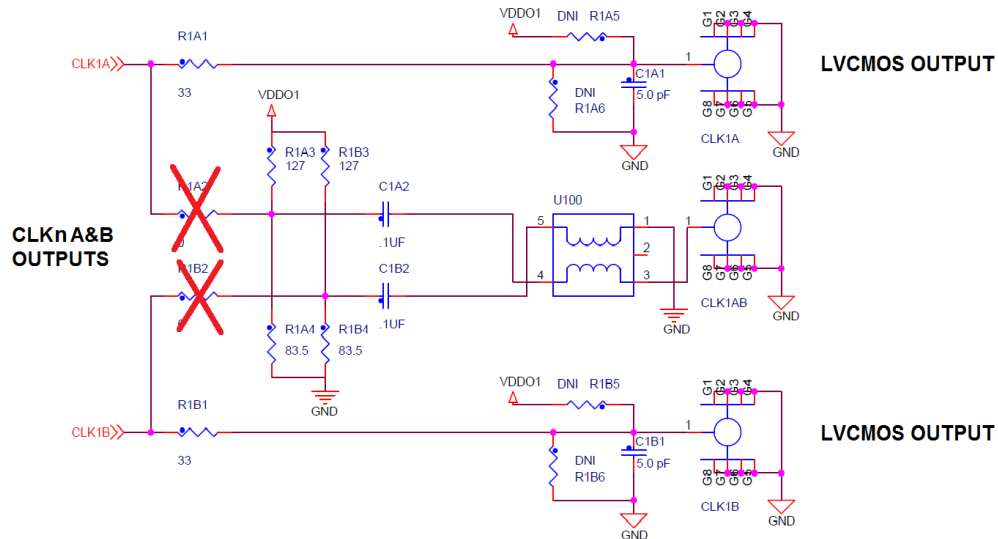


Figure 13. LVC MOS Output Configuration

**LVPECL Output Configuration** – Remove R1A1 and R1B1; R1A2 and R1B2 remain installed; R1A3 & R1A4 and

R1B3 & R1B4 are Thevenin equivalent DC load and AC termination resistors.

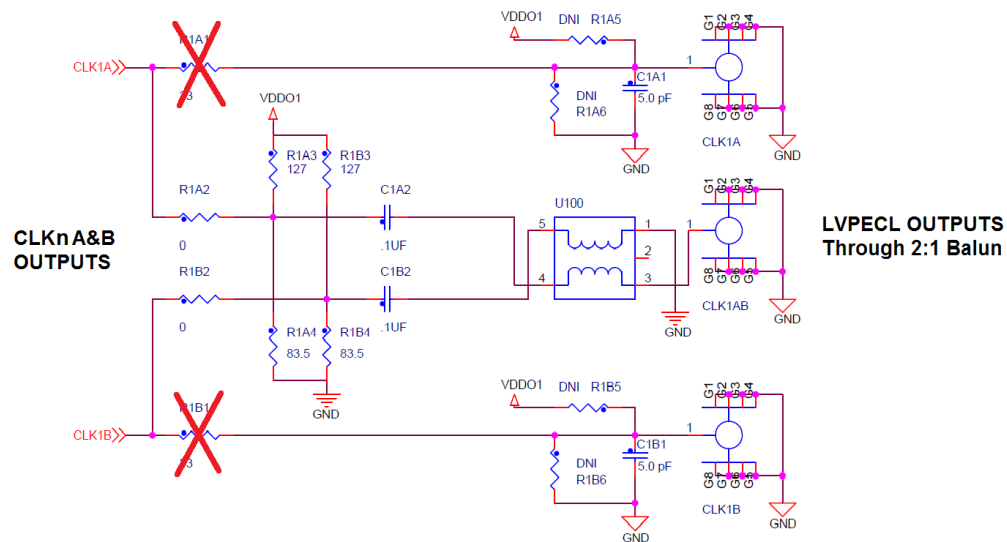


Figure 14. LVPECL Output Configuration

The differential LVPECL outputs are DC loaded and AC terminated with Thevenin resistors, capacitor-coupled into U100, a 2:1 balun which creates a true differential signal. This signal connects directly into a test instrument, primarily a phase noise analyzer, an oscilloscope with a high-Z probe, frequency counter, etc.

**NOTES:** In pin-strap mode, the NB3H5150 CLK1 defaults to LVC MOS only, and CLK2 defaults to LVPECL only. Therefore, on the EVB, remove the appropriate resistors such that CLK1A & CLK1B defaults to LVC MOS output configuration, and the CLK1AB SMA connector is open (Figure 13).

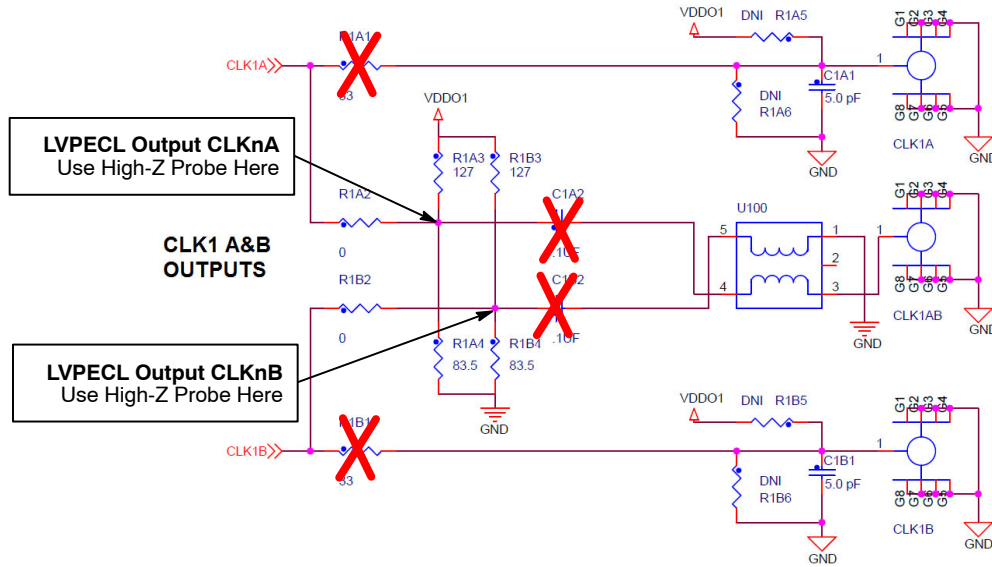
Use a high-Z probe on the two single-ended outputs. CLK2 defaults to differential LVPECL output configuration. Remove the appropriate resistors such that the CLK2AB SMA connector is used and CLK2A & CLK2B SMA connectors are open (Figure 14).

**LVPECL Complementary Single Ended Output Configuration**

The NB3H5150 EVB has the ability to observe LVPECL waveforms single-ended using the two separate options. Components will either need to be added or removed for appropriate configuration. The following describes the two options to view LVPECL as complementary single-ended waveforms.

*Option 1*

1. The LVPECL outputs can be observed at the Thevenin termination resistors, but C1A2 and C1B2 must be removed, as the cap-coupled balun will affect the signal at this node. Observe the two single-ended LVPECL outputs with Hi-Z probe at the nodes below with a high-Z probe.

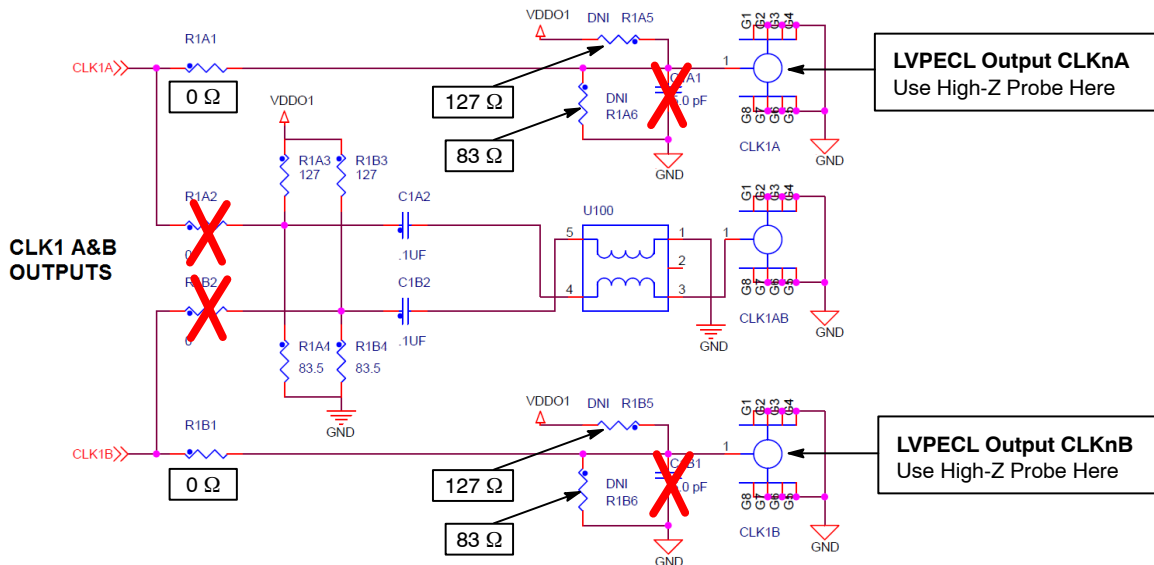


**Figure 15. LVPECL Outputs – Optional Set-Up**

*Option 2*

The LVPECL outputs can also be monitored by modifying a few board components: remove R1A2 & R1B2, Replace

R1A1 & R1B1 with 0-Ω resistors, remove 5-pF, install Thevenin resistors R1A5 & R1A6 and R1B5 & R1B6.



**Figure 16. LVPECL Outputs – Optional Set-Up**

# NB3H5150MNGEVB

## STEP 5: POWER SEQUENCE FOR EVB

The NB3H5150 EVB has the flexibility of being powered by two different methods; external power supply or via USB module connection.

### External Power Supply

1. Connect power supply cables to VCC and GND connectors.
2. Configure board according to Steps 1 through 4.
3. Turn on VDD power supply
4. Monitor CLKnA & CLKnB outputs on oscilloscope or other test instrument.

### USB Power Supply

1. Configure board according to Steps 1 through 4.
2. Connect USB cable to I2C Module
3. Monitor CLKnA & CLKnB outputs on oscilloscope or other test instrument.

**\*When using an external clock source, board must be powered first.**

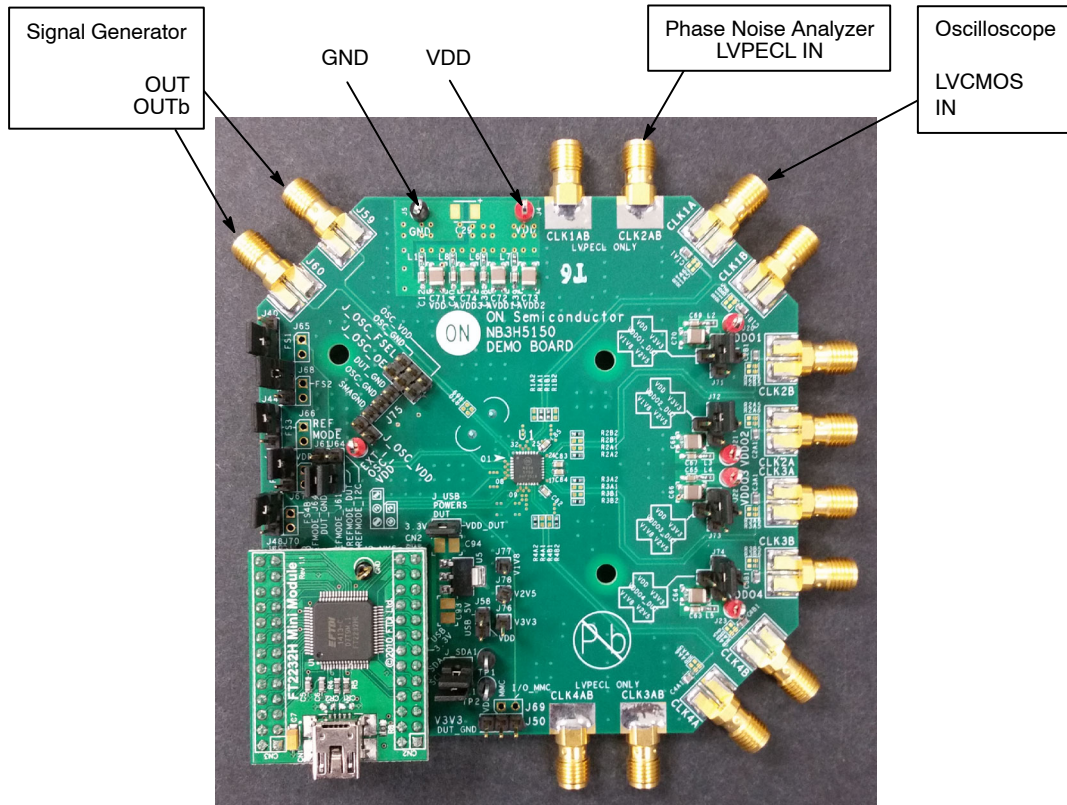


Figure 17. Power Sequence Diagram

### Graphical User Interface (GUI)

There is a stand-alone Graphical User Interface software package and GUI user's manual that will interface with the DUT via the USB connector.

### USB & I<sup>2</sup>C/SMBus Interface

The NB3H5150 EVB has an on-board I<sup>2</sup>C/SMBus interface module located in the lower left section of the board.

This circuitry will interface the device with the GUI software via the SDA and SCL/PD input pins. The GUI can control the Frequency Select pins, output types, output enable, and PLL ByPass Mode.

### SCL/PD & SDA

The SMBus Clock (SCL/PD) and Data (SDA) pins are exercised through the on-board I<sup>2</sup>C interface.

In order to enable the I<sup>2</sup>C control of the DUT, see Step 3. The I<sup>2</sup>C/SMBus interface circuitry is powered separately from the USB type-B connection and is isolated from the device VDD and VDDOn. The SDA and SCL/PD pins can also be externally accessed by an off-board programmer, allowing other SMBus emulators to be used to program the DUT. "Test-point anvils" TP5 & TP6 are available for external control of the device with the use with mini-grabber cables.

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## Graphical User Interface Set-Up

1. Connect the USB port on the evaluation board to a USB port via PC cable.
2. See the stand-alone GUI instructions document.
3. Allow Windows to install the necessary drivers for the evaluation board USB interface hardware.
4. Start the GUI program.

## Board Layout

The NB3H5150 QFN-32 Evaluation Board provides a high bandwidth, 50- $\Omega$  controlled trace impedance environment (100- $\Omega$  line-to-line differential) and is implemented in six layers.

All layers are constructed with FR4 dielectric material.

### Layer Stack

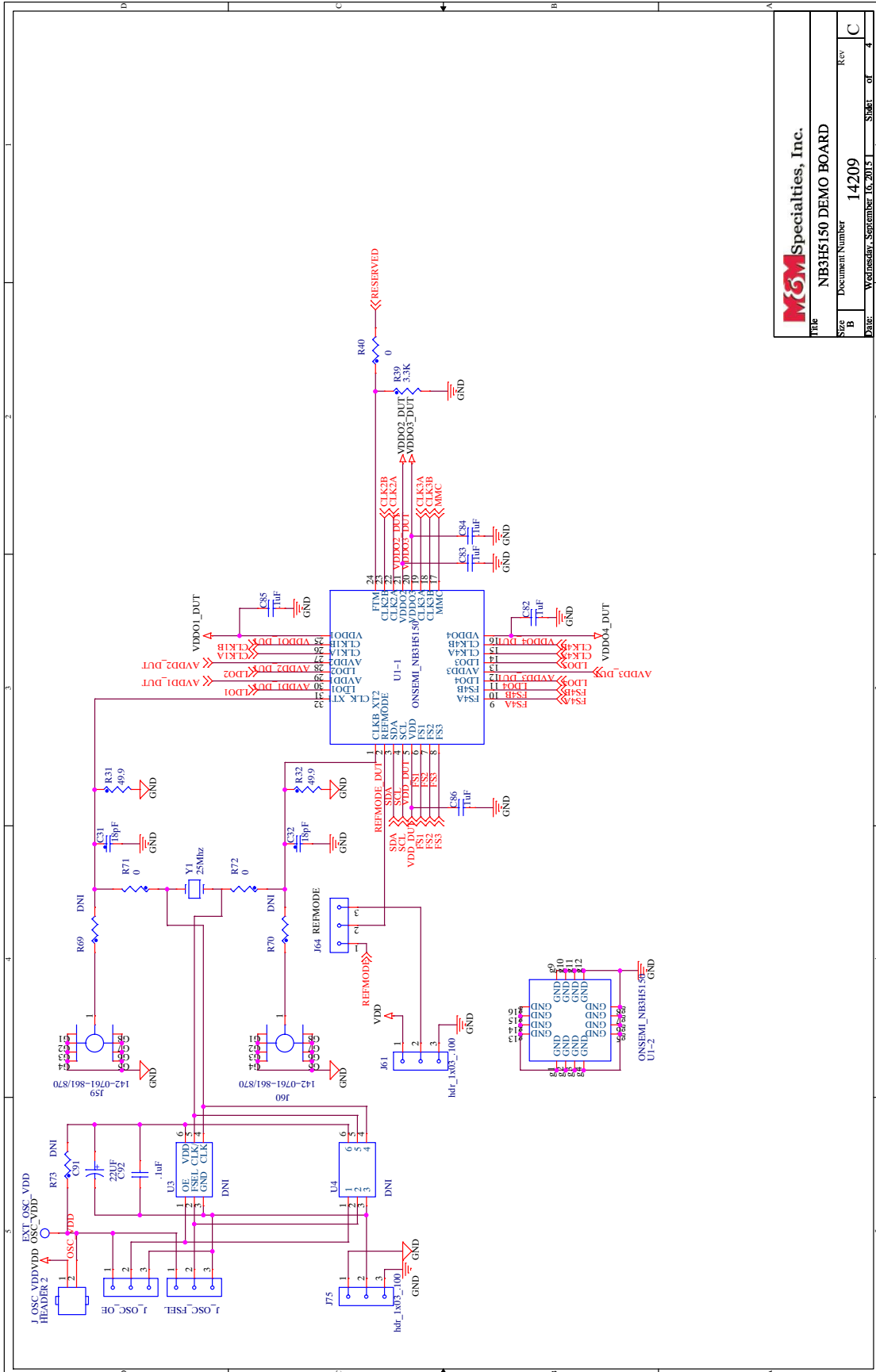
- L1 (Top) Signal
- L2 Ground
- L3 Power
- L4 Power
- L5 Ground
- L6 (Bottom) Signal

STACKUP: 6 LAYERS				IMPEDANCE	
Layer Number	Layer Name	Thickness (Inches)	Material	$\Omega$ ( $\pm 5\%$ )	Line Width
1	Top	0.0012	Copper	50, 100	0.010; 0.012
-	Dielectric	0.0080	FR-4	-	-
2	GND	0.0012	Copper	-	-
-	Dielectric	0.0040	FR-4	-	-
3	PWR1	0.0012	Copper	-	-
-	Dielectric	ADJUST	FR-4	-	-
4	PWR2	0.0012	Copper	-	-
-	Dielectric	0.0040	FR-4	-	-
5	GND	0.0012	Copper	-	-
-	Dielectric	0.0080	FR-4	-	-
6	Bottom	0.0012	Copper	50, 100	0.010; 0.012

Figure 18. NB3H5150MNG Evaluation Board Layer Stack-Up

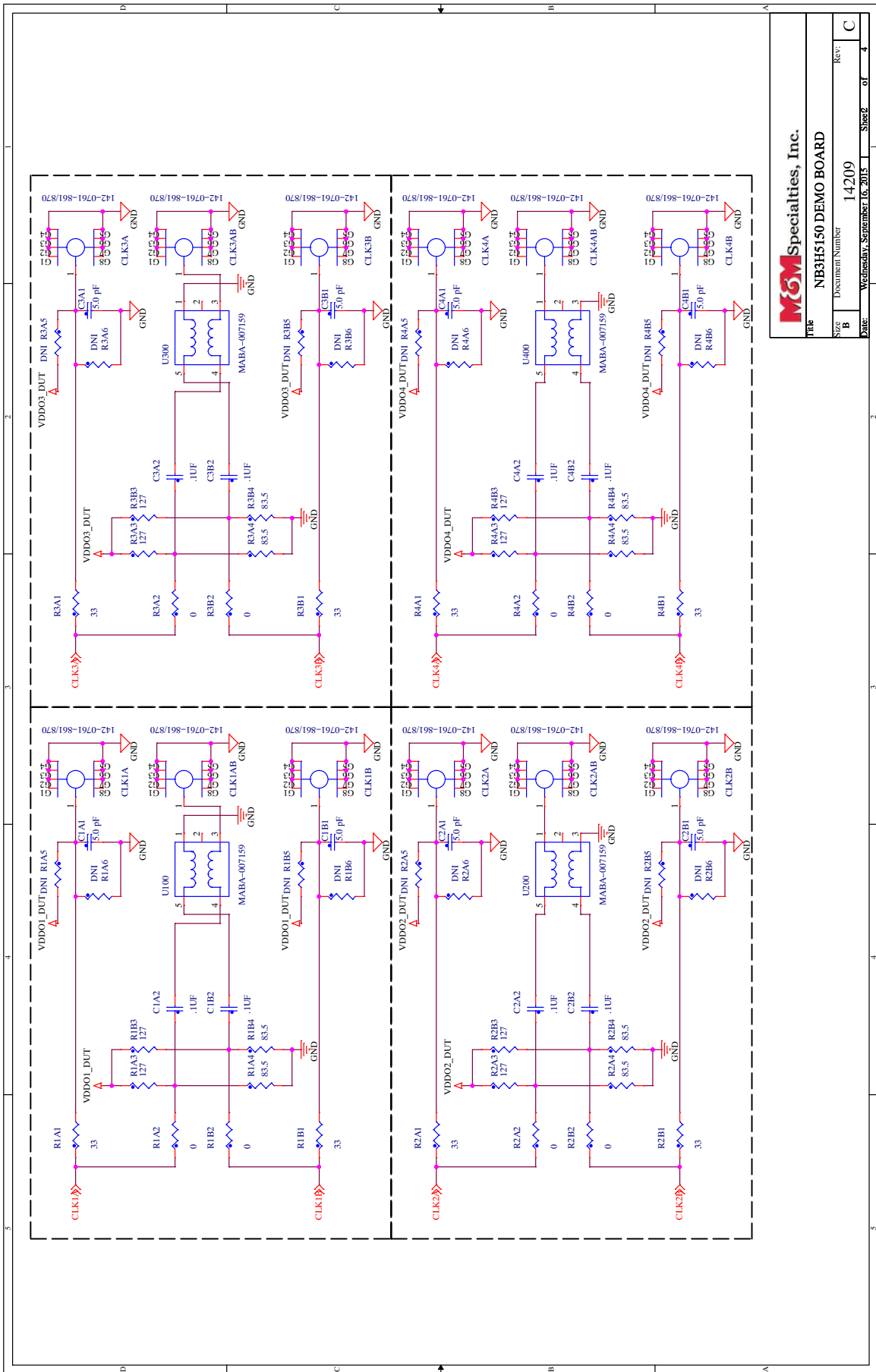
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## SCHEMATICS



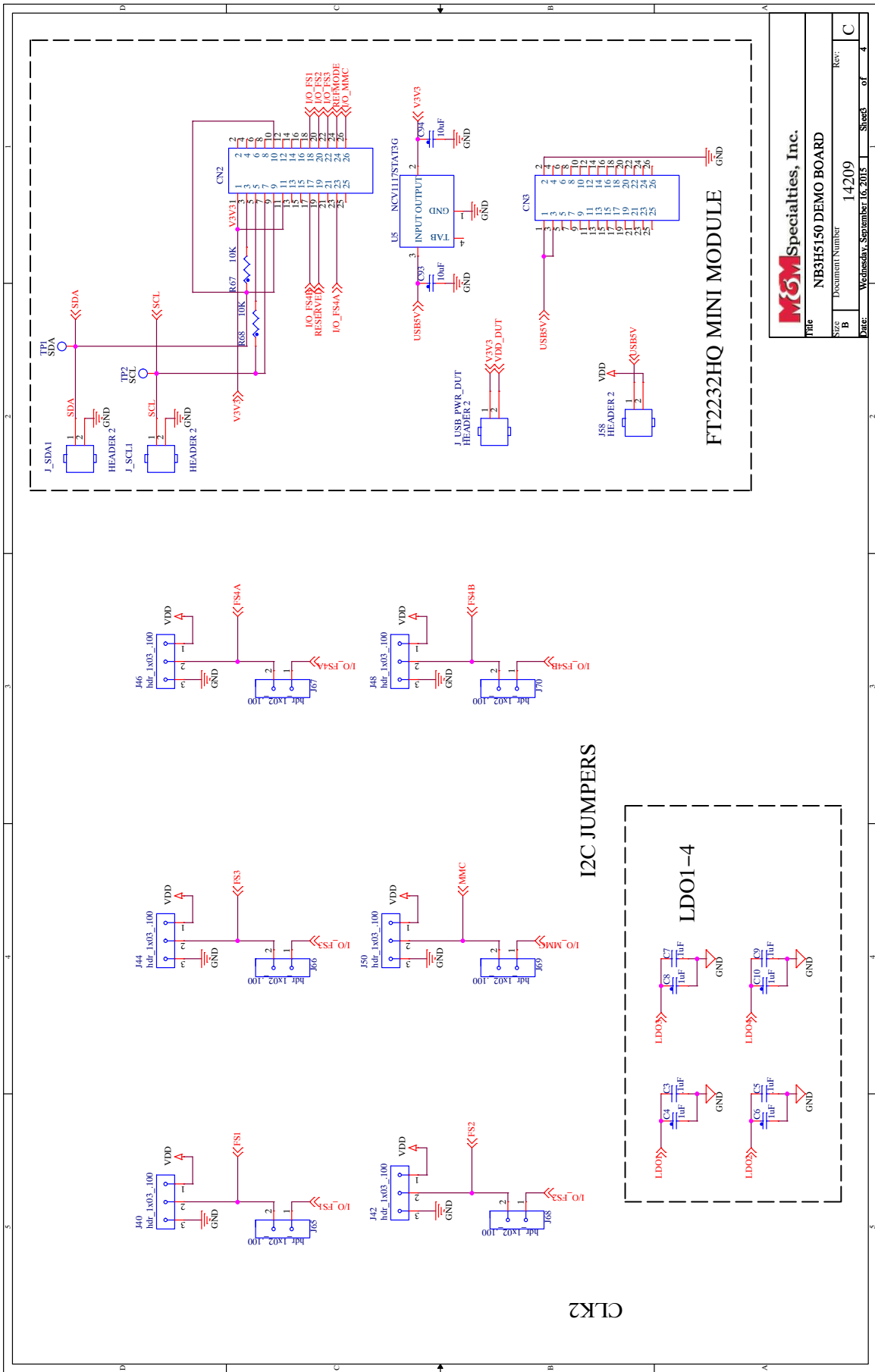
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THE NB3H5150 DEMO BOARD	
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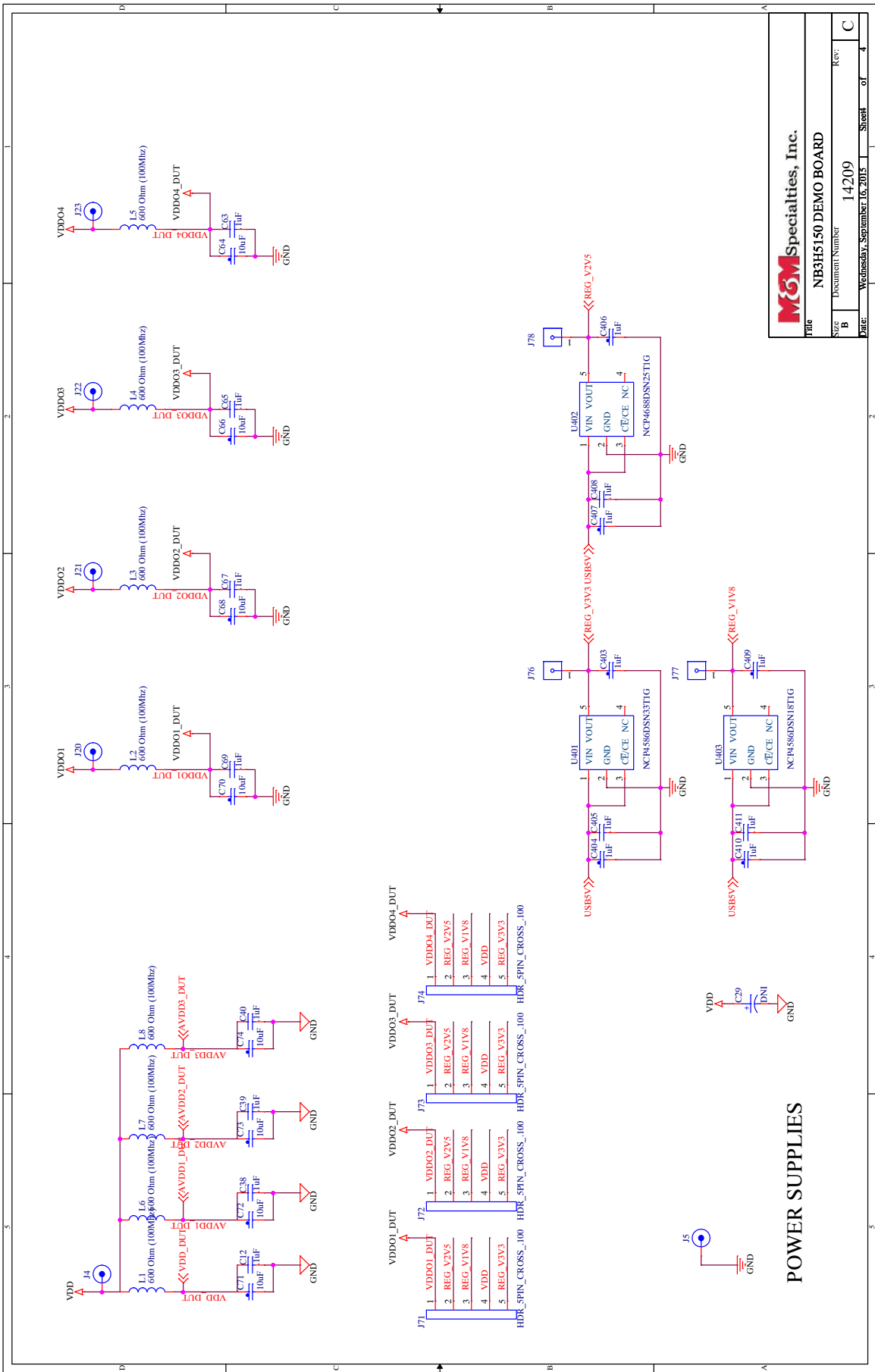


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Title NB3H5150 DEMO BOARD	
Size B	Document Number 14209
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POWER SUPPLIES

# NB3H5150MNGEVB

## BILL OF MATERIALS

**Table 5. NB3H5150MNGEVB BILL OF MATERIALS**

MM_ICN#	COMP_DEVICE_TYPE	COMP_VALUE	SOURCE	SOURCE_PN#	QTY	REFDES
80-111-00666	CAP, CER, 0.1 $\mu$ F, 50 V, 10%, X5R, 0402	0.1 $\mu$ F	Digi-Key	445-5942-1-ND	8	C1A2, C1B2, C2A2, C2B2, C3A2, C3B2, C4A2, C4B2
80-111-00219	Cap, Chip, 18 pF, 0402, 10 V, $\pm$ 2%	18 pF	Digi-Key	478-4435-1-ND	2	C31, C32
80-111-00031	Cap, Chip, 1 $\mu$ F, 0603, 10V, 10%, X7R	1 $\mu$ F	SMEC	MCCB105K1NRT	10	C4, C6, C8, C10, C403, C404, C406, C407, C409, C410
80-111-00147	CAP, CER, 0.1 $\mu$ F, 50 V, 10%, X7R, 0603	0.1 $\mu$ F	Digi-Key	490-1519-1-ND	17	C12, C38, C39, C40, C63, C65, C67, C69, C82, C83, C84, C85, C86, C92, C405, C408, C411
80-111-00536	Cap, Chip, 5.0 pF, 0603, 50 V	5.0 pF	Digi-Key	GRM1885C1H5R0CZ01D	8	C1A1, C1B1, C2A1, C2B1, C3A1, C3B1, C4A1, C4B1
80-111-00255	Cap, Chip, 0.1 $\mu$ F, 0805, 50 V, 5% X7R	0.1 $\mu$ F	Digi-Key	MOUSER 581-05055C104J	1	C3
80-111-00796	Cap, Cer, 1206, 50 V, 0.1 $\mu$ F, X7R, 10%	0.1 $\mu$ F	Digi-Key	478-1556-1-ND	3	C5, C7, C9
80-111-00074	Cap, Chip, 10 $\mu$ F, 1210, 10 V, 10%, X5R	10 $\mu$ F	Digi-Key	587-1370-1-ND	8	C64, C66, C68, C70, C71, C72, C73, C74
DNI	CAP_DNI_TANTB	DNI	DNI	DNI	1	C29
80-111-00197	Cap, Chip, 22 $\mu$ F, Tant "D", 25 V 10%	22 $\mu$ F	Digi-Key	478-1729-1-ND	1	C91
0805N	RES_DNI_0805	DNI	DNI	DNI	1	R73
DNI	Res, Chip, 49.9 $\Omega$ , 0402, 1/16 W, 1%	49.9 $\Omega$	Digi-Key	P49.9LCT-ND 80-114-00163	2	R31, R32
80-114-01607	Res SMD 3.3 k $\Omega$ 1% 1/16 W 0402	3.3 k $\Omega$	Digi-Key	RHM3.3KCDTR-ND	1	R39
80-114-00052	Res, Chip, 0 $\Omega$ , 0402, 1/16 W, 5%	0 $\Omega$	Digi-Key	311-0.0JRTR-ND	9	R40, R71, R72, R2A2, R2B2, R3A2, R3B2, R4A2, R4B2
DNI	Res, Chip, 0 $\Omega$ , 0402, 1/16 W, 5%	0 $\Omega$	Digi-Key	311-0.0JRTR-ND	2	R1A2, R1B2
0402N	RES_0_1/16W_5%_0402	DNI	DNI	DNI	2	R69, R70
80-114-00473	Res, Chip, 33 $\Omega$ , 0402, 1/16 W, 5%	33 $\Omega$	SMEC	RC73L2Z330JT	2	R1A1, R1B1
DNI	Res, Chip, 33 $\Omega$ , 0402, 1/16 W, 5%	33 $\Omega$	SMEC	RC73L2Z330JT	6	R2A1, R2B1, R3A1, R3B1, R4A1, R4B1
80-114-01612	Res SMD 127 $\Omega$ 1% 1/16 W 0402	127 $\Omega$	Digi-Key	541-127LDKR-ND	8	R1A3, R1B3, R2A3, R2B3, R3A3, R3B3, R4A3, R4B3
0402S1	RES_DNI_0402	DNI	DNI	DNI	16	R1A5, R1A6, R1B5, R1B6, R2A5, R2A6, R2B5, R2B6, R3A5, R3A6, R3B5, R3B6, R4A5, R4A6, R4B5, R4B6
80-114-01460	Res 10 k $\Omega$ 1/10 W 1% 0603 SMD	10 k $\Omega$	Digi-Key	P10.0KHCT-ND	2	R67, R68
80-114-01628	Res SMD 82 $\Omega$ 0.1% 0.15 W 0805	82.5 $\Omega$ , 0603	Digi-Key	ERA-6AEB820V; P82DACT-ND	8	R1A4, R1B4, R2A4, R2B4, R3A4, R3B4, R4A4, R4B4
80-118-00259	IND_FERRITE-BEAD_60_0OHM_100MHZ*	600 $\Omega$ (100 MHz)	Digi-Key	587-1846-1-ND	8	L1, L2, L3, L4, L5, L6, L7, L8
80-118-00260	TRANSFORMER	MABA-007159	Digi-Key	1465-1302-1-ND	4	U100, U200, U300, U400
80-080-00330	CONN SMA JACK 50 $\Omega$ EDGE MNT	SMA 142-0761-861	Digi-Key	J805-ND	14	CLK1A, CLK1AB, CLK1B, CLK2A, CLK2AB, CLK2B, CLK3A, CLK3AB, CLK3B, CLK4A, CLK4AB, CLK4B, J59, J60
80-112-00108	Connector, Header, 50 Pos, 0.100"	HDR_1x01	Samtec	TSW-150-14-G-S	3	J76, J77, J78
DNI	Connector, Header, 50 Pos, 0.100"	hdr_1x02_100	Samtec	TSW-150-14-G-S	6	J65, J66, J67, J68, J69, J70
80-112-00108	Connector, Header, 50 Pos, 0.100"	hdr_1x03_100	Samtec	TSW-150-14-G-S	13	J40, J42, J44, J46, J48, J50, J61, J62, J63, J64, J75, J_OSC_FSEL, J_OSC_OE

# NB3H5150MNGEVB

**Table 5. NB3H5150MNGEVB BILL OF MATERIALS** (continued)

MM_ICN#	COMP_DEVICE_TYPE	COMP_VALUE	SOURCE	SOURCE_PN#	QTY	REFDES
80-112-00249	CONN HEADER FMAL 26PS.1" DL GOLD	26 pis conn	Digi-Key	S7116-ND	2	CN2, CN3
80-112-00108	HDR_5PIN_CROSS_100 _HEADER, MAL	HDR_1x01(5 pin)	Samtec	TSW-150-14-G-S	4	J71, J72, J73, J74
80-112-00108	Connector, Header, 50 Pos, 0.100"	hdr_1x02_100	Samtec	TSW-150-14-G-S	5	J58, J_OSC_VDD, J_SCL1, J_SDA1, J_USB_PWR_DUT
DNI	OSC_ON_NBXDBA014_ CLCC_7X5_254_D	DNI	DNI	DNI	1	U3
DNI	OSC_ECS_SUBMINIATU RE_OSC_MINI_6	DNI	DNI	DNI	1	U4
80-112-00199	TEST POINT, PC, MULTI PURPOSE, RED	TP RED	Digi-Key	5010K-ND	6	J4, J5, J20, J21, J22, J23
80-112-00148	TEST POINT, PC, MULTI PURPOSE, BLK	TP BLK	Digi-Key	5011K-ND	1	EXT_OSC_VDD
80-112-00148	TEST POINT, PC, MULTI PURPOSE, BLK	TP BLK	Digi-Key	5011K-ND	1	TP1
80-112-00148	TEST POINT, PC, MULTI PURPOSE, BLK	TP BLK	Digi-Key	5011K-ND	1	TP2
80-113-00905	Crystal, CTS, 25 MHz, TH	25 MHz	Digi-Key	ABL-25.000MHZ-B2F	1	Y1
80-116-00527	IC REG LDO 3.3 V 0.15 A SOT23-5	3.3 V	Digi-Key	NCP4586DSN33T1G-ND	1	U401
80-116-00526	IC REG LDO 2.5 V 0.15 A SOT23-5	2.5 V	Digi-Key	NCP4688DSN25T1GOSCT-N D	1	U402
80-116-00528	IC REG LDO 1.8 V 0.15 A SOT23-5	1.8 V	Digi-Key	MIC5247-1.8YM5TR	1	U403
80-116-00549	IC REG LDO ADJ 1 A SOT223		Digi-Key	NCV1117STAT3G	1	U5
CSP	ONSEMI_NB3H5150_SK T_MM_50-000-0	QFM	ON Semiconductor	NB3H5150	1	U1
80-080-00327	Conn Jumper	Jumper	Digi-Key	S9341-ND	28	
80-080-00337	USB Cable - USB A Mini-B 1.8M Frost White		DNI	88732-8800	1	
80-113-00906	USB Hi-Speed FT2232H Evaluation Module		DNI	FT2232H Mini Module	1	

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