DS125BR401AEVM User’s Guide

User's Guide

Literature Number: SNLU150A
September 2013–Revised March 2014

DS125BR401AEVM Evaluation Kit

The DS125BR401AEVM – SMA evaluation kit provides a complete high band-width platform to evaluate the signal integrity and signal conditioning features of the Texas Instruments signal conditioning products – with Equalization and De-emphasis. SMA edge launch connectors are used as the input and the output connections for this evaluation board. Commercially available adaptor boards can be purchased to facilitate connection to cables or backplane interconnects.

Topic **Page**

1 **Features** 3
2 **4-Level IO Control** 5
3 **Switch Connection Overview** 6
4 **Quick Start Guide** 7
5 **SMBus Slave Mode of the EQ, VOD, and De-Emphasis level:** 10
6 **Bill of Materials** 11
7 **Schematic** 12
8 **EVM Layout** 13

1 Features

- 4 Lane Repeater with Equalization up to 12 Gbps
- Low 65 mW/channel power consumption, with option to power down unused channels
- Linear Equalization allows for Link Training protocol for PCIe and SAS
- Supports Out-of-Band Signaling
- B-Side: Receive Equalization up to 24 dB at 6 GHz
- B-Side: Transmit de-emphasis driver > 10 dB
- B-Side: Transmit voltage control: 700 – 1300 mV
- A-Side: Receive Equalization up to 10 dB at 6 GHz
- A-Side: Linear output drive
- A-Side: Maximum output voltage range over 1200 mV
- Programmable via Terminal selection, EEPROM, or SMBus interface
- Single supply operation: VIN = 3.3V±10% or VDD = 2.5V ±5%
- -40°C to +85°C Operation
- 4 kV HBM ESD rating
- High speed signal flow–thru pin-out package: 54-pin QFN (10 mm x 5.5 mm, 0.5 mm pitch)

Applications

FR-4 Backplane Traces and High Speed Cable in serial interfaces up to 12 Gbps

Ordering Information

EVM ID	DEVICE ID	DEVICE PACKAGE
DS125BR401AEVM	DS125BR401ANJYT	WQFN-54

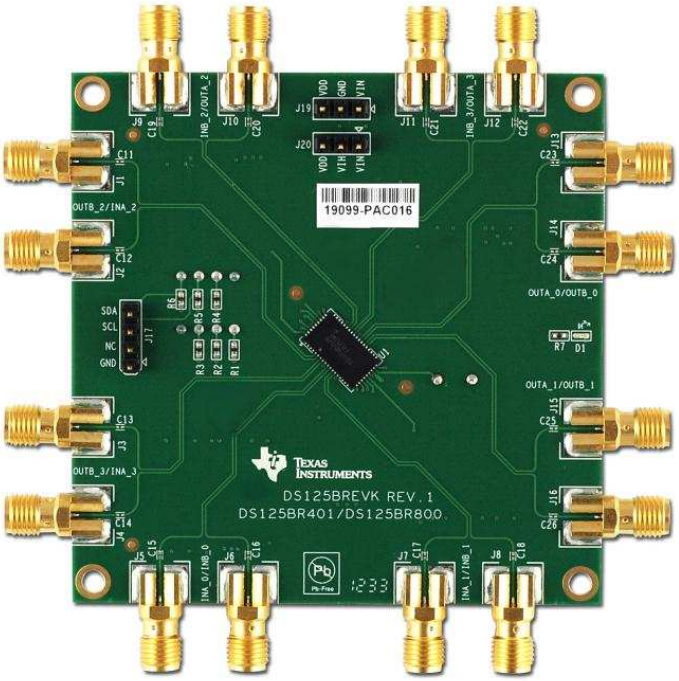

Figure 1. Top Assembly

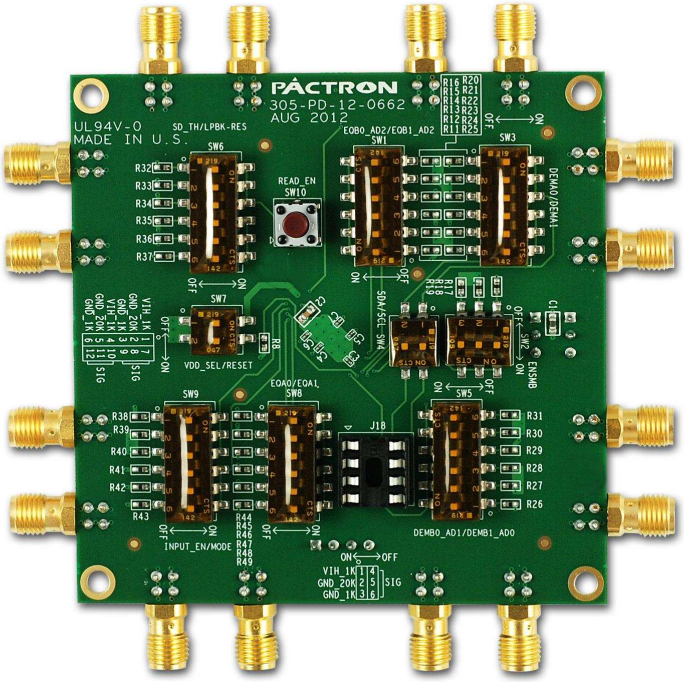

Figure 2. Bottom Assembly

2 4-Level IO Control

Many of the control pins on the DS125BR401A have more than two valid levels. Table 1 shows how to access each of these levels with the switch banks on the back side of the EVM.

Table 1. Switches to set the 4-Level input control pins

4-Level Input Settings	Setting for 3 pin switches (3-2-1)
0 - Tie 1 kΩ to GND	**ON** - OFF - OFF
R - Tie 20 kΩ to GND	OFF - **ON** - OFF
F - FLOAT (open)	OFF - OFF - OFF
1 - Tie 1 kΩ to VIH	OFF - OFF - **ON**

The following switches are used to set the input condition for the 4-level inputs:

- **SW1, SW2, SW3, SW5, SW6, SW8, SW9**

There are 3 switches connected to an input signal pin. Each switch when set to the ON position sets the pin to one of the 4-level setting. The 6 pin switches are assigned similar to the 3 pin switches. The only difference is 2 signal pins are connected and thus 6-5-4 is for the one signal pin and 3-2-1 is for another signal pin.

NOTE: Only 1 switch at the ON position is allowed. Activating more than one switch concurrently results in an indeterminate voltage level.

3 Switch Connection Overview

Table 2. Connection and Control Description

Component	Name	Function
J1 to J8	IN_B2+, IN_B2-, IN_B3+, IN_B3-, IN_A0+, IN_A0-, IN_A1+, IN_A1-	High-speed differential inputs
J9 to J16	OUT_B2+, OUT_B2-, OUT_B3+, OUT_B3-, OUT_A0+, OUT_A0-, OUT_A1+, OUT_A1-	High-speed differential outputs
J19	VIN or VDD	DC Power - VIN or VDD to DS125BR401A
J20	VIN or VDD	Jumper – VIN or VDD to VIH power
J17	SDA, SCL	Optional SMBUS access pins. See the datasheet for additional information on SMBUS.
J18	EEPROM	Optional socket for EEPROM
SW1	EQB[1:0] or AD[3:2]	PIN MODE – EQ control for channel B inputs SMBUS MODE – AD[3:2] device address bits
SW2	ENSMB	ENSMB = LOW – PIN MODE ENSMB = HIGH – SMBUS (slave mode) ENSMB = FLOAT – SMBUS (master mode – load configuration from EEPROM)
SW3	DEMA[1:0]	PIN MODE – Output control for channel A outputs
SW4	SDA/SCL	“ON” position connects SDA and SCL lines to the device pin.
SW5	DEMB[1:0] or AD[1:0]	PIN MODE – DE control for channel B outputs SMBUS MODE – AD[1:0] device address bits
SW6	SD_TH and LPBK-RES	SD_TH – Signal detect threshold level for Channel B[3:0] (FLOAT = Default level) LPBK-RES is defined as RES on the BR401A, this pin must stay floating for BR401A (FLOAT = Normal operation)
SW7	VDD_SEL and RESET	VDD_SEL – Enable or disable the internal 3.3V to 2.5V regulator. RESET: PWDN Terminal - Enable or disable the device (LOW – enable)
SW8	EQA[1:0]	PIN MODE – EQ control for channel A inputs
SW9	INPUT_EN and MODE	INPUT_EN – Enable or disable the internal 50 ohm to VDD terminations MODE: MODE_B terminal Tie 1 kΩ to GND = GEN 1,2 and SAS 1,2 Float = Auto Mode Select (for PCIe) Tie 20 kΩ to GND = SAS-3 and GEN-3 without De-emphasis Tie 1 kΩ to VDD = SAS-3 and GEN-3 with De-emphasis
SW10	READ_EN	ENSMB = FLOAT – SMBUS (master mode – load configuration from EEPROM) SW6: SD_TH becomes the READ_EN pin. To start the loading at power up, set SW6 pin 3 to “ON” position (pull to GND). To manually control the start, set SW6 pin 1 to “ON” position (pull to VDD) and push the SW10 button for the high to low transition to start the loading. When the loading is complete the LED – D1 light should turn OFF.

4 Quick Start Guide

1. **Connect J19: VIN = 3.3V or VDD = 2.5V and GND.**
   - **For VIN = 3.3V:**
     Set SW7 pin1 (VDD_SEL) to the ON position (enable internal LDO regulator) and float VDD at J19.
   - **For VIN = 2.5V:**
     Set SW7 pin1 (VDD_SEL) to the OFF positions (disable internal LDO regulator) and float VIN at J19.
2. **Set jumper – J20 for VIH connection to VIN or VDD.**
3. **Connect 50 Ohm SMA cables to the board.**
   - The input signals J5 to J12 can be connected from a pattern generator. Set SW7 pin1 (VDD_SEL) to the ON position (enable internal LDO regulator) and float VDD at J19.
   - The output signals J1 to J4 and J13 to J16 can be connected to a scope.

Table 3. SMA Channel Connections

A/B Channels	Input Channel	Output Channel
B-Channels	J1 – OUT_B2+, J2 – OUT_B2-	J9 – IN_B2+, J10 – IN_B2-
	J3 – OUT_B3+, J4 – OUT_B3-	J11 – IN_B3+, J12 – IN_B3-
A-Channels	J5 – IN_A0+, J6 – IN_A0-	J13 – OUT_A0+, J14 – OUT_A0-
	J7 – IN_A1+, J8 – IN_A1-	J15 – OUT_A1+, J16 – OUT_A1-

4. **Set the control pins for normal operation**
   - SW7 – RESET = 0 (enables the device): set switch pin2 to the ON position.
   - SW9 – INPUT_EN = 1 (50 ohm input termination): set switches (3-2-1) = (OFF-OFF-**ON**).
   - SW9 – MODE = VDD (enables SAS-3 / PCIe GEN3 mode): set switches (6-5-4) = (OFF-OFF-**ON**).
   - SW6 – SD_TH = F (default signal detect threshold level): set switches (3-2-1) = (OFF-OFF-OFF).
   - SW6 – LPBK - RES = F (normal operation): set switches (6-5-4) = (OFF-OFF-OFF).

5. **Set the input equalization level.**
   - **For external pin mode control of the equalization level:**
   - Set ENSMB = 0 (1 kΩ to GND) by using the SW2 (3-2-1) = (**ON**-OFF-OFF).
   - SW4 pin1,2 must be set to the OFF positions, so the SMBUS signals are disconnected.
   - Refer to Table 1 for information on the 3 switch settings for the 4 level input.

   Example:
   - Set EQB[1:0] with SW1 for the B bank of inputs (top 4 inputs of DS125BR401A).
   - SW1 (6-5-4), (3-2-1) = (**ON**-OFF-OFF), (**ON**-OFF-OFF) = EQB[1:0] = 0,0 (Level 1).
   - Set EQA[1:0] with SW8 for the A bank of inputs (bottom 4 inputs of DS125BR401A).
   - SW8 (6-5-4), (3-2-1) = (**ON**-OFF-OFF), (OFF-OFF-**ON**) = EQA[1:0] = 0,1 (Level 3).

Table 4. EQB Settings available with PIN MODE

Level	EQB[1:0]	SW1 - EQB[1:0]						EQ (dB) @ 6 GHz
		6	5	4	3	2	1	
1	0, 0	**ON**	OFF	OFF	**ON**	OFF	OFF	3.1
2	0, R	**ON**	OFF	OFF	OFF	**ON**	OFF	6.7
3	0, F	**ON**	OFF	OFF	OFF	OFF	OFF	8.4
4	0, 1	**ON**	OFF	OFF	OFF	OFF	**ON**	9.1
5	R, 0	OFF	**ON**	OFF	**ON**	OFF	OFF	13.7
6	R, R	OFF	**ON**	OFF	OFF	**ON**	OFF	16.2
7	R, F	OFF	**ON**	OFF	OFF	OFF	OFF	15.9
8	R, 1	OFF	**ON**	OFF	OFF	OFF	**ON**	17.0
9	F, 0	OFF	OFF	OFF	**ON**	OFF	OFF	20.7
10	F, R	OFF	OFF	OFF	OFF	**ON**	OFF	21.8
11	F, F	OFF	OFF	OFF	OFF	OFF	OFF	23.6
12	F, 1	OFF	OFF	OFF	OFF	OFF	**ON**	24.7
13	1, 0	OFF	OFF	**ON**	**ON**	OFF	OFF	28.0
14	1, R	OFF	OFF	**ON**	OFF	**ON**	OFF	29.2
15	1, F	OFF	OFF	**ON**	OFF	OFF	OFF	30.9
16	1, 1	OFF	OFF	**ON**	OFF	OFF	**ON**	31.9

Table 5. EQA Settings available with PIN MODE

Level	EQA[1:0]	SW8 - EQA[1:0]						EQ (dB) @ 6 GHz
		6	5	4	3	2	1	
1	0, 0	**ON**	OFF	OFF	**ON**	OFF	OFF	3.1
2	0, R	**ON**	OFF	OFF	OFF	**ON**	OFF	6.7
3	0, F	**ON**	OFF	OFF	OFF	OFF	OFF	8.4
4	0, 1	**ON**	OFF	OFF	OFF	OFF	**ON**	9.1

6. **Set the output VOD and De-emphasis level.**
   - **For external pin mode control for the VOD and De-emphasis level:**
   - Set ENSMB = 0 (1 kΩ to GND) by using the SW2 (3-2-1) = (**ON**-OFF-OFF).
   - SW4 pin1,2 must be set to the OFF positions, so the SMBUS signals are disconnected.
   - Refer to Table 1 for information on the 3 switch settings for the 4 level input.

   Example:
   - Set DEMB[1:0] with SW5 for the B bank of outputs (top 4 outputs of DS125BR401A).
   - SW5 (6-5-4), (3-2-1) = (**ON**-OFF-OFF), (OFF-OFF-**ON**) = DEMB[1:0] = 0,1 (VOD=1.0V, DE=0 dB).
   - Set DEMA[1:0] with SW3 for the A bank of outputs (bottom 4 outputs of DS125BR401A).
   - SW3 (6-5-4), (3-2-1) = (OFF-OFF-**ON**), (**ON**-OFF-OFF) = DEMA1:0] = 0,1 (VOD=1.3V, DE=0 dB).

Table 6. Channel B Output Settings available in PIN MODE

Level	DEMB[1:0]	SW5 - DEMB[1:0]						GEN1 and GEN2	
		6	5	4	3	2	1	Inner Amplitude (V_{PP})	DE (dB)
1	0, 0	**ON**	OFF	OFF	**ON**	OFF	OFF	0.8	0
2	0, R	**ON**	OFF	OFF	OFF	**ON**	OFF	0.9	0
3	0, F	**ON**	OFF	OFF	OFF	OFF	OFF	0.6	-3.5
4	0, 1	**ON**	OFF	OFF	OFF	OFF	**ON**	1.0	0
5	R, 0	OFF	**ON**	OFF	**ON**	OFF	OFF	0.7	-3.5
6	R, R	OFF	**ON**	OFF	OFF	**ON**	OFF	0.5	-6
7	R, F	OFF	**ON**	OFF	OFF	OFF	OFF	1.1	0
8	R, 1	OFF	**ON**	OFF	OFF	OFF	**ON**	0.7	-3.5
9	F, 0	OFF	OFF	OFF	**ON**	OFF	OFF	0.6	-6
10	F, R	OFF	OFF	OFF	OFF	**ON**	OFF	1.2	0
11	F, F	OFF	OFF	OFF	OFF	OFF	OFF	0.8	-3.5
12	F, 1	OFF	OFF	OFF	OFF	OFF	**ON**	0.6	-6
13	1, 0	OFF	OFF	**ON**	**ON**	OFF	OFF	1.3	0
14	1, R	OFF	OFF	**ON**	OFF	**ON**	OFF	0.9	-3.5
15	1, F	OFF	OFF	**ON**	OFF	OFF	OFF	0.7	-6
16	1, 1	OFF	OFF	**ON**	OFF	OFF	**ON**	0.5	-9

NOTE: The De-Emphasis levels are also available in SAS-3 / GEN-3 mode when MODE = 1

Table 7. Channel A Output Settings available in PIN MODE

Level	DEMA[1:0]	SW3 - DEMA[1:0]						Input (V_{PP})	Output (V_{PP})
		6	5	4	3	2	1		
1	0, 0	**ON**	OFF	OFF	**ON**	OFF	OFF	1.0	0.70
2	0, R	**ON**	OFF	OFF	OFF	**ON**	OFF	1.0	0.78
4	0, 1	**ON**	OFF	OFF	OFF	OFF	**ON**	1.0	0.83
7	R, F	OFF	**ON**	OFF	OFF	OFF	OFF	1.0	0.88
10	F, R	OFF	OFF	OFF	OFF	**ON**	OFF	1.0	0.91
13	1, 0	OFF	OFF	**ON**	**ON**	OFF	OFF	1.0	1.00

NOTE: Channel A is designed to be linear, ideal for small to moderate levels of input attenuation or when Tx FIR transparency is critical to system operation

5 SMBus Slave Mode of the EQ, VOD, and De-Emphasis level:

- Set ENSMB = 1 (1 kΩ to VIH) by using the SW2 (3-2-1) = (OFF-OFF-**ON**).
- Set SW4 pin1,2 to the ON position so the SMBUS signals are connected.
- Set SW3 pin1 thru pin6 switches to the OFF position so they do not connect to the SDA and SCL line.
- Set the SW1 and SW5 for the AD[3:0] pins. AD[3:0]=0000 sets device slave address = B0'hex.
- Connect SDA, SCL and GND to J17. Please refer to datasheet for register map for EQ, VOD and DEM.

6 Bill of Materials

Bill of Materials

Item	Qty	Reference	Digikey PN	Manufacture PN	Descriptions
1	1	C1	445-3448-1-ND	C1608Y5V0J106Z	CAP CER 10UF 6.3V Y5V 0603
2	1	C2	445-1322-1-ND	C1608X5R0J105K	CAP CER 1.0UF 6.3V X5R 0603
3	5	C3, C4, C5, C6, C7	445-4711-1-ND	C0603X5R0J104M	CAP CER .10UF 6.3V X5R 0201
4	16	C11, C12, C13, C14, C15, C16, C17, C18, C19, C20, C21, C22, C23, C24, C25, C26	587-2483-1-ND	LMK063BJ224MP-F	CAP CER .22UF 10V X5R 0201
5	1	D1	511-1592-1-ND	SML-P12PTT86	LED GRN 0.2MM 13MCD 0402 SMD
6	16	J1, J2, J3, J4, J5, J6, J7, J8, J9, J10, J11, J12, J13, J14, J15, J16	J801-ND	142-0761-881	CONN JACK SMA 50 OHMS PC MOUNT
7	1	J17	WM6504-ND	22-28-4043	CONN HEADER 4POS .100 VERT GOLD
8	2	J19, J20	WM6503-ND	22-28-4033	CONN HEADER 3POS .100 VERT GOLD
9	1	J18	3M5473-ND	4808-3004-CP	SOCKET IC 8-POS .3"
10	31	R1, R2, R3, R4, R8, R11, R13, R14, R16, R17, R19, R20, R22, R23, R25, R26, R28, R29, R31, R32, R34, R35, R37, R38, R40, R41, R43, R44, R46, R47, R49	P1.00KLCT-ND	ERJ-2RKF1001X	RES 1.00K 1/10W 1% 0402
11	1	R7	P220LCT-ND	ERJ-2RKF2200X	RES 220 1/10W 1% 0402
12	13	R12, R15, R18, R21, R24, R27, R30, R33, R36, R39, R42, R45, R48	P20.0KLCT-ND	ERJ-2RKF2002X	RES 20.0K 1/10W 1% 0402
13	2	R5, R6	P4.70KLCT-ND	ERJ-2RKF4701X	RES 4.70K OHM 1/10W 1% 0402 SMD
14	6	SW1, SW3, SW5, SW6, SW8, SW9	CT2196MST-ND	219-6MST	SWITCH TAPE SEAL 6 POS SMD
15	1	SW2	CT2193MST-ND	219-3MST	SWITCH TAPE SEAL 3 POS SMD
16	2	SW4, SW7	CT2192MST-ND	219-2MST	SWITCH TAPE SEAL 2 POS SMD
17	1	SW10	P12225SCT-ND	EVQ-21505R	SWITCH LT 6MM 160GF 5MM HEIGHT
18	1	U1	NA	DS125BR401ANJYT	BUFFER - REPEATER

7 Schematic

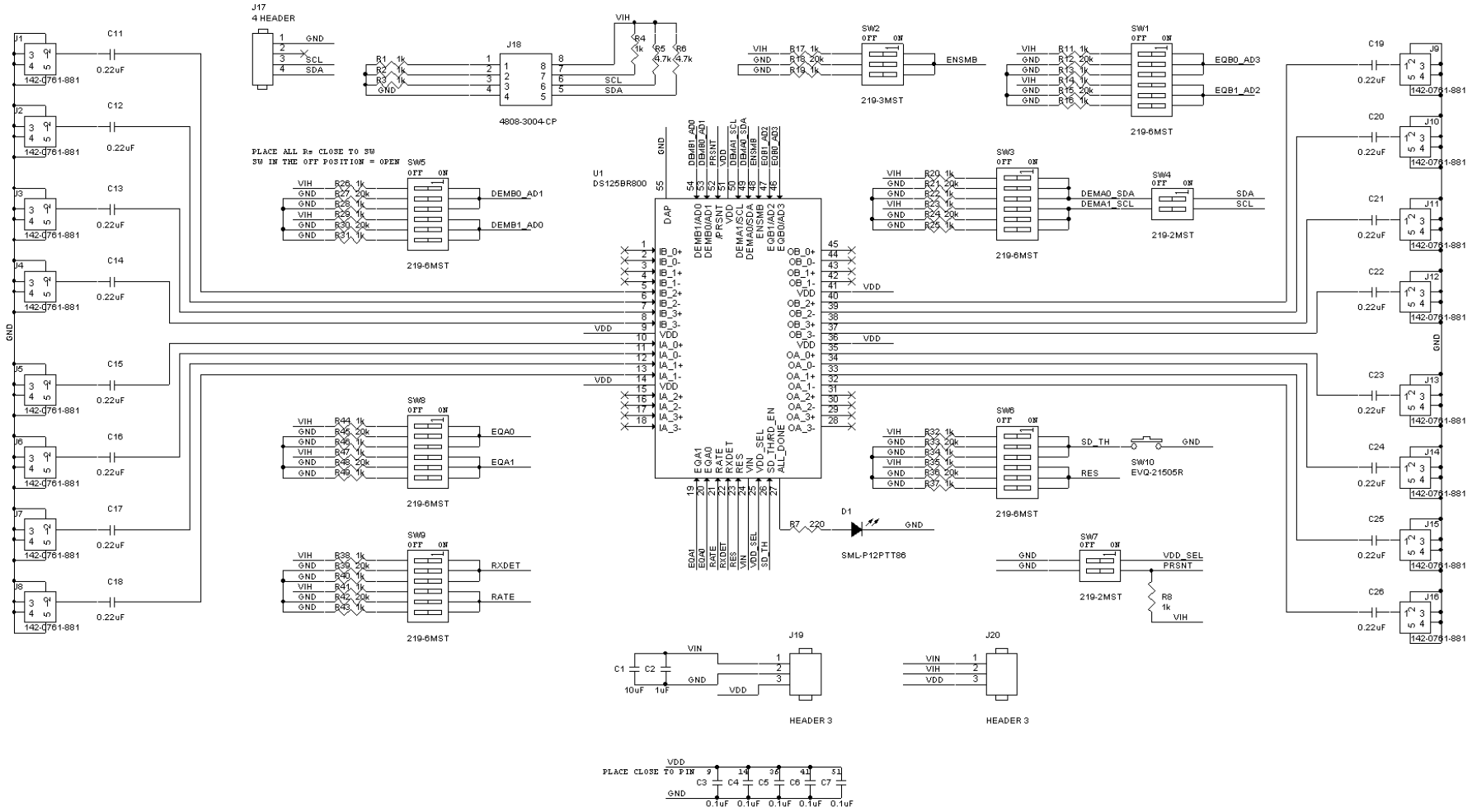

Figure 3. Schematic

8 EVM Layout

The following Figures show the DS125BR401AEVM board layout. The EVM controls signal integrity functions via a combination of switches and jumpers.

The DS125BR401A is very compact and low power. The WQFN package offers an exposed thermal pad to enhance electrical and thermal performance. This must be soldered to the copper landing on the PWB.

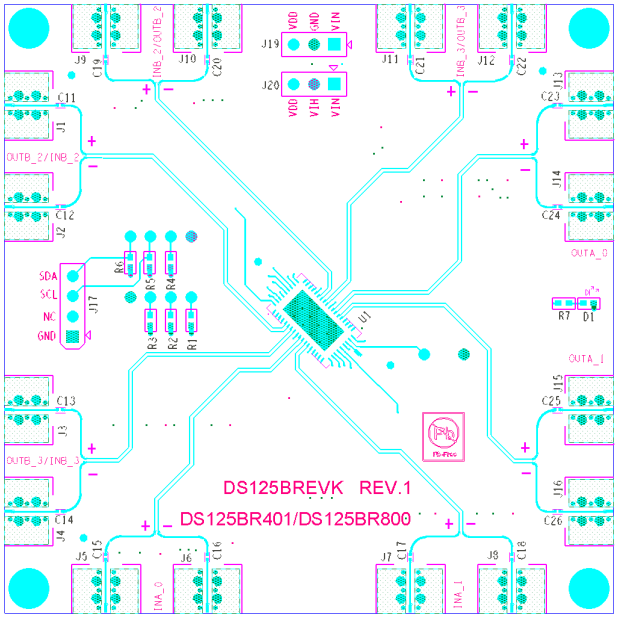

Figure 4. Top Assembly Layer

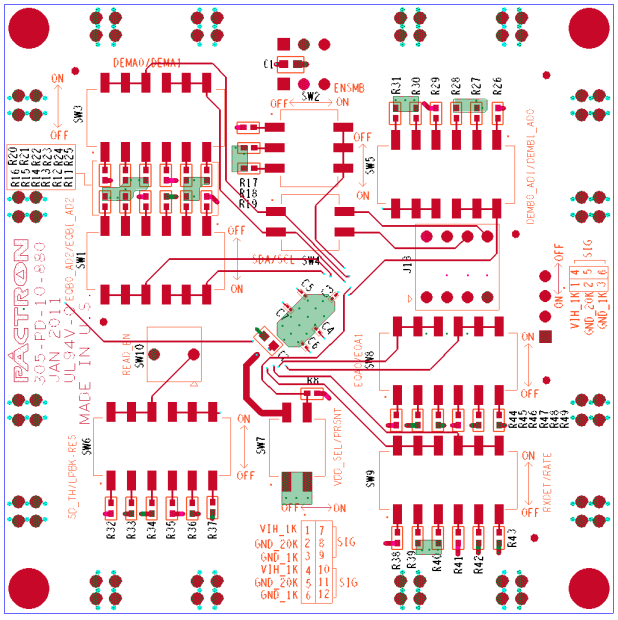

Figure 5. Bottom Assembly Layer

Revision History

Changes from Original (SEPTEMBER 2013) to A Revision	Page
• Changed table	9

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

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