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DATA SHEET
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Linear Regulator – Low Dropout, Very Low I_q, Reset, Reset Delay

350 mA

NCV8675

The NCV8675 is a precision 5.0 V and 3.3 V fixed output, low dropout integrated voltage regulator with an output current capability of 350 mA. Careful management of light load current consumption, combined with a low leakage process, achieve a typical quiescent ground current of 34 μA.

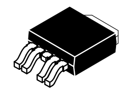
NCV8675 is pin for pin compatible with NCV4275 and it could replace this part when very low quiescent current is required.

The output voltage is accurate within ±2.0% for D^2PAK−5 package and ±2.5% for DPAK−5 package, and maximum dropout voltage is 600 mV at full rated load current.

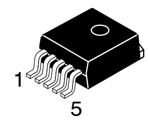
It is internally protected against input transients, input supply reversal, output overcurrent faults, and excess die temperature. No external components are required to enable these features.

Features

- 5 V and 3.3 V Fixed Output (2.5 V Version Available Upon Request)
- ±2.0% or ±2.5% Output Accuracy, Over Full Temperature Range
- 34 μA Typical Quiescent Current at I_{out} = 100 μA, 50 μA Maximum up to 85°C
- 600 mV Maximum Dropout Voltage at 350 mA Load Current
- Wide Input Voltage Operating Range of 4.5 V to 45 V
- Internal Fault Protection
  - −42 V Reverse Voltage
  - Short Circuit/Overcurrent
  - Thermal Overload
- AEC−Q100 Qualified
- EMC Compliant
- NCV Prefix for Automotive and Other Applications Requiring Site and Control Changes
- These are Pb−Free Devices

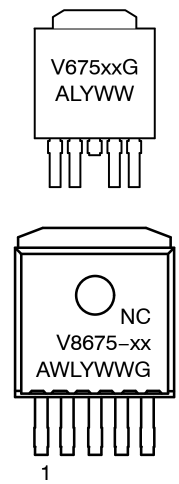


DPAK−5
DT SUFFIX
CASE 175AA



D^2PAK−5
DS SUFFIX
CASE 936A

MARKING DIAGRAMS



Pin 1. V_{in}
2. RO
Tab, 3. GND*
4. D
5. V_{out}

* Tab is connected to Pin 3 on all packages

xx	= 50 (5.0 V Version)
	33 (3.3 V Version)
A	= Assembly Location
WL, L	= Wafer Lot
Y	= Year
WW	= Work Week
G	= Pb−Free Package

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 15 of this data sheet.

NOTE: Some of the devices on this data sheet have been **DISCONTINUED**. Please refer to the table on page 15.

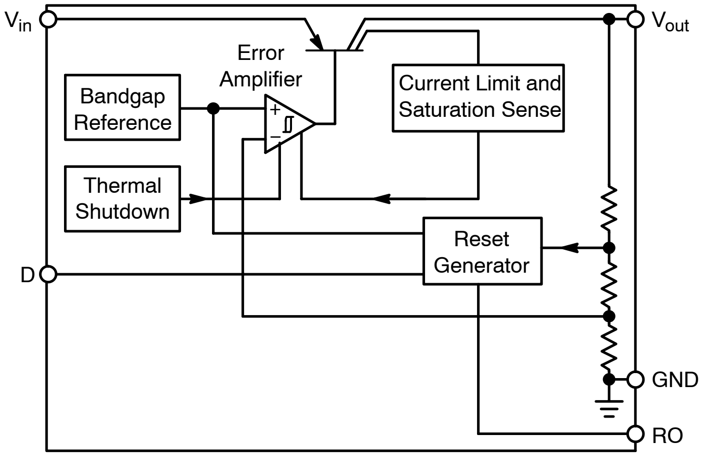


Figure 1. Block Diagram

PIN DESCRIPTIONS

Symbol	Function
V_{in}	Unregulated Input Voltage; 4.5 V to 45 V; Battery Input Voltage. Bypass to GND with a Ceramic Capacitor.
RO	Reset Output; Open Collector Active Reset (Accurate when V_{in} > 1.0 V)
GND	Ground; Pin 3 Internally Connected to Tab
D	Reset Delay; Timing Capacitor to GND for Reset Delay Function
V_{out}	Output; 350 mA. 22 μF, ESR < 9 Ω

MAXIMUM RATINGS

Symbol	Pin Symbol, Parameter	Min	Max	Unit
V_{in}	Input Voltage	−42	45	V
V_{out}	Output Voltage	−0.3	16	V
V_{RO}	Reset Output Voltage	−0.3	25	V
I_{RO}	Reset Output Current	−5.0	5.0	mA
V_D	Reset Delay Voltage	−0.3	7.0	V
I_D	Reset Delay Current	−2.0	2.0	mA
T_{Stg}	Storage Temperature	−55	+150	°C
 – –	ESD Capability −Human Body Model −Machine Model	 4 200		 kV V
T_{Stg}	Storage Temperature	−55	+150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

OPERATING RANGE

Symbol	Pin Symbol, Parameter	Min	Max	Unit
V_{in}	Input Voltage Operating Range	4.5	45	V
T_J	Junction Temperature	−40	150	°C

THERMAL RESISTANCE

Symbol	Parameter		Min	Max	Unit
R_{thja}	Junction Ambient	D^2PAK		82.1	°C/W
R_{thjc}	Junction Case	D^2PAK		4.3	
R_{thja}	Junction Ambient	DPAK		112.2	°C/W
R_{thjc}	Junction Case	DPAK		4.3	

1. 1 oz., 100 mm^2 copper area.

Pb SOLDERING TEMPERATURE AND MSL

Symbol	Parameter	Min	Max	Unit
T_{sld}	Lead Temperature Soldering Reflow (SMD styles only), Pb−Free (Note 2)		 265 pk	°C
MSL	Moisture Sensitivity Level	1		–

2. Pb−Free, 60 sec – 150 sec above 217°C, 40 sec maximum at peak.

ELECTRICAL CHARACTERISTICS V_{in} = 13.5 V, T_J = −40°C to +150°C, unless otherwise specified

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
OUTPUT						
V_{out}	Output Voltage 5.0 V Version D2PAK DPAK	0.1 mA ≤ I_{out} ≤ 350 mA (Note 3) 6.0 V ≤ V_{in} ≤ 16 V	4.900 4.875	5.000 5.000	5.100 5.125	V
V_{out}	Output Voltage 3.3 V Version D2PAK DPAK	0.1 mA ≤ I_{out} ≤ 350 mA (Note 3) 4.5 V ≤ V_{in} ≤ 16 V	3.234 3.217	3.300 3.300	3.366 3.383	V
V_{out}	Output Voltage 5.0 V Version D2PAK DPAK	0.1 mA ≤ I_{out} ≤ 200 mA (Note 3) 6.0 V ≤ V_{in} ≤ 40 V	4.900 4.875	5.000 5.000	5.100 5.125	V
V_{out}	Output Voltage 3.3 V Version D2PAK DPAK	0.1 mA ≤ I_{out} ≤ 200 mA (Note 3) 4.5 V ≤ V_{in} ≤ 40 V	3.234 3.217	3.300 3.300	3.366 3.383	V
ΔV_{out} Versus V_{in}	Line Regulation	I_{out} = 5 mA 6.0 V ≤ V_{in} ≤ 28 V	−25	5	+25	mV
ΔV_{out} Versus. I_{out}	Load Regulation	1.0 mA ≤ I_{out} ≤ 350 mA (Note 3)	−40	5	+40	mV
$V_{in} - V_{out}$	Dropout Voltage 5.0 V Version	I_{out} = 200 mA (Notes 3 and 4) I_{out} = 350 mA (Notes 3 and 4)	– –	215 310	500 600	mV
I_q	Quiescent Current	I_{out} ≤ 100 µA T_J = 25°C T_J = −40°C to +85°C T_J = 125°C		34 34 54	45 50 60	µA
$I_{G (ON)}$	Active Ground Current	I_{out} = 50 mA (Note 3) I_{out} = 350 mA (Note 3)		1.8 20	3.5 40	mA
P_{SRR}	Power Supply Rejection	V_{RIPPLE} = 0.5 V_{PP}, F = 100 Hz		70		%/V
C_{out} ESR C_{out} ESR	Output Capacitor for Stability 5.0 V Version 3.3 V Version	I_{out} = 0.1 mA to 350 mA	22 22 		 9 7	µF Ω µF Ω
RESET TIMING D AND OUTPUT R_O						
V_{out}, r_t	Reset Switching Threshold	5.0 V Version 3.3 V Version	4.50 2.97	4.65 3.069	4.80 3.168	V
V_{ROL}	Reset Output Low Voltage	R_{Ext} > 5.0k, V_{out} > 1.0V	–	0.20	0.40	V
I_{ROH}	Reset Output Leakage Current	V_{ROH} = 5.0 V V_{ROH} = 3.3 V	– –	0 0	10 10	µA
$I_{D,C}$	Reset Charging Current	V_D = 1.0 V	2.0	4.0	6.5	µA
V_{DU}	Upper Timing Threshold	–	1.2	1.3	1.4	V
V_{LU}	Lower Timing Threshold			1.24		V
t_{rd}	Reset Delay Time 5.0 V Version 3.3 V Version	C_D = 47 nF	10 10	16 16	22 24	ms
t_{rr}	Reset Reaction Time	C_D = 47 nF		1.5	4.0	µs
PROTECTION						
$I_{out(LIM)}$	Current Limit	V_{out} = 4.5 V (5.0 V Version) V_{out} = 3.0 V (3.3 V Version)	350 350			mA
$I_{out(SC)}$	Short Circuit Current Limit	V_{out} = 0 V (Note 3)	100	600		mA
T_{TSD}	Thermal Shutdown Threshold	(Note 5)	150		200	°C

3. Use pulse loading to limit power dissipation.
4. Dropout voltage = ($V_{in} - V_{out}$), measured when the output voltage has dropped 100 mV relative to the nominal value obtained with V_{in} = 13.5 V.
5. Not tested in production. Limits are guaranteed by design.

TYPICAL CHARACTERISTIC CURVES – 5 V VERSION

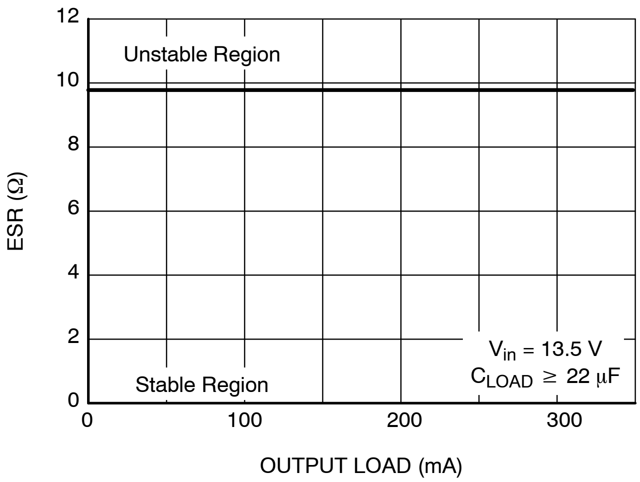


Figure 2. NCV8675 Stability Curve (5 V Version)

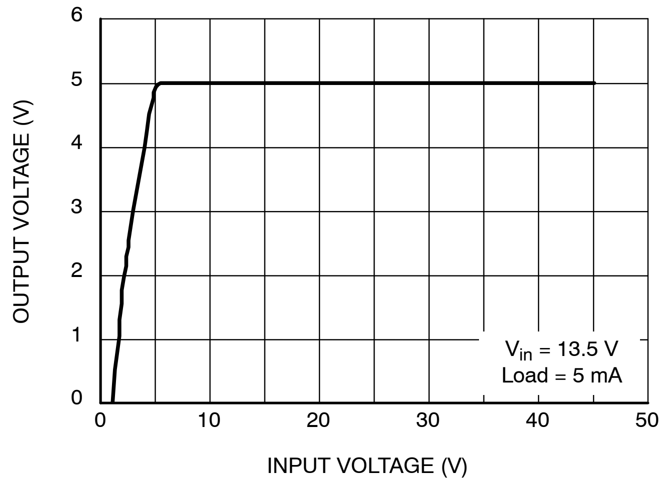


Figure 3. NCV8675 Input Voltage vs. Output Voltage (Full Range) (5 V Version)

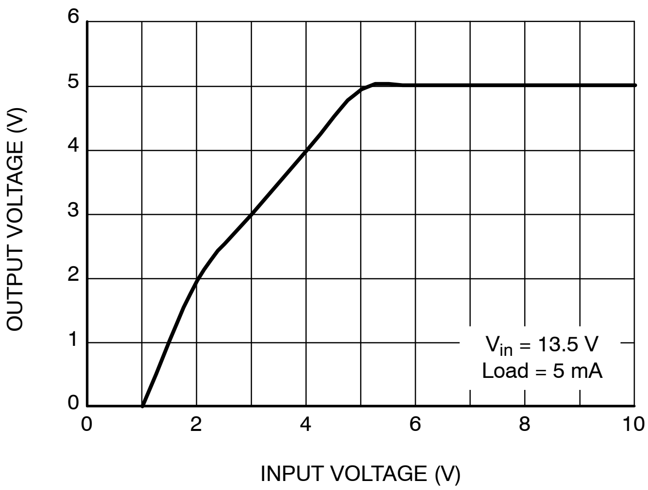


Figure 4. NCV8675 Input Voltage vs. Output Voltage (Low Voltage) (5 V Version)

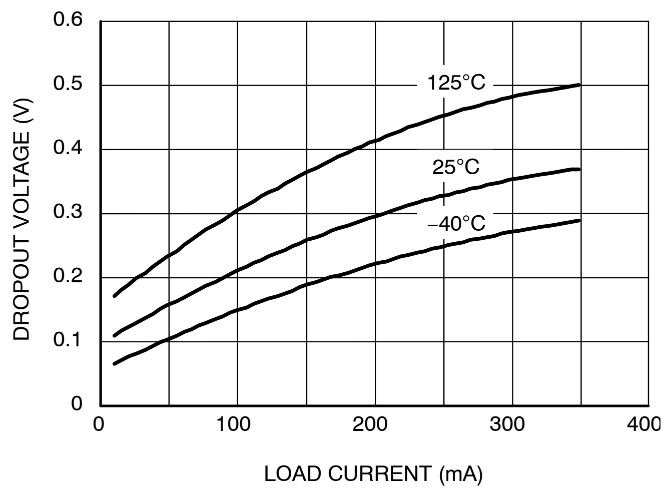


Figure 5. NCV8675 Dropout Voltage vs. Load Current (5 V Version)

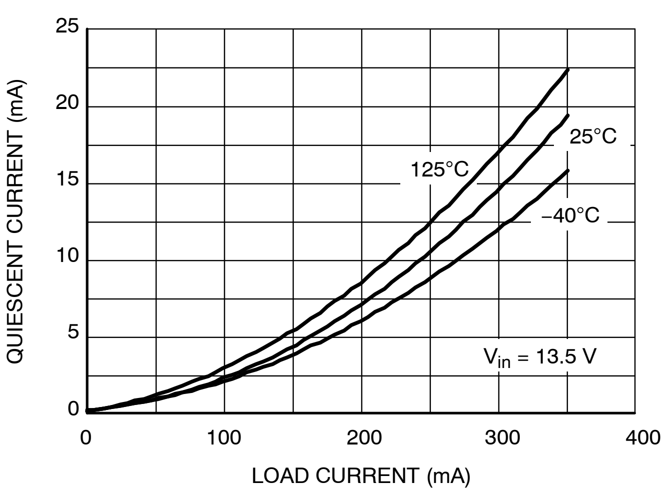


Figure 6. NCV8675 Quiescent Current vs. Load Current (Full Range) (5 V Version)

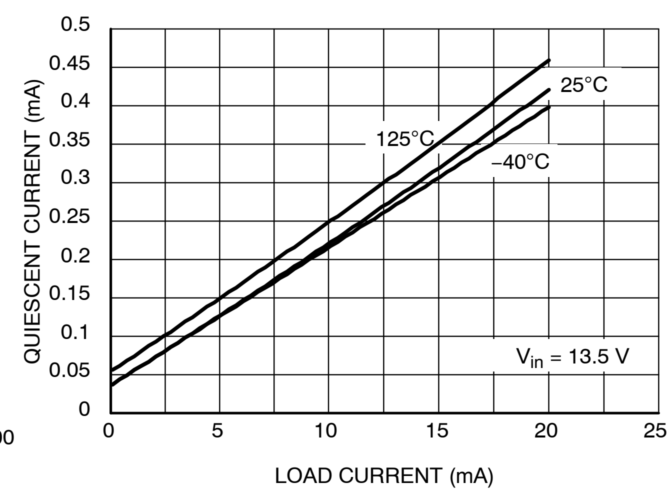


Figure 7. NCV8675 Quiescent Current vs. Load Current (Light Load) (5 V Version)

TYPICAL CHARACTERISTIC CURVES – 5 V VERSION (continued)

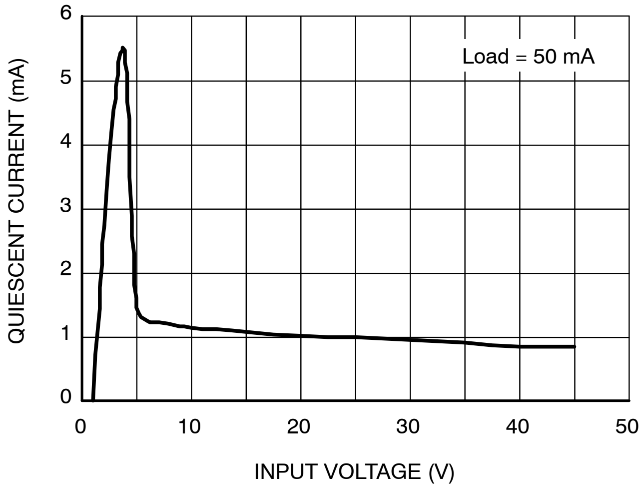


Figure 8. NCV8675 Quiescent Current vs. Input Voltage (5 V Version)

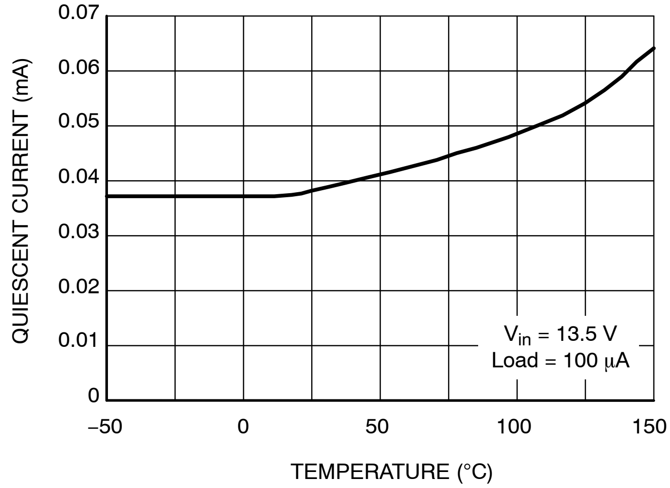


Figure 9. NCV8675 Quiescent Current vs. Temperature (5 V Version)

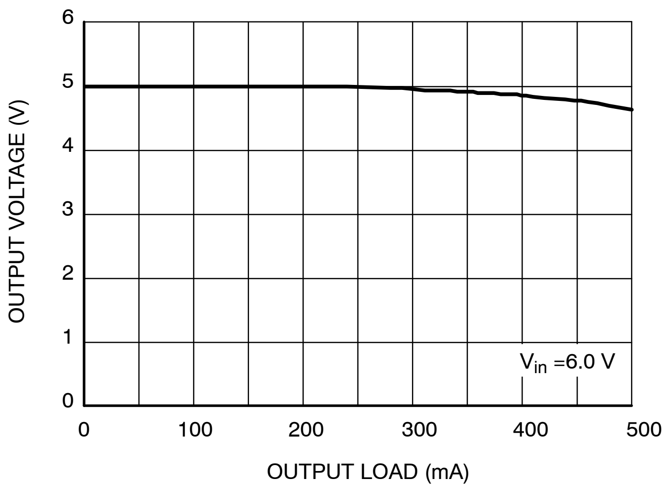


Figure 10. NCV8675 Output Voltage vs. Output Load (5 V Version)

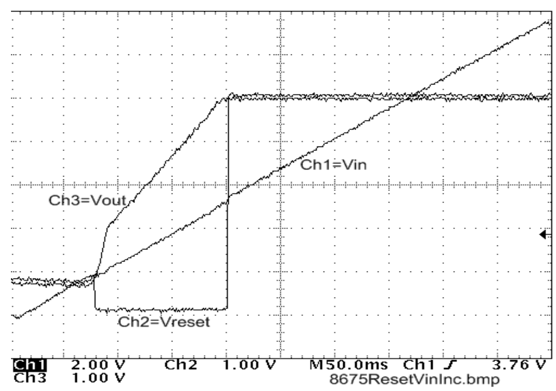


Figure 11. Reset vs. Output Voltage (V_{in} Rising) (5 V Version)

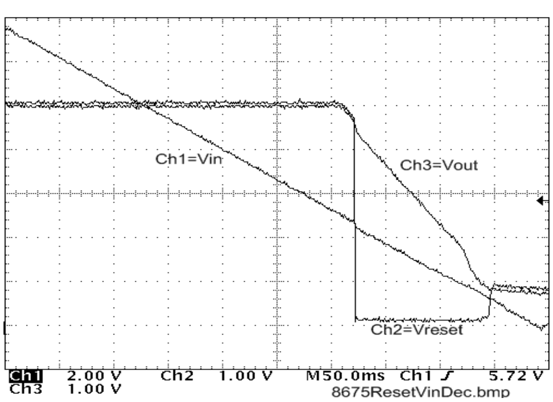


Figure 12. Reset vs. Output Voltage (V_{in} Falling) (5 V Version)

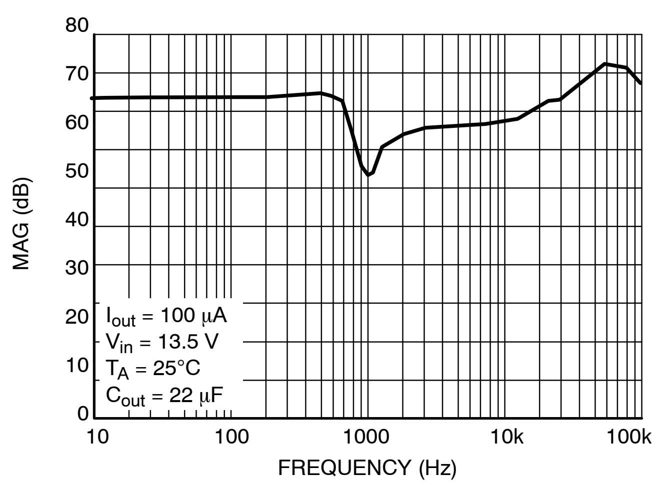


Figure 13. Power Supply Rejection Ratio (5 V Version)

TYPICAL CHARACTERISTIC CURVES – 5 V VERSION (continued)

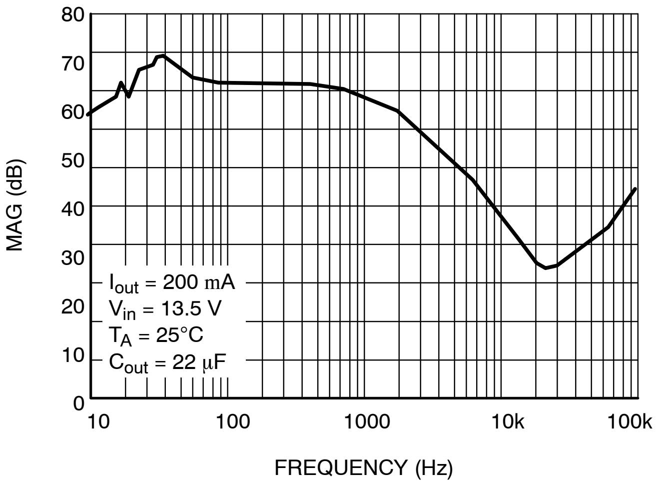


Figure 14. Power Supply Rejection Ratio (5 V Version)

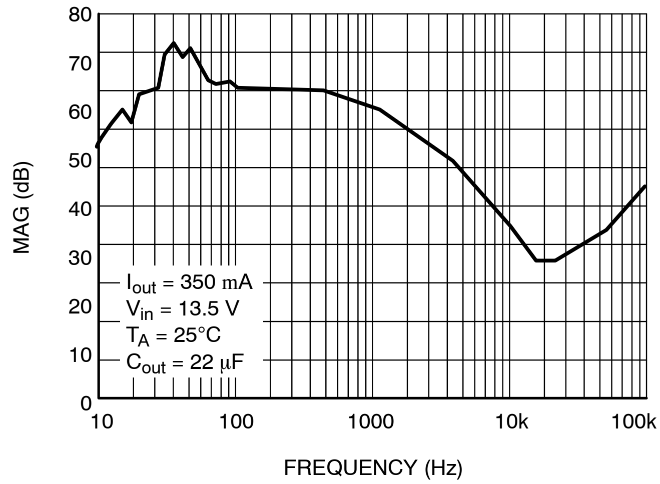


Figure 15. Power Supply Rejection Ratio (5 V Version)

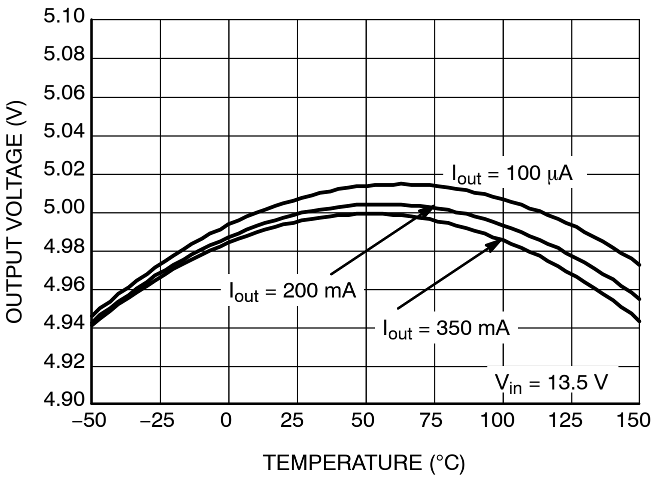


Figure 16. NCV8675 Output Voltage vs. Temperature (5 V Version)

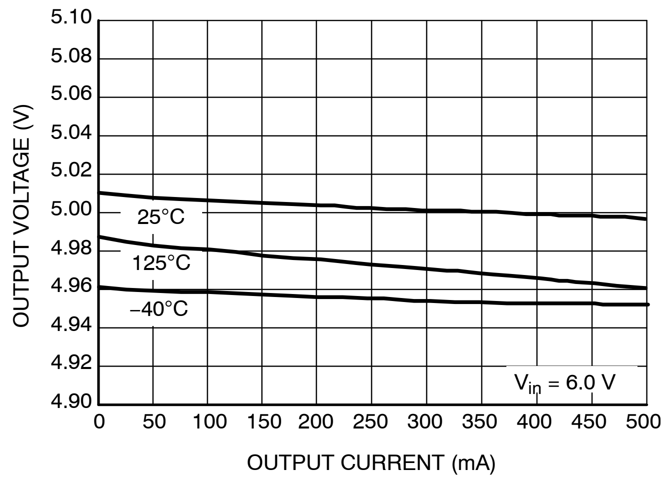


Figure 17. NCV8675 Output Voltage vs. Output Load (5 V Version)

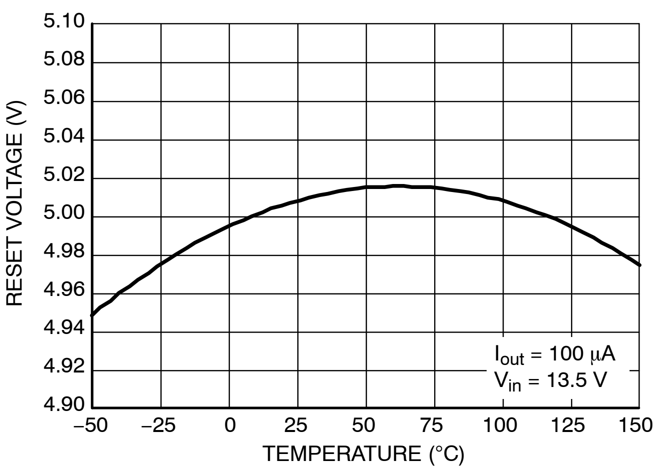


Figure 18. NCV8675 Reset Voltage vs. Temperature (5 V Version)

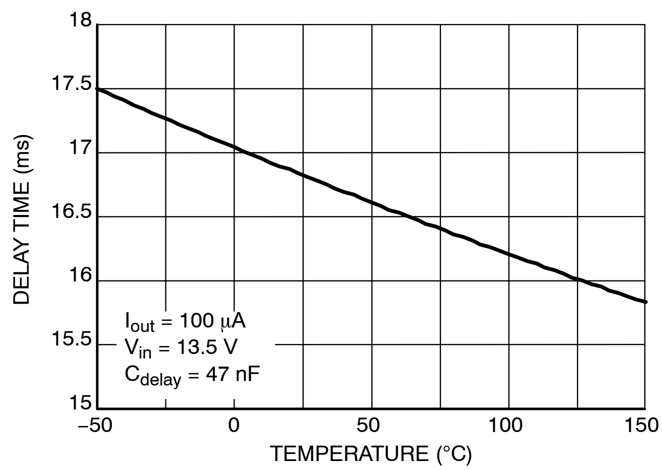


Figure 19. NCV8675 Reset Delay Time vs. Temperature (5 V Version)

TYPICAL CHARACTERISTIC CURVES – 5 V VERSION (continued)

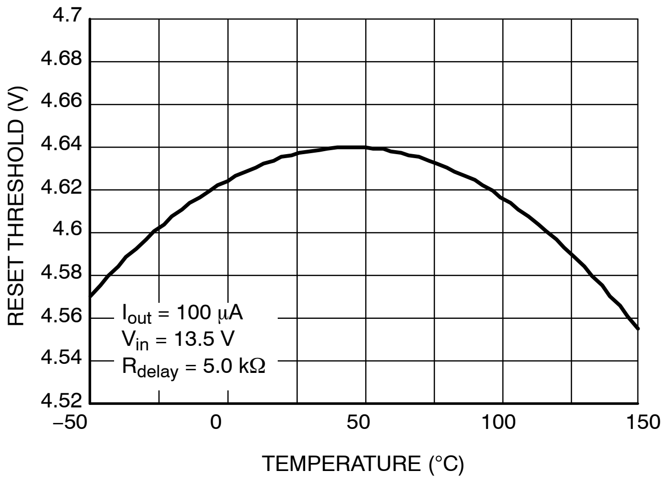


Figure 20. NCV8675 Reset Threshold vs. Temperature (5 V Version)

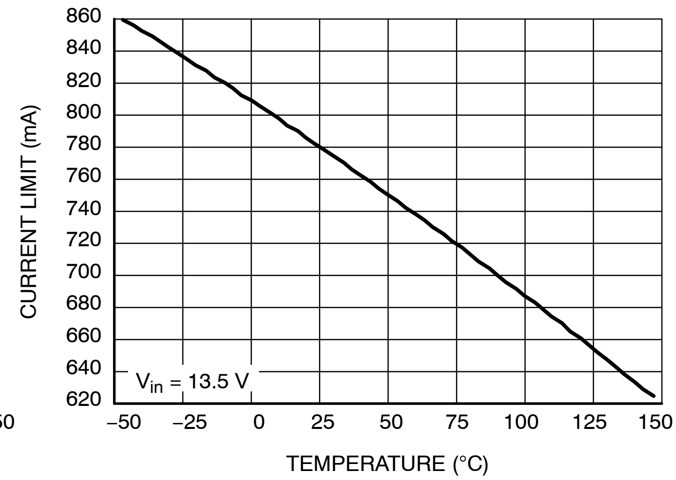


Figure 21. NCV8675 Current Limit Threshold vs. Temperature (5 V Version)

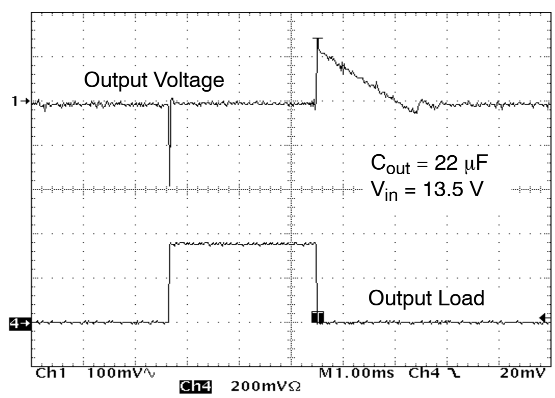


Figure 22. NCV8675 100 μA – 350 mA Load Transient (5 V Version)

TYPICAL CHARACTERISTIC CURVES – 3.3 V VERSION

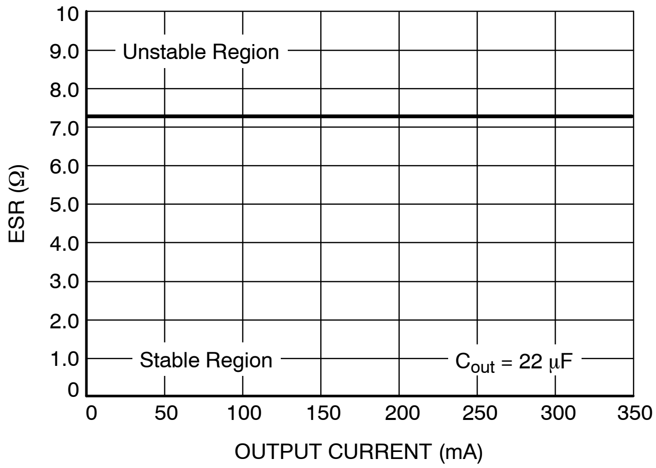


Figure 23. ESR Stability vs. Output Current (3.3 V Version)

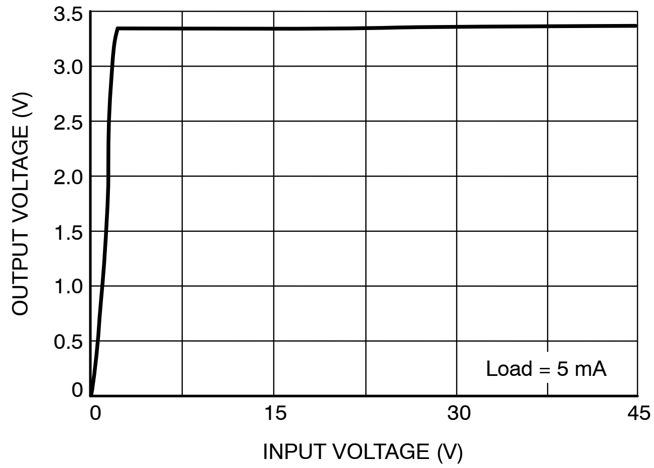


Figure 24. Input Voltage vs. Output Voltage (3.3 V Version)

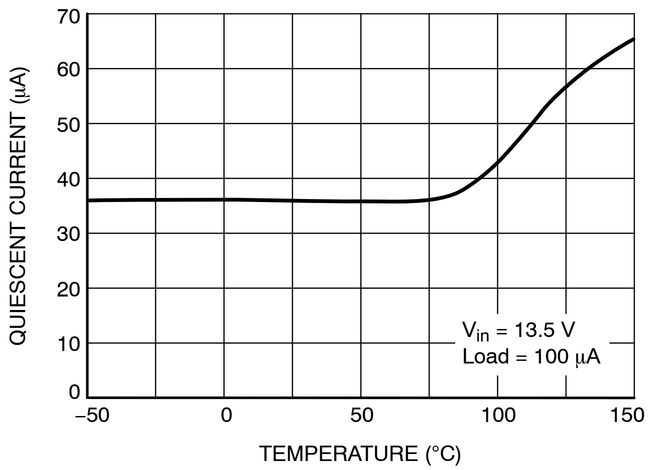


Figure 25. Quiescent Current vs. Temperature (3.3 V Version)

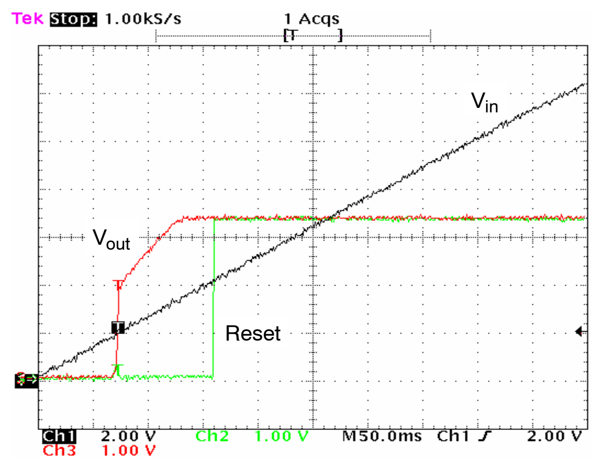


Figure 26. Reset vs. Output Voltage (V_{in} Rising) (3.3 V Version)

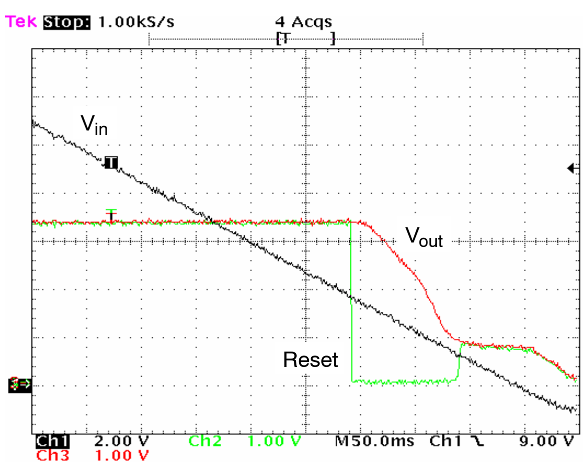


Figure 27. Reset vs. Output Voltage (V_{in} Falling) (3.3 V Version)

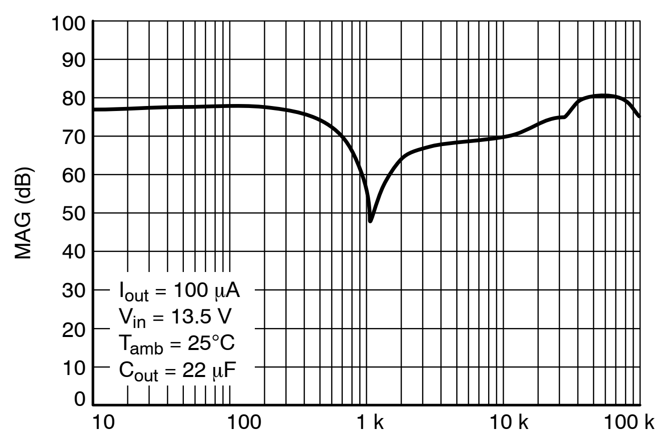


Figure 28. Power Supply Rejection Ratio (3.3 V Version)

TYPICAL CHARACTERISTIC CURVES – 3.3 V VERSION (continued)

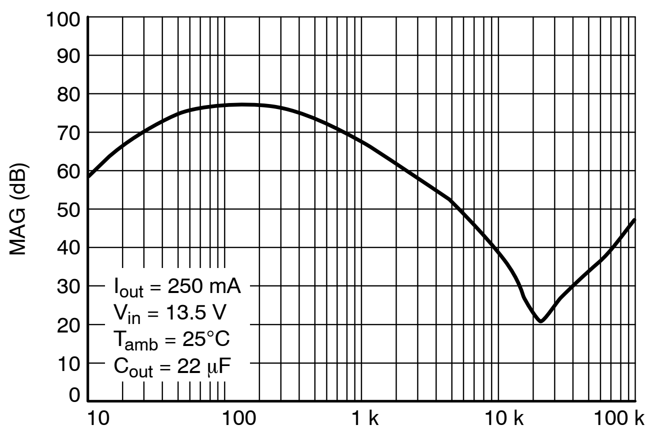


Figure 29. Power Supply Rejection Ratio (3.3 V Version)

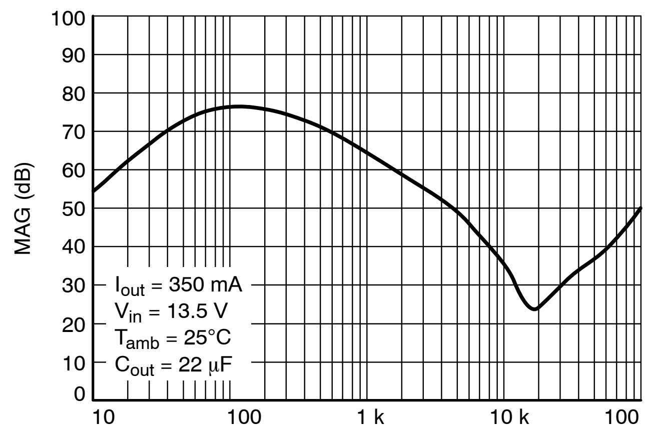


Figure 30. Power Supply Rejection Ratio (3.3 V Version)

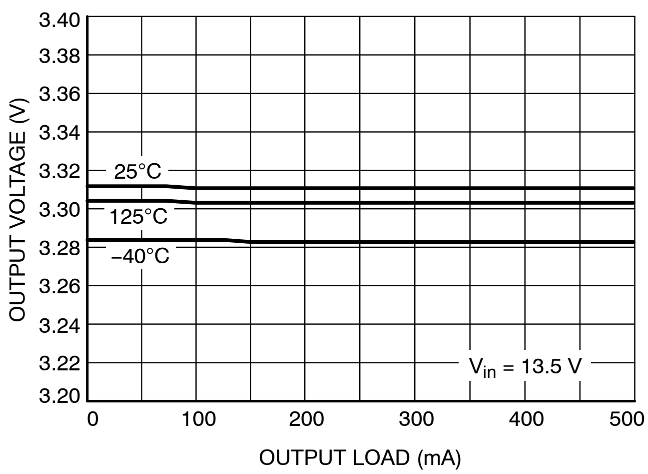


Figure 31. Output Voltage vs. Output Load (3.3 V Version)

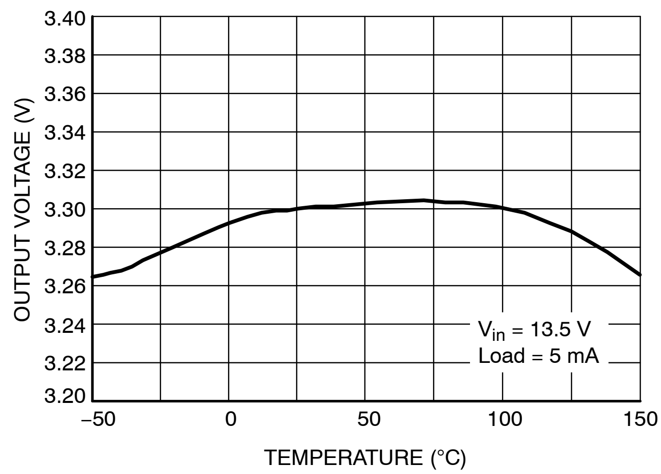


Figure 32. Output Voltage vs. Temperature (3.3 V Version)

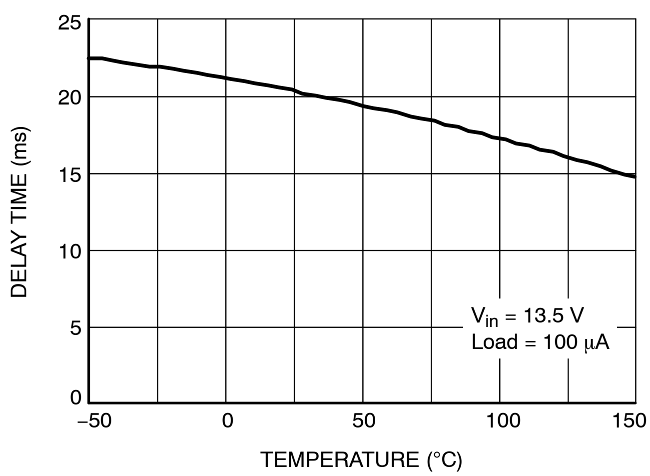


Figure 33. Reset Delay Time vs. Temperature (3.3 V Version)

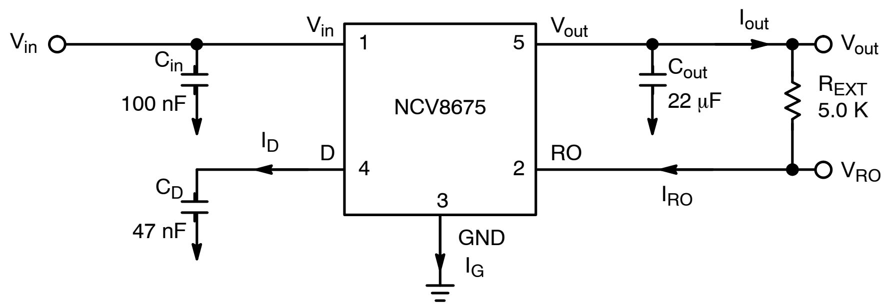


Figure 34. Application Circuits

Circuit Description

The NCV8675 is an integrated low dropout regulator that provides 5.0 V 350 mA, or 3.3 V 350 mA protected output and a signal for power on reset. The regulation is provided by a PNP pass transistor controlled by an error amplifier with a bandgap reference, which gives it the lowest possible drop out voltage and best possible temperature stability. The output current capability is 350 mA, and the base drive quiescent current is controlled to prevent over saturation when the input voltage is low or when the output is overloaded. The regulator is protected by both current limit and thermal shutdown. Thermal shutdown occurs above 150°C to protect the IC during overloads and extreme ambient temperatures. The delay time for the reset output is adjustable by selection of the timing capacitor. See Figure 34, Test Circuit, for circuit element nomenclature illustration.

Regulator

The error amplifier compares the reference voltage to a sample of the output voltage (V_{out}) and drives the base of a PNP series pass transistor by a buffer. The reference is a bandgap design to give it a temperature−stable output. Saturation control of the PNP is a function of the load current and input voltage. Oversaturation of the output power device is prevented, and quiescent current in the ground pin is minimized.

Regulator Stability Considerations

The input capacitor (C_{in}) is necessary to stabilize the input impedance to avoid voltage line influences. The output capacitor helps determine three main characteristics of a linear regulator: startup delay, load transient response and loop stability. The capacitor value and type should be based on cost, availability, size and temperature constraints. Ceramic, tantalum, or electrolytic capacitors of 22 μF, or greater, are stable with very low ESR values. Refer to Figure 2 for specific ESR ratings. The aluminum electrolytic capacitor is the least expensive solution, but, if the circuit operates at low temperatures (−25°C to −40°C), both the capacitance and ESR of the capacitor will vary considerably. The capacitor manufacturer's data sheet usually provides this information. The value for the output capacitor C_{out} shown in Figure 13, Test Circuit, should work for most applications; however, it is not necessarily the optimized solution.

Reset Output

The reset output is used as the power on indicator to the microcontroller. This signal indicates when the output voltage is suitable for reliable operation of the controller. It pulls low when the output is not considered to be ready. RO is pulled up to V_{out} by an external resistor, typically 5.0 kΩ in value. The input and output conditions that control the Reset Output and the relative timing are illustrated in Figure 35, Reset Timing. Output voltage regulation must be maintained for the delay time before the reset output signals a valid condition. The delay for the reset output is defined as the amount of time it takes the timing capacitor on the delay pin to charge from a residual voltage of 0 V to the upper timing threshold voltage V_{DU} of 1.3 V. The charging current for this is I_D of 4 μA and D pin voltage in steady state is typically 2.4 V. By using typical IC parameters with a 47 nF capacitor on the D Pin, the following time delay is derived:

$$t_{RD} = C_D * V_{DU} / I_D$$

$$t_{RD} = 47\ \text{nF} * (1.3\ \text{V}) / 4\ \mu\text{A} = 15.3\ \text{ms}$$

Other time delays can be obtained by changing the C_D capacitor value. The Delay Time can be reduced by decreasing the capacitance of C_D. Using the formula above, Delay can be reduced as desired. Leaving the Delay Pin open is not desirable as it can result in unwanted signals being coupled onto the pin.

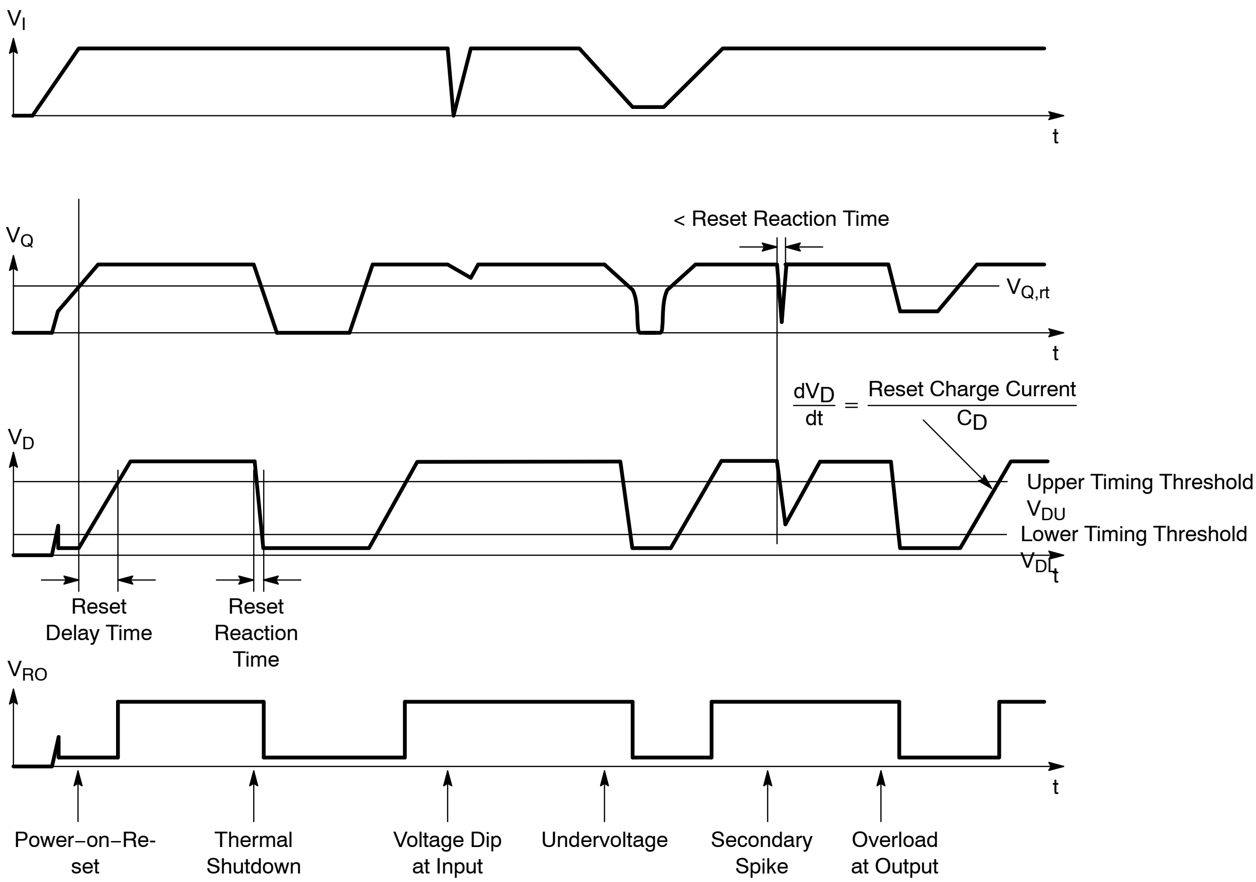


Figure 35. Reset Timing

Calculating Power Dissipation in a Single Output Linear Regulator

The maximum power dissipation for a single output regulator (Figure 36) is:

$$P_{D(max)} = [V_{in(max)} - V_{out(min)}]\, I_{out(max)} + V_{I(max)} I_q \quad (1)$$

where

$V_{in(max)}$ is the maximum input voltage,
$V_{out(min)}$ is the minimum output voltage,
$I_{out(max)}$ is the maximum output current for the application,
I_q is the quiescent current the regulator consumes at $I_{Q(max)}$.

Once the value of $P_{D(max)}$ is known, the maximum permissible value of $R_{\theta JA}$ can be calculated:

$$R_{\theta JA} = \frac{150^\circ C - T_A}{P_D} \quad (2)$$

The value of $R_{\theta JA}$ can then be compared with those in the package section of the data sheet. Those packages with $R_{\theta JA}$'s less than the calculated value in Equation 2 will keep the die temperature below 150°C.

In some cases, none of the packages will be sufficient to dissipate the heat generated by the IC, and an external heatsink will be required.

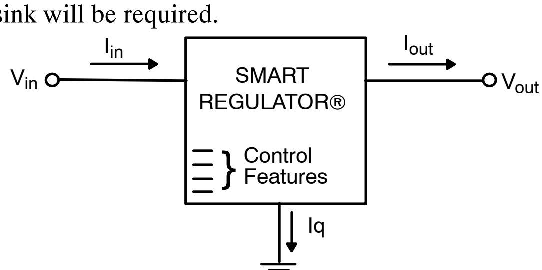


Figure 36. Single Output Regulator with Key Performance Parameters Labeled

Heatsinks

A heatsink effectively increases the surface area of the package to improve the flow of heat away from the IC and into the surrounding air.

Each material in the heat flow path between the IC and the outside environment will have a thermal resistance. Like series electrical resistances, these resistances are summed to determine the value of $R_{\theta JA}$:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CS} + R_{\theta SA} \quad (3)$$

where

$R_{\theta JC}$ is the junction−to−case thermal resistance,
$R_{\theta CS}$ is the case−to−heatsink thermal resistance,
$R_{\theta SA}$ is the heatsink−to−ambient thermal resistance.

$R_{\theta JC}$ appears in the package section of the data sheet. Like $R_{\theta JA}$, it too is a function of package type. $R_{\theta CS}$ and $R_{\theta SA}$ are functions of the package type, heatsink and the interface between them. These values appear in heatsink data sheets of heatsink manufacturers.

Thermal, mounting, and heatsinking considerations are discussed in the **onsemi** application note AN1040/D.

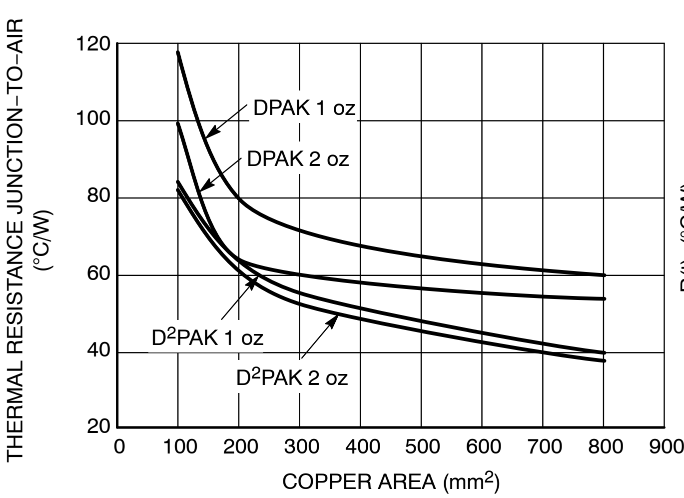


Figure 37. JA vs. Copper Spreader Area

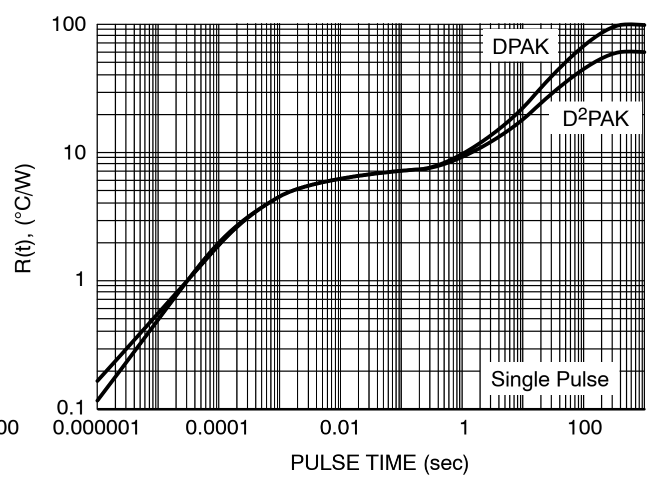


Figure 38. NCV8675 @ PCB Cu Area 100 mm² PCB Cu thk 1 oz

EMC−Characteristics: Conducted Susceptibility

All EMC−Characteristics are based on limited samples and no part of production test according to 47A/658/CD IEC62132−4 (direct Power Injection).

Test Conditions

Supply Voltage V_{in} = 12 V
Temperature T_A = 23°C + −5°C
Load R_L = 100 Ω

Direct power Injection
33d Bm (Note 1) forward power CW for global pin (Note 2)
17 dBm (Note 1) forward power CW for local pin (Note 3)

Acceptance Criteria
Amplitude Dev. max 4% of Output Voltage
Reset outputs remain in correct state + −1 V

1. dBm means dB milli−Watts, $P_{(dBm)}$ = 10 log ($P_{(mW)}$)
2. A global pin carries a signal or power which enters or leaves the application board
3. A local pin carries a signal or power which does not leave the application board. It remains on the application board as a signal between two components

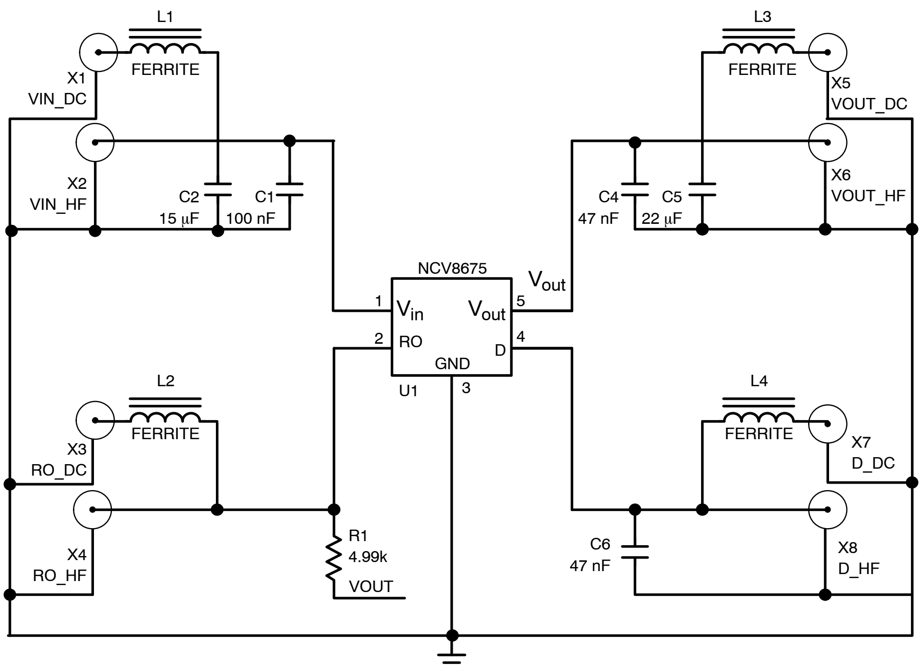


Figure 39. Test Circuit

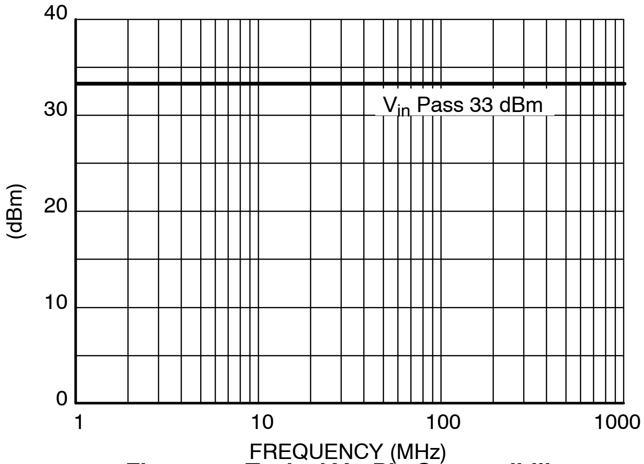


Figure 40. Typical V_{in} Pin Susceptibility

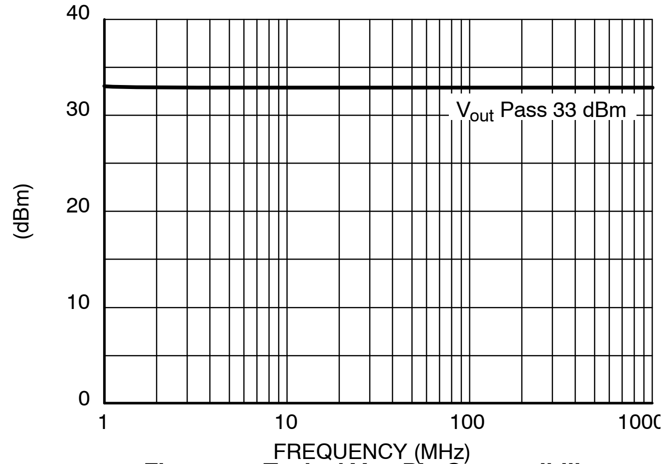


Figure 41. Typical V_{out} Pin Susceptibility

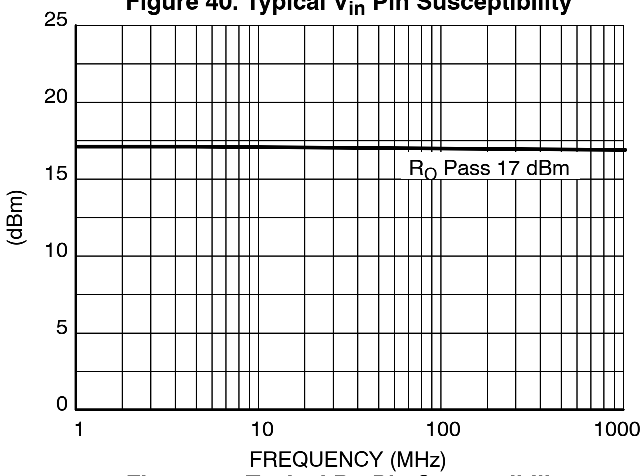


Figure 42. Typical R_O Pin Susceptibility

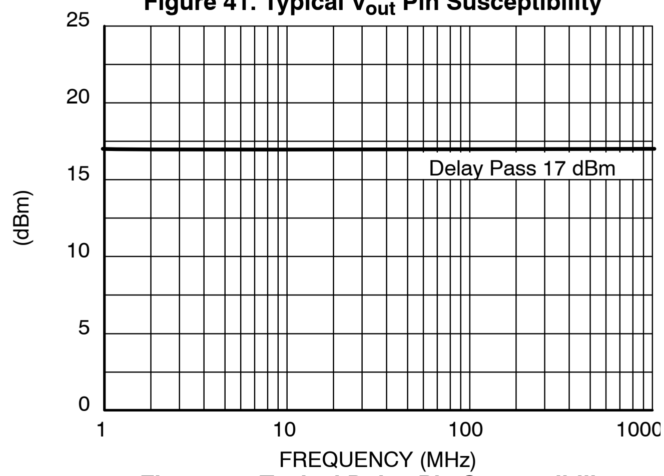


Figure 43. Typical Delay Pin Susceptibility

ORDERING INFORMATION

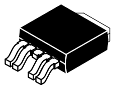
Device	Output Voltage	Package	Shipping†
NCV8675DT50RKG	5.0 V	DPAK (Pb−Free)	2,500 / Tape & Reel

DISCONTINUED (Note 6)

NCV8675DS50G	5.0 V	D^2PAK (Pb−Free)	50 Units / Rail
NCV8675DS50R4G			800 / Tape & Reel
NCV8675DS33G	3.3 V	D^2PAK (Pb−Free)	50 Units / Rail
NCV8675DS33R4G			800 / Tape & Reel
NCV8675DT33RKG		DPAK (Pb−Free)	2,500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

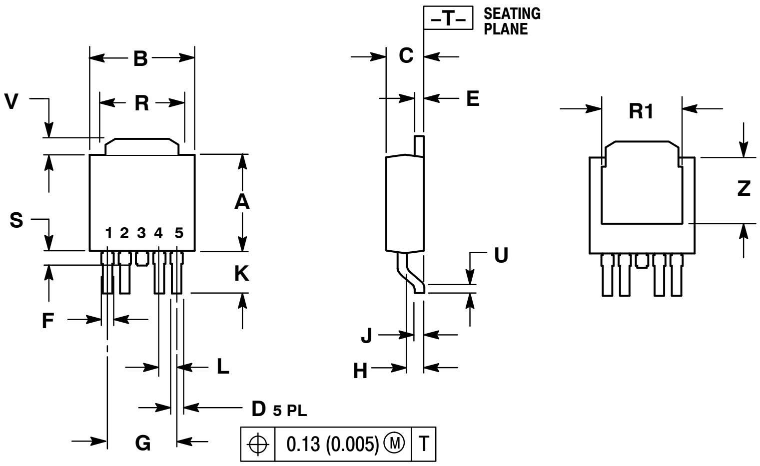
6. **DISCONTINUED:** These devices are not recommended for new design. Please contact your **onsemi** representative for information. The most current information on these devices may be available on www.onsemi.com.



SCALE 1:1

DPAK−5, CENTER LEAD CROP
CASE 175AA
ISSUE B

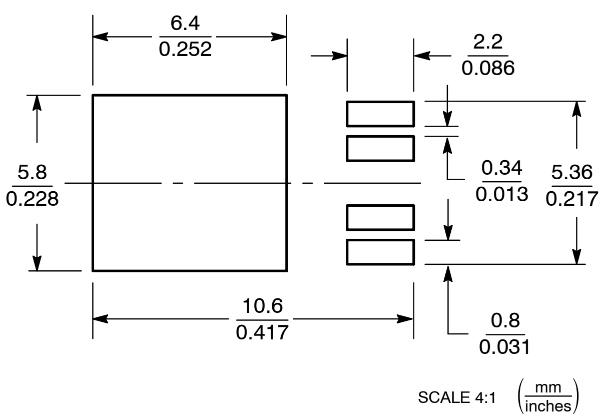
DATE 15 MAY 2014



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

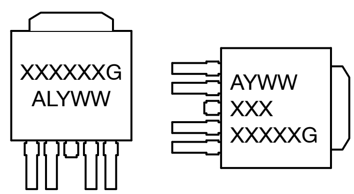
	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.235	0.245	5.97	6.22
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.020	0.028	0.51	0.71
E	0.018	0.023	0.46	0.58
F	0.024	0.032	0.61	0.81
G	0.180 BSC		4.56 BSC	
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.102	0.114	2.60	2.89
L	0.045 BSC		1.14 BSC	
R	0.170	0.190	4.32	4.83
R1	0.185	0.210	4.70	5.33
S	0.025	0.040	0.63	1.01
U	0.020	---	0.51	---
V	0.035	0.050	0.89	1.27
Z	0.155	0.170	3.93	4.32

RECOMMENDED SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAMS*



IC **Discrete**

XXXXXX = Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot " ▪", may or may not be present.

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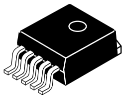
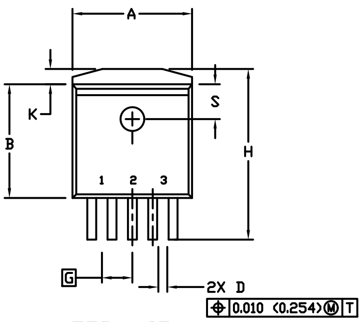


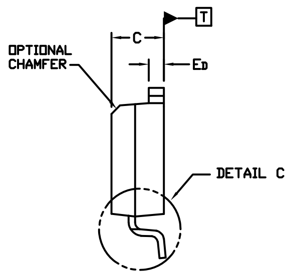
SCALE 1:1

D²PAK 5−LEAD
CASE 936A−02
ISSUE E

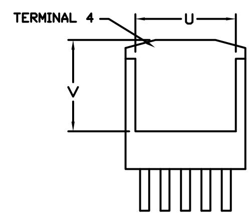
DATE 28 JUL 2021



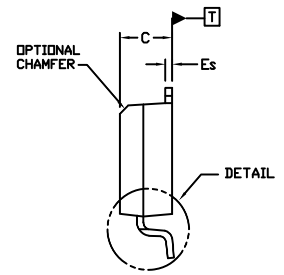
TOP VIEW



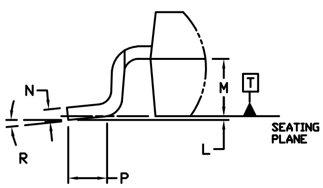
SIDE VIEW
DUAL GUAGE CONSTRUCTION



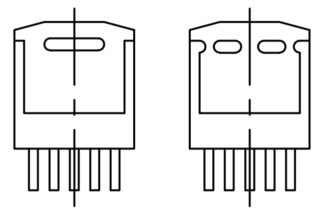
BOTTOM VIEW



SIDE VIEW
SINGLE GUAGE CONSTRUCTION



DETAIL C
TIP LEADFORM
ROTATED 90° CW

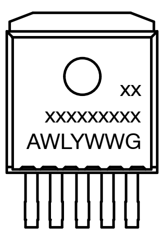


BOTTOM VIEW
OPTIONAL CONSTRUCTIONS

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCHES
3. TAB CONTOUR OPTIONAL WITHIN DIMENSIONS A AND K.
4. DIMENSIONS U AND V ESTABLISH A MINIMUM MOUNTING SURFACE FOR TERMINAL 4.
5. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH OR GATE PROTRUSIONS. MOLD FLASH AND GATE PROTRUSIONS NOT TO EXCEED 0.025 (0.635) MAXIMUM.

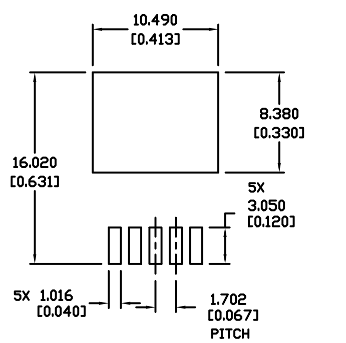
DIM	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.
A	0.396	0.403	9.804	10.236
B	0.356	0.368	9.042	9.347
C	0.170	0.180	4.318	4.572
D	0.026	0.036	0.660	0.914
ED	0.045	0.055	1.143	1.397
ES	0.018	0.026	0.457	0.660
G	0.067 BSC		1.702 BSC	
H	0.539	0.579	13.691	14.707
K	0.050 REF		1.270 REF	
L	0.000	0.010	0.000	0.254
M	0.088	0.102	2.235	2.591
N	0.018	0.026	0.457	0.660
P	0.058	0.078	1.473	1.981
R	0°	8°	0°	8°
S	0.116 REF		2.946 REF	
U	0.200 MIN		5.080 MIN	
V	0.250 MIN		6.350 MIN	

GENERIC MARKING DIAGRAM*



XXXXXX	= Device Code
A	= Assembly Location
WL	= Wafer Lot
Y	= Year
WW	= Work Week
G	= Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.



RECOMMENDED MOUNTING FOOTPRINT *

* For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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DESCRIPTION:	D2PAK 5−LEAD	PAGE 1 OF 1

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