LP8340 Low Dropout, Low I_Q, 1.0A CMOS Linear Regulator

Check for Samples: LP8340

FEATURES

- **±1.5% Typical V_{OUT} Tolerance**
- **420mV Typical Dropout @ 1.0A (V_O = 5V)**
- **Wide Operating Range 2.7V to 10V**
- **Internal 1.0A PMOS Output Transistor**
- **19µA Typical Quiescent Current**
- **Thermal Overload Limiting**
- **Foldback Current Limiting**
- **Zener Trimmed Bandgap Reference**
- **Space Saving WSON package**
- **Temperature Range**
  - **LP8340C 0°C to 125°C**
  - **LP8340I −40°C to 125°C**

APPLICATIONS

- **Hard Disk Drives**
- **Notebook Computers**
- **Battery Powered Electronics**
- **Portable Instrumentation**

DESCRIPTION

The LP8340 low-dropout CMOS linear regulator is available in 5V, 3.3V, 2.5V, 1.8V and adjustable output versions. Packaged in the 6ld WSON package and 3ld PFM. The LP8340 can deliver up to 1.0A output current.

Typical dropout voltage is 420mV at 1.0A for the 5.0V version, 540mV at 1.0A for the 3.3V version, 670mV at 1.0A for the 2.5V version and 680mV at 800mA for the 1.8V version.

The LP8340 includes a zener trimmed bandgap voltage reference, foldback current limiting and thermal overload limiting.

The LP8340 features a PMOS output transistor which unlike PNP type low dropout regulators requires no base drive current. This allows the device ground current to remain less than 50µA over operating temperature, supply voltage and irrespective of the load current.

Typical Applications

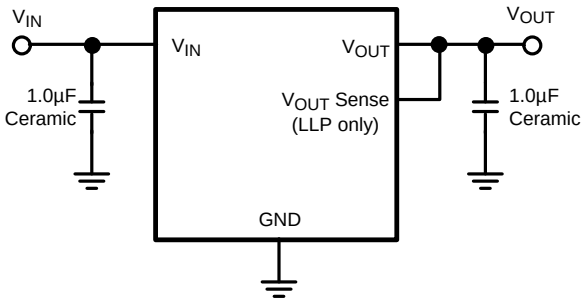


Figure 1. Fixed V_{OUT}

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

All trademarks are the property of their respective owners.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

Copyright © 2003–2013, Texas Instruments Incorporated

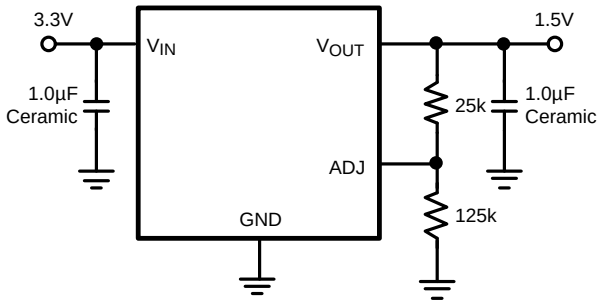


Figure 2. Adjustable V_{OUT}

Connection Diagrams

Bottom View

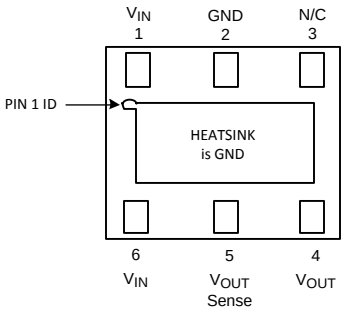


Figure 3. 6-Pin WSON Package
Fixed Output Voltage
See Package Number NGD0006A

Bottom View

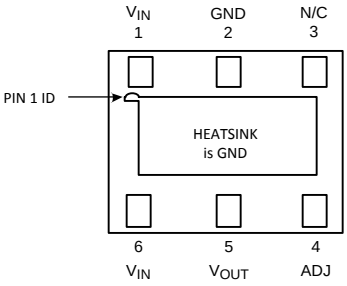


Figure 4. 6-Pin WSON Package
Adjustable Output Voltage
See Package Number NGD0006A

NOTE

V_{IN} Pins (Pin 1 & 6) must be connected together externally for full 1 amp operation (500mA max per pin).

V_{OUT} Sense (Pin 5) must be connected to V_{OUT} (Pin 4).

Top View

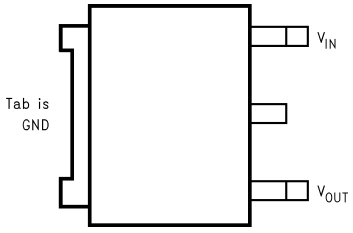


Figure 5. PFM Package
See Package Number NDP0003B

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Copyright © 2003–2013, Texas Instruments Incorporated

Absolute Maximum Ratings(1)(2)(3)

V_{IN}, V_{OUT}, V_{OUT} Sense, ADJ		−0.3V to 12V
Storage Temperature Range		−65°C to 160°C
Junction Temperature (T_J)		150°C
Power Dissipation		See(4)
ESD Rating	Human Body Model(5)	2kV
	Machine Model	200V

(1) Absolute Maximum ratings indicate limits beyond which damage may occur. Electrical specifications do not apply when operating the device outside of its rated operating conditions.
(2) All voltages are with respect to the potential at the ground pin.
(3) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(4) Maximum Power dissipation for the device is calculated using the following equations: $P_D = \frac{T_{J(MAX)} - T_A}{\theta_{JA}}$ where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance. The value of the θ_{JA} for the WSON package is specifically dependant on the PCB trace area, trace material, and the number of layers and thermal vias. For improved thermal resistance and power dissipation for the WSON package, refer to Application Note AN-1187 (SNOA401).
(5) Human body model 1.5kΩ in series with 100pF.

Operating Ratings(1)(2)

Supply Voltage	2.7 to 10V
Temperature Range	
LP8340C	0°C to 125°C
LP8340I	−40°C to 125°C

(1) Absolute Maximum ratings indicate limits beyond which damage may occur. Electrical specifications do not apply when operating the device outside of its rated operating conditions.
(2) All voltages are with respect to the potential at the ground pin.

LP8340C Electrical Characteristics

Unless otherwise specified all limits ensured for $V_{IN} = V_O + 1V$, $C_{IN} = C_{OUT} = 10\mu F$, $T_J = 25°C$. **Boldface** limits apply over the full operating temperature range of $T_J = 0°C$ to 125°C

Symbol	Parameter	Conditions	Min(1)	Typ(2)	Max(1)	Units
V_{IN}	Input Voltage	LP8340-ADJ,1.8, 2.5 LP8340-3.3, 5.0	**2.7**		**10** **10**	V
V_{OUT}	Output Voltage	LP8340-ADJ, ADJ = OUT I_{OUT} = 10mA, V_{IN} = 2.7V, T_J = 25°C 100µA ≤I_{OUT}≤ 800mA, 3.0V ≤V_{IN}≤V_{OUT} +4V 800mA <I_{OUT} ≤1.0A, 3.2V ≤V_{IN} ≤V_{OUT} +4V	 1.231 **1.213** **1.213**	1.250	 1.269 **1.288** **1.288**	V
		LP8340-1.8 I_{OUT} = 10mA, V_{IN} = 2.8V, T_J = 25°C 100µA ≤I_{OUT} ≤800mA, 3.2V ≤V_{IN}≤6V 800mA <I_{OUT} ≤1.0A, 3.4V ≤V_{IN} ≤6V	 1.773 **1.746** **1.746**	1.800	 1.827 **1.854** **1.854**	V
		LP8340-2.5 I_{OUT} = 10mA, V_{IN} = 3.8V, T_J = 25°C 100µA ≤I_{OUT} ≤1.0A, 3.8V ≤V_{IN} ≤6.5V	 2.463 **2.425**	2.500	 2.538 **2.575**	V
		LP8340-3.3 I_{OUT} = 10mA, V_{IN} = 4.3V T_J = 25°C 100µA ≤I_{OUT} ≤1.0A, 4.3V ≤V_{IN} ≤7.5V	 3.250 **3.201**	3.300	 3.350 **3.399**	V
		LP8340-5.0 I_{OUT} = 10mA, V_{IN} = 6V, T_J = 25°C 100µA ≤I_{OUT} ≤1.0A, 6V ≤V_{IN} ≤9V	 4.925 **4.850**	5.000	 5.075 **5.150**	V

(1) All limits are specified by testing or statistical analysis.
(2) Typical Values represent the most likely parametric norm.

Copyright © 2003–2013, Texas Instruments Incorporated

LP8340C Electrical Characteristics (continued)

Unless otherwise specified all limits ensured for $V_{IN} = V_O + 1V$, $C_{IN} = C_{OUT} = 10\mu F$, $T_J = 25°C$. **Boldface** limits apply over the full operating temperature range of $T_J = 0°C$ to $125°C$

Symbol	Parameter	Conditions	Min(1)	Typ(2)	Max(1)	Units
ΔV_O	Load Regulation	LP8340-ADJ, ADJ=OUT I_{OUT} = 1mA to 1.0A, V_{IN} = 3.2V		6	**25**	mV
		LP8340-1.8 I_{OUT} = 1mA to 1.0A, V_{IN} = 3.4V		8	**30**	
		LP8340-2.5 I_{OUT} = 1mA to 1.0A, V_{IN} = 3.5V		15	**50**	
		LP8340-3.3 I_{OUT} = 1mA to 1.0A, V_{IN} = 4.3V		20	**75**	
		LP8340-5.0 I_{OUT} = 1mA to 1.0A, V_{IN} = 6V		25	**100**	
ΔV_O	Line Regulation	V_{OUT} + 0.5V ≤V_{IN} ≤10V, I_{OUT} = 25mA(3)		4	**15**	mV
$V_{IN} - V_O$	Dropout Voltage(3)(4)	LP8340-1.8 I_{OUT} = 800mA		680	**1400**	mV
		LP8340-2.5 I_{OUT} = 800mA		550	**1000**	
		LP8340-2.5 I_{OUT} = 1.0A		670	**1300**	
		LP8340-3.3 LP8340-ADJ, V_{OUT} = 3.3V, I_{OUT} = 800mA		420	**800**	
		LP8340-3.3 LP8340-ADJ, I_{OUT} = 1.0A		540	**1000**	
		LP8340-5.0 I_{OUT} = 800mA		330	**650**	
		LP8340-5.0 I_{OUT} = 1.0A		420	**800**	
I_Q	Quiescent Current	V_{IN} ≤10V		19	**50**	µA
	Minimum Load Current	$V_{IN} - V_{OUT}$ ≤4V			**100**	µA
I_{LIMIT}	Foldback Current Limit	$V_{IN} - V_{OUT}$ >5V		450		mA
		$V_{IN} - V_{OUT}$ <4V		1600		
	Ripple Rejection Ratio	V_{IN} (dc) = V_{OUT} + 2V V_{IN} (ac) = 1 V_{P-P} @ 120Hz	**48**	55		dB
T_{SD}	Thermal Shutdown Temp. Thermal Shutdown Hyst.			160 10		°C
	ADJ Input Leakage Current	V_{ADJ} = 1.5V or 0V		±0.01	±100	nA
	V_{OUT} Leakage Current	LP8340-ADJ ADJ = OUT, V_{OUT} = 2V, V_{IN} = 10V			10	µA
		LP8340-1.8, V_{OUT} = 2.5V, V_{IN} = 10V			10	
		LP8340-2.5, V_{OUT} = 3.5V, V_{IN} = 10V			10	
		LP8340-3.3, V_{OUT} = 4V, V_{IN} = 10V			10	
		LP8340-5.0, V_{OUT} = 6V, V_{IN} = 10V			10	
e_n	Output Noise	10Hz to 10kHz, R_L = 1kΩ, C_{OUT} = 10µF		250		µVrms

(3) Condition does not apply to input voltages below 2.7V since this is the minimum input operating voltage.
(4) Dropout voltage is measured by reducing V_{IN} until V_O drops 100mV from its normal value.

Copyright © 2003–2013, Texas Instruments Incorporated

LP8340I Electrical Characteristics

Unless otherwise specified all limits ensured for $V_{IN} = V_O + 1V$, $C_{IN} = C_{OUT} = 10\mu F$, $T_J = 25°C$. **Boldface** limits apply over the full operating temperature range of $T_J = -40°C$ to $125°C$

Symbol	Parameter	Conditions	Min[1]	Typ[2]	Max[1]	Units
V_{IN}	Input Voltage	LP8340-ADJ,1.8, 2.5 LP8340-3.3, 5.0	**2.7**		**10** **10**	V
V_{OUT}	Output Voltage	LP8340-ADJ, ADJ = OUT I_{OUT} = 10mA, V_{IN} = 2.7V, T_J = 25°C 100µA ≤I_{OUT}≤ 800mA, 3.0V ≤V_{IN}≤V_{OUT} +4V 800mA <I_{OUT} ≤1.0A, 3.2V ≤V_{IN} ≤V_{OUT} +4V	1.231 **1.213** **1.213**	1.250	1.269 **1.288** **1.288**	V
		LP8340-1.8 I_{OUT} = 10mA, V_{IN} = 2.8V, T_J = 25°C 100µA ≤I_{OUT} ≤800mA, 3.2V ≤V_{IN}≤6V 800mA <I_{OUT} ≤1.0A, 3.4V ≤V_{IN} ≤6V	1.773 **1.746** **1.746**	1.800	1.827 **1.854** **1.854**	V
		LP8340-2.5 I_{OUT} = 10mA, V_{IN} = 3.8V, T_J = 25°C 100µA ≤I_{OUT} ≤1.0A, 3.8V ≤V_{IN} ≤6.5V	2.463 **2.425**	2.500	2.538 **2.575**	V
		LP8340-3.3 I_{OUT} = 10mA, V_{IN} = 4.3V T_J = 25°C 100µA ≤I_{OUT} ≤1.0A, 4.3V ≤V_{IN} ≤7.5V	3.250 **3.201**	3.300	3.350 **3.399**	V
		LP8340-5.0 I_{OUT} = 10mA, V_{IN} = 6V, T_J = 25°C 100µA ≤I_{OUT} ≤1.0A, 6V ≤V_{IN} ≤9V	4.925 **4.850**	5.000	5.075 **5.150**	V
ΔV_O	Load Regulation	LP8340-ADJ, ADJ=OUT I_{OUT} = 1mA to 1.0A, V_{IN} = 3.2V		6	**25**	mV
		LP8340-1.8 I_{OUT} = 1mA to 1.0A, V_{IN} = 3.4V		8	**30**	
		LP8340-2.5 I_{OUT} = 1mA to 1.0A, V_{IN} = 3.5V		15	**50**	
		LP8340-3.3 I_{OUT} = 1mA to 1.0A, V_{IN} = 4.3V		20	**75**	
		LP8340-5.0 I_{OUT} = 1mA to 1.0A, V_{IN} = 6V		25	**100**	
ΔV_O	Line Regulation	V_{OUT} + 0.5V ≤V_{IN} ≤10V, I_{OUT} = 25mA[3]		4	**15**	mV
$V_{IN} - V_O$	Dropout Voltage[3][4]	LP8340-1.8 I_{OUT} = 800mA		680	**1400**	mV
		LP8340-2.5 I_{OUT} = 800mA		550	**1000**	
		LP8340-2.5 I_{OUT} = 1.0A		670	**1300**	
		LP8340-3.3 LP8340-ADJ, V_{OUT} = 3.3V, I_{OUT} = 800mA		420	**800**	
		LP8340-3.3 LP8340-ADJ, I_{OUT} = 1.0A		540	**1000**	
		LP8340-5.0 I_{OUT} = 800mA		330	**650**	
		LP8340-5.0 I_{OUT} = 1.0A		420	**800**	
I_Q	Quiescent Current	V_{IN} ≤10V		19	**50**	µA
	Minimum Load Current	$V_{IN} - V_{OUT}$ ≤4V			**100**	µA
I_{LIMIT}	Foldback Current Limit	$V_{IN} - V_{OUT}$ >5V		450		mA
		$V_{IN} - V_{OUT}$ <4V		1600		
	Ripple Rejection Ratio	V_{IN} (dc) = V_{OUT} + 2V V_{IN} (ac) = 1 V_{P-P} @ 120Hz	**48**	55		dB

(1) All limits are specified by testing or statistical analysis.
(2) Typical Values represent the most likely parametric norm.
(3) Condition does not apply to input voltages below 2.7V since this is the minimum input operating voltage.
(4) Dropout voltage is measured by reducing V_{IN} until V_O drops 100mV from its normal value.

Copyright © 2003–2013, Texas Instruments Incorporated

LP8340I Electrical Characteristics (continued)

Unless otherwise specified all limits ensured for $V_{IN} = V_O + 1V$, $C_{IN} = C_{OUT} = 10\mu F$, $T_J = 25°C$. **Boldface** limits apply over the full operating temperature range of $T_J = -40°C$ to $125°C$

Symbol	Parameter	Conditions	Min(1)	Typ(2)	Max(1)	Units
T_{SD}	Thermal Shutdown Temp. Thermal Shutdown Hyst.			160 10		°C
	ADJ Input Leakage Current	V_{ADJ} = 1.5V or 0V		±0.01	±100	nA
	V_{OUT} Leakage Current	LP8340-ADJ ADJ = OUT, V_{OUT} = 2V, V_{IN} = 10V			10	µA
		LP8340-1.8, V_{OUT} = 2.5V, V_{IN} = 10V			10	
		LP8340-2.5, V_{OUT} = 3.5V, V_{IN} = 10V			10	
		LP8340-3.3, V_{OUT} = 4V, V_{IN} = 10V			10	
		LP8340-5.0, V_{OUT} = 6V, V_{IN} = 10V			10	
e_n	Output Noise	10Hz to 10kHz, R_L = 1kΩ, C_{OUT} = 10µF		250		µVrms

Copyright © 2003–2013, Texas Instruments Incorporated

Typical Performance Characteristics

Unless otherwise specified, $V_{IN} = V_O + 1.5V$, $C_{IN} = C_{OUT} = 10\mu F$ X7R ceramic, $T_J = 25°C$

Output Voltage Change vs. Temperature

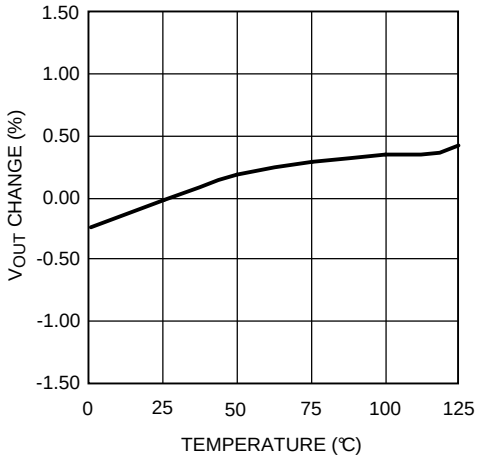


Figure 6.

Dropout Voltage vs. Load Current

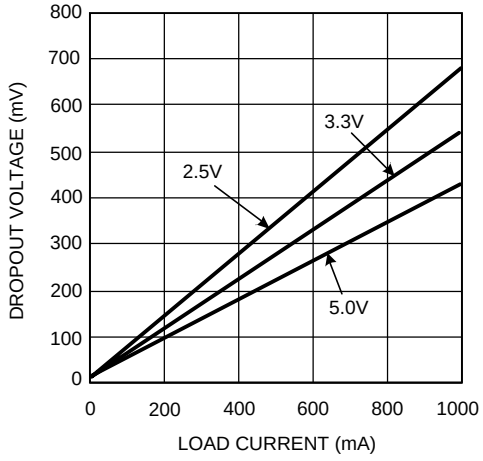


Figure 7.

Ground Current vs. Temperature (I_{LOAD} = 1A)

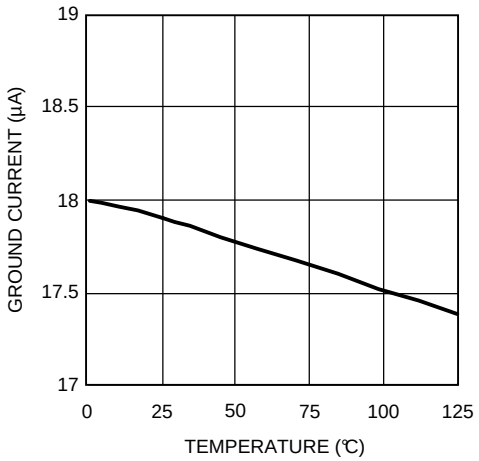


Figure 8.

Ground Current vs. Load Current

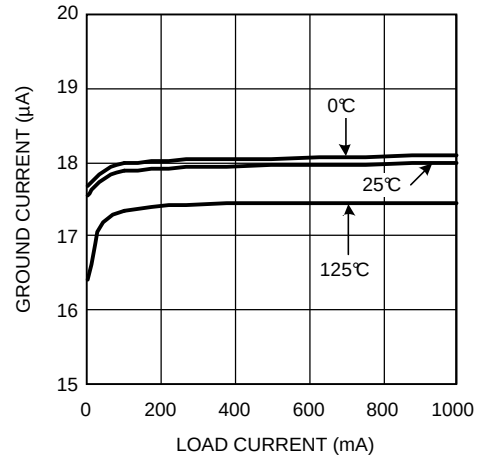


Figure 9.

Ground Current vs. Input Voltage

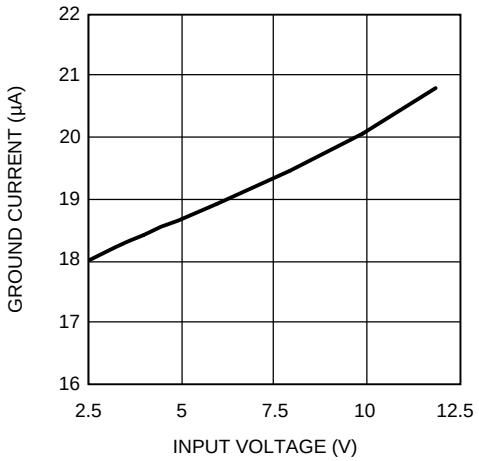


Figure 10.

Ripple Rejection Ratio vs. Frequency

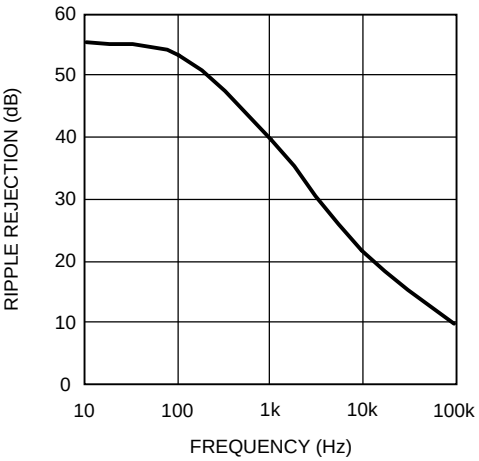


Figure 11.

Copyright © 2003–2013, Texas Instruments Incorporated

Typical Performance Characteristics (continued)

Unless otherwise specified, $V_{IN} = V_O + 1.5V$, $C_{IN} = C_{OUT} = 10\mu F$ X7R ceramic, $T_J = 25°C$

LP8340-1.8V Min V_{IN}

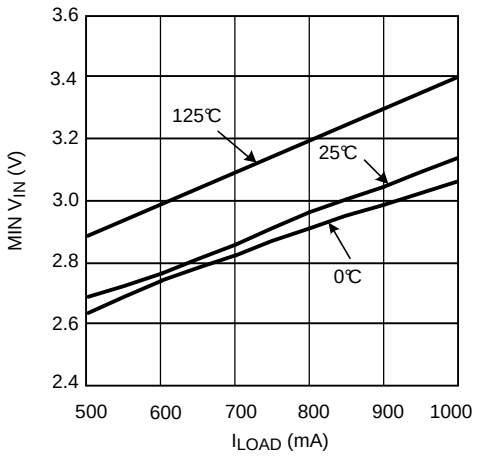


Figure 12.

LP8340-ADJ Min V_{IN}

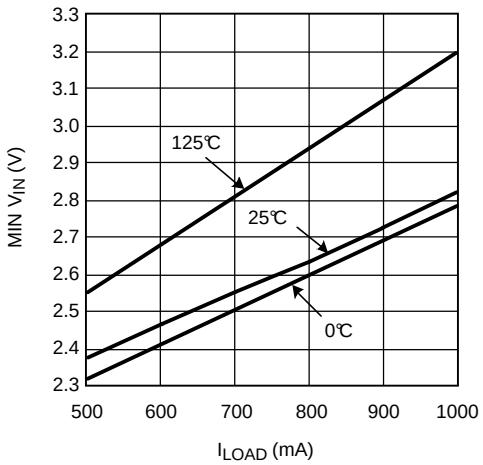


Figure 13.

Load Transient Response

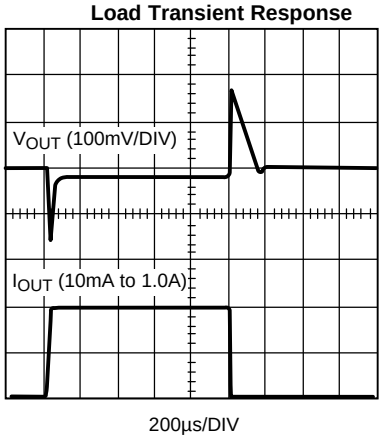


Figure 14.

Line Transient Response (I_{LOAD} = 10mA)

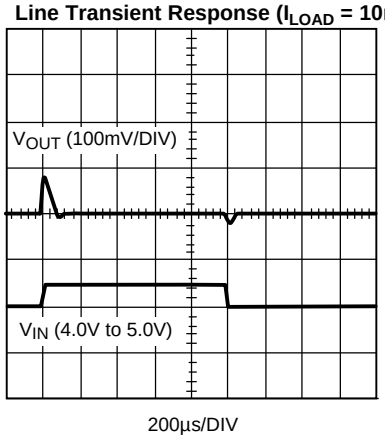


Figure 15.

Start-up Response

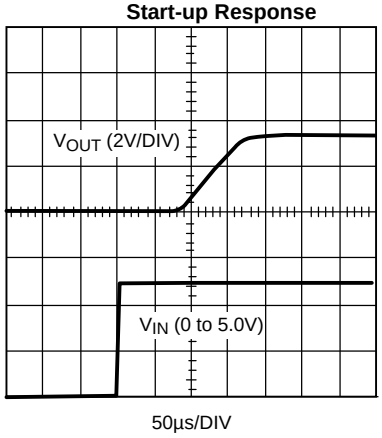


Figure 16.

Minimum Input Voltage Rise Time

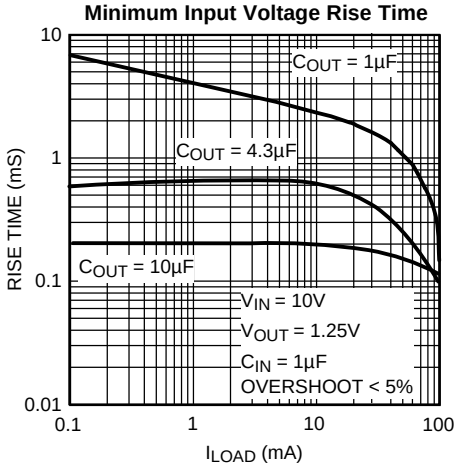


Figure 17.

Copyright © 2003–2013, Texas Instruments Incorporated

Typical Performance Characteristics (continued)

Unless otherwise specified, $V_{IN} = V_O + 1.5V$, $C_{IN} = C_{OUT} = 10\mu F$ X7R ceramic, $T_J = 25°C$

Minimum Input Voltage Rise Time

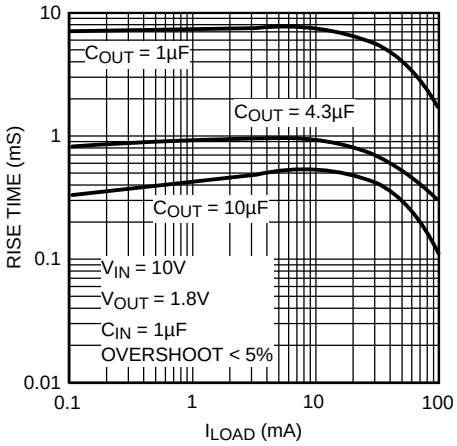


Figure 18.

Minimum Input Voltage Rise Time

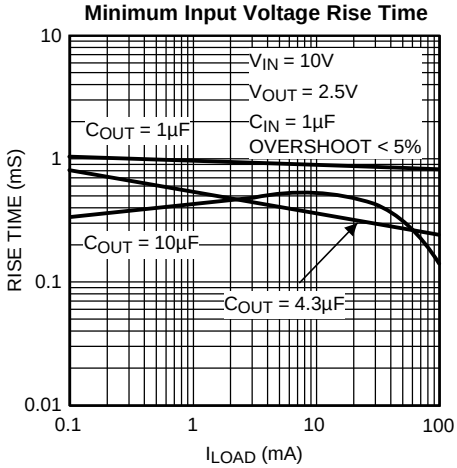


Figure 19.

Minimum Input Voltage Rise Time

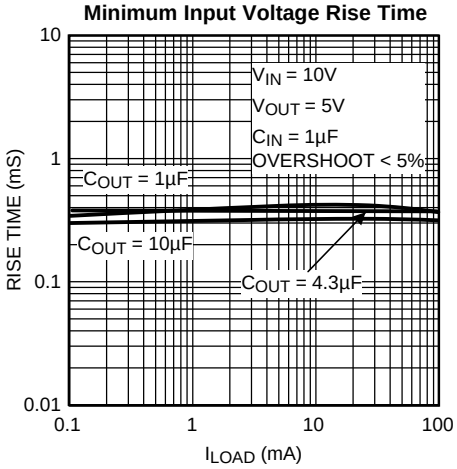


Figure 20.

Minimum Input Voltage Rise Time

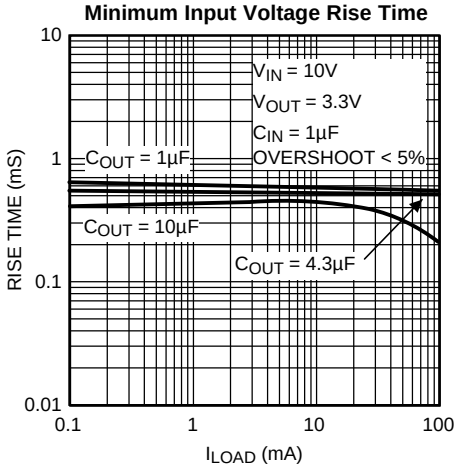


Figure 21.

Copyright © 2003–2013, Texas Instruments Incorporated

APPLICATIONS SECTION

GENERAL INFORMATION

The LP8340 is a low-dropout, low quiescent current linear regulator. As shown in Figure 22 it consists of a 1.25V reference, error amplifier, MOSFET driver, PMOS pass transistor and for the fixed output versions, an internal feedback network (R_1/R_2). In addition, the device is protected from overload by a thermal shutdown circuit and a foldback current limit circuit

The 1.25V reference is connected to the inverting input of the error amplifier. Regulation of the output voltage is achieved by means of negative feedback to the non-inverting input of the error amplifier. Feedback resistors R_1 and R_2 are either internal or external to the device, depending on whether it is a fixed voltage version or the adjustable version. The negative feedback and high open loop gain of the error amplifier cause the two inputs of the error amp to be virtually equal in voltage. If the output voltage changes due to load changes, the error amplifier and MOSFET driver provide the appropriate drive to the pass transistor to maintain the error amplifier's inputs as virtually equal.

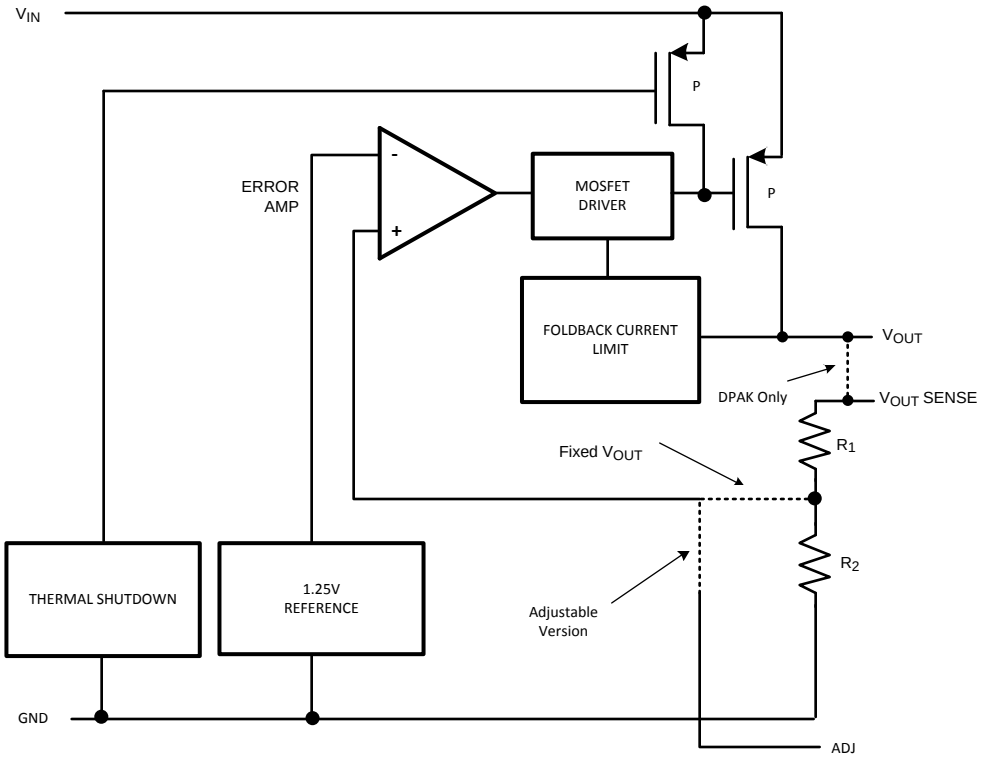


Figure 22. LP8340 Functional Block Diagram

EXTERNAL CAPACITOR

An Input capacitor of 1µF or greater is required between the LP8340 V_{IN} pin and ground. While 1µF will provide adequate bypassing of the V_{IN} supply larger values of input capacitor (i.e. 10µF) can provide improved bypassing of power supply noise.

Stable operation can be achieved with an output capacitor of 1µF or greater, either ceramic X7R dielectric or aluminum/tantalum electrolytic. While the minimum capacitor value is 1µF, the typical output capacitor values selected range from 1µF to 10µF. The larger values provide improved load-transient response, power supply rejection and stability.

Copyright © 2003–2013, Texas Instruments Incorporated

OUTPUT VOLTAGE SETTING (ADJ VERSION ONLY)

The output voltage is set according to the amount of negative feedback (Note that the pass transistor inverts the feedback signal). This feedback is determined by R_1 and R_2 with the resulting output voltage represented by the following equation:

$$V_O = V_{REF}\left[\frac{R_1}{R_2} + 1\right] \quad (1)$$

Use the following equation to determine the values of R_1 and R_2 for a desired V_{OUT} (R_2 = 100kΩ is recommended).

$$R_1 = R_2\left[\frac{V_O}{1.25V} - 1\right] \quad (2)$$

MINIMUM LOAD CURRENT

A minimum load of 100µA is required for regulation and stability over the entire operating temperature range. If actual load current fall below 100µA it is recommended that a resistor of value $R_L = V_O/100\mu A$ be placed between V_O and ground.

START UP CONSIDERATIONS

Under certain operating conditions, overshoot of V_{OUT} at start-up can occur. The observed overshoot is a function of rise time of V_{IN} waveform, C_{OUT}, start-up load current, and $V_{IN}-V_{OUT}$ differential. The relationship between these conditions is shown in the Typical Performance Characteristics curves (Minimum Input Voltage Rise Time). V_{IN} rise times above the curve result in <5% overshoot.

Customers are encouraged to check the suitability of LP8340 in their specific application.

Copyright © 2003–2013, Texas Instruments Incorporated

REVISION HISTORY

Changes from Revision C (April 2013) to Revision D	Page
• Changed layout of National Data Sheet to TI format	11

Copyright © 2003–2013, Texas Instruments Incorporated

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LP8340ILDX-ADJ/NOPB	ACTIVE	WSON	NGD	6	4500	RoHS & Green	SN	Level-3-260C-168 HR	0 to 125	L078B	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

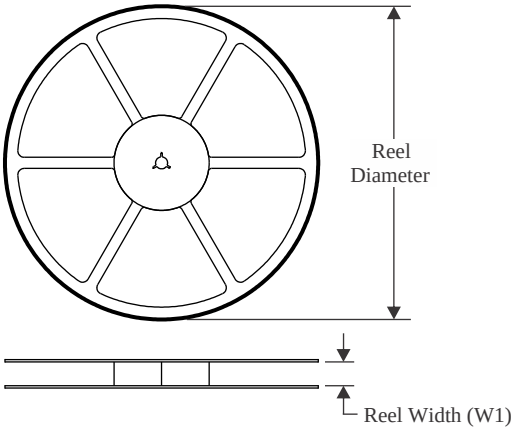
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

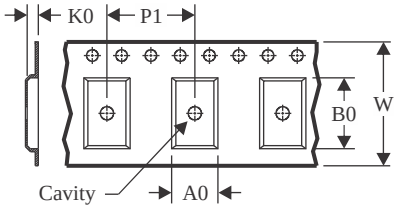
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

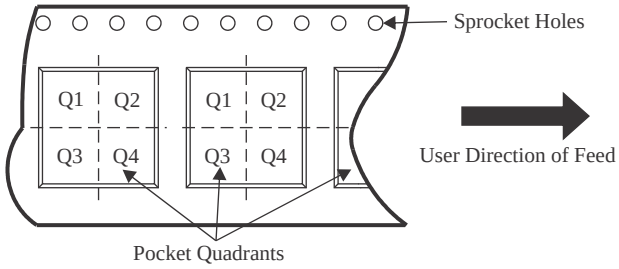


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

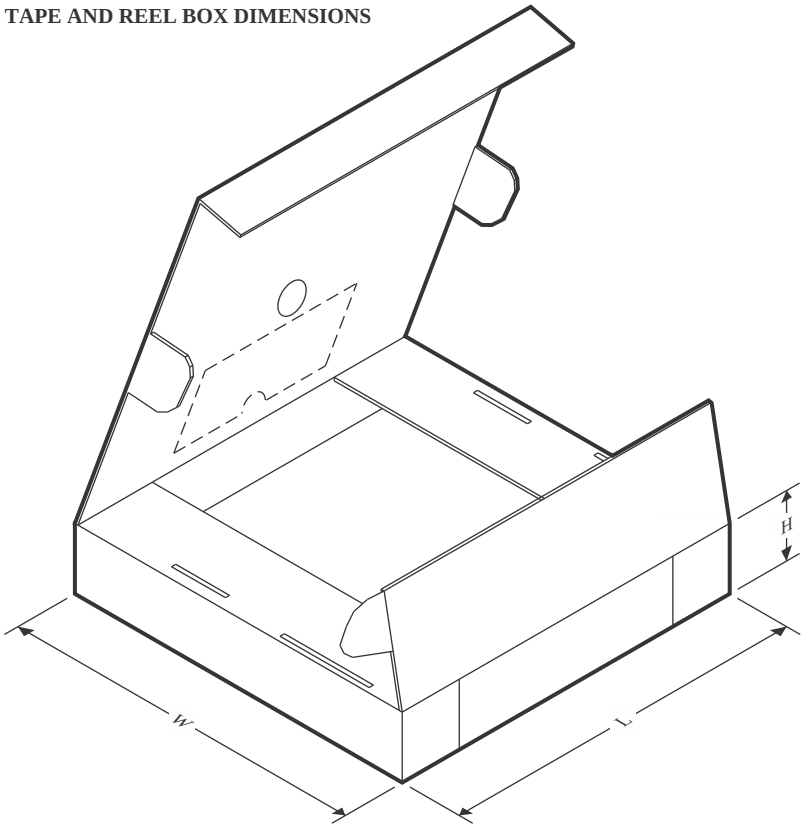
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP8340ILDX-ADJ/NOPB	WSON	NGD	6	4500	330.0	12.4	3.6	3.2	1.0	8.0	12.0	Q1

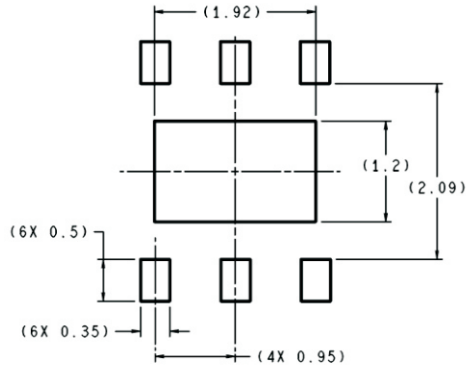
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

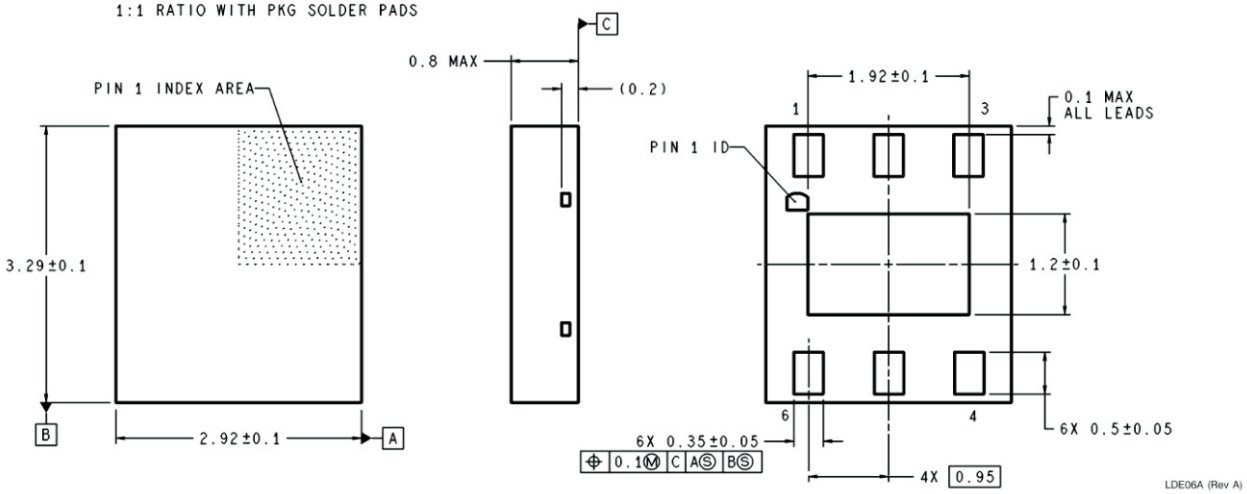
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP8340ILDX-ADJ/NOPB	WSON	NGD	6	4500	356.0	356.0	36.0

NGD0006A



RECOMMENDED LAND PATTERN
1:1 RATIO WITH PKG SOLDER PADS

DIMENSIONS ARE IN MILLIMETERS



IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2024, Texas Instruments Incorporated