LMS8117A 1-A Low-Dropout Linear Regulator

1 Features

- Available in 1.8-V, 3.3-V, and Adjustable Versions
- Space-Saving SOT-223 and TO-252 Packages
- Current Limiting and Thermal Protection
- Output Current: 1 A
- Temperature Range: 0°C to 125°C
- Line Regulation: 0.2% (Maximum)
- Load Regulation: 0.4% (Maximum)

2 Applications

- Post Regulator for Switching DC-DC Converters
- High Efficiency Linear Regulators
- Battery Chargers
- Battery-Powered Instrumentation

3 Description

The LMS8117A device is a series of low-dropout voltage regulators with a dropout of 1.2 V at 1 A of load current. The device has the same pinout as the LM317.

The LMS8117A is available in an adjustable version, which can set the output voltage from 1.27 V to 13.8 V with only two external resistors. In addition, the device is also available in two fixed voltages, 1.8 V and 3.3 V.

The LMS8117A offers current limiting and thermal shutdown. The device circuit includes a Zener trimmed band-gap reference to assure output voltage accuracy to within ±1%.

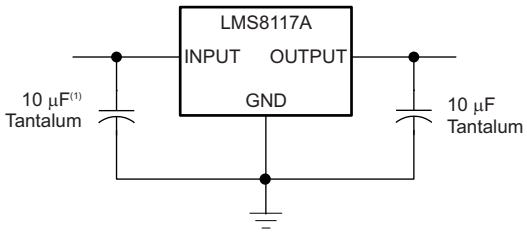
The LMS8117A is available in SOT-223 and TO-252 D-PAK packages. A 10-µF (minimum) tantalum capacitor is required at the output to improve the transient response and stability.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LMS8117A	SOT-223 (4)	3.50 mm × 6.50 mm
	TO-252 (3)	6.10 mm × 6.58 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Functional Block Diagram



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4 Revision History

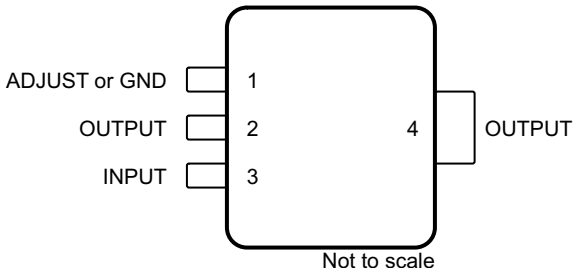
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision E (April 2005) to Revision F **Page**

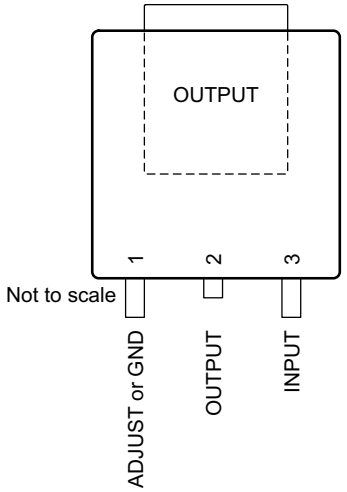
- Added *Device Information* table, *Pin Configuration and Functions* section, *Specifications* section, *ESD Ratings* table, *Recommended Operating Conditions* table, *Detailed Description* section, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Deleted *Ordering Information* table; see *Package Option Addendum* at the end of the data sheet ... 1
- Deleted Soldering information from *Absolute Maximum Ratings* table ... 3
- Added *Thermal Information* table ... 4
- Changed Junction-to-ambient, $R_{\theta JA}$, values in *Thermal Information* table From: 136°C/W To: 61.4°C/W (SOT-223) and From: 92°C/W To: 56.1°C/W(TO-252) ... 4
- Changed Junction-to-case, $R_{\theta JC(top)}$, values in *Thermal Information* table From: 15°C/W To: 43°C/W (SOT-223) and From: 10°C/W To: 42.8°C/W (TO-252) ... 4
- Deleted duplicate paragraph from *Output Voltage* section ... 10

5 Pin Configuration and Functions

DCY Package
3-Pin SOT-223
Top View



NDP Package
3-Pin TO-252
Top View



Pin Functions

PIN			I/O	DESCRIPTION
NAME	SOT-223	TO-252		
ADJUST or GND	1	1	—	Adjust pin for adjustable output version. Ground pin for fixed output versions.
INPUT	3	3	I	Input voltage (V_I) pin for the regulator.
OUTPUT	2, Tab (4)	2, Tab	O	Output voltage (V_O) pin for the regulator.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)

	MIN	MAX	UNIT
Maximum input voltage (all versions), V_{IN}		20	V
Power dissipation(3)	Internally limited		
Junction temperature, $T_{J(MAX)}$		150	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(3) The maximum power disspation is a function of $T_{J(MAX)}$, $R_{\theta JA}$, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} – T_A) / R_{\theta JA}$. All numbers apply for packages soldered directly onto a PCB.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)(2)	±2000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) For testing purposes, ESD was applied using human body model, 1.5-kΩ resistor in series iwth 100-pF capacitor.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Input voltage (all versions)		15	V
Junction temperature, T_J	0	125	°C

6.4 Thermal Information

THERMAL METRIC[1]		LMS8117A		UNIT
		DCY (SOT-223)	NDP (TO-252)	
		4 PINS	3 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	61.4	56.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	43	42.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	10	29.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	2.4	5.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	9.9	28.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	4.1	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

Typical values apply for T_J = 25°C and Minimum and Maximum limits apply for T_J = 0°C to 125°C (unless otherwise noted). Typical values represent the most likely parametric norm. All limits are guaranteed using by testing or statistical analysis.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{REF}	Reference voltage	Adjustable version	I_{OUT} = 10 mA, $V_{IN} - V_{OUT}$ = 2 V, T_J = 25°C	1.238	1.25	1.262	V
			I_{OUT} = 10 mA to 1 A, $V_{IN} - V_{OUT}$ = 1.4 V to 10 V	1.225		1.27	
V_{OUT}	Output voltage	1.8-V version	I_{OUT} = 10 mA, V_{IN} = 3.8 V, T_J = 25°C	1.782	1.8	1.818	V
			I_{OUT} = 0 A to 1 A, V_{IN} = 3.2 V to 10 V	1.746		1.854	
		3.3-V version	I_{OUT} = 10 mA, V_{IN} = 5 V, T_J = 25°C	3.267	3.3	3.333	
			I_{OUT} = 0 A to 1 A, V_{IN} = 4.75 V to 10 V	3.235		3.365	
ΔV_{OUT}	Line regulation[1]	Adjustable version, I_{OUT} = 10 mA, $V_{IN} - V_{OUT}$ = 1.5 V to 13.75 V			0.035%	0.2%	
		1.8-V version, I_{OUT} = 0 mA, V_{IN} = 3.2 V to 10 V			1	6	mV
		3.3-V version, I_{OUT} = 0 mA , V_{IN} = 4.75 V to 15 V			1	6	
	Load regulation[1]	Adjustable version, I_{OUT} = 10 mA to 1 A, $V_{IN} - V_{OUT}$ = 3 V			0.2%	0.4%	
		1.8-V version, I_{OUT} = 0 mA to 1 A, V_{IN} = 3.2 V			1	10	mV
		3.3-V version, I_{OUT} = 0 mA to 1 A, V_{IN} = 4.75 V			1	10	
$V_{IN} - V_{OUT}$	Dropout voltage[2]	I_{OUT} = 100 mA			1.1	1.15	V
		I_{OUT} = 500 mA			1.15	1.2	
		I_{OUT} = 1 A			1.1	1.25	
I_{LIMIT}	Current limit	$V_{IN} - V_{OUT}$ = 5 V, T_J = 25°C		1	1.4	1.9	A
	Minimum load current[3]	Adjustable version, V_{IN} = 15 V			1.7	5	mA
	Quiescent current	1.8-V and 3.3-V versions, $V_{IN} \le$ 15 V			5	10	mA
	Thermal regulation	30-ms pulse, T_A = 25°C			0.01%	0.1%	W
	Ripple regulation	f_{RIPPLE} = 120 Hz, $V_{IN} - V_{OUT}$ = 3 V, V_{RIPPLE} = 1 V_{PP}		60	75		dB
	ADJUST pin current				60	120	µA
	ADJUST pin current change	I_{OUT} = 10 mA to 1 A, $V_{IN} - V_{OUT}$ = 1.4 V to 10 V			0.2	5	µA
	Temperature stability				0.5%		
	Long term stability	1000 hrs, T_A = 125°C			0.3%		
	RMS output noise	Percentage of V_{OUT}, f = 10 Hz to 10 kHz			0.003%		

(1) Line and load regulation are measured at constant junction room temperature.
(2) The dropout voltage is the input and output differential at which the circuit ceases to regulate against further reduction in input voltage. It is measured when the output voltage drops 100 mV from the nominal value obtained by $V_{IN} = V_{OUT} + 1.5$ V.
(3) The minimum output current required to maintain regulation.

6.6 Typical Characteristics

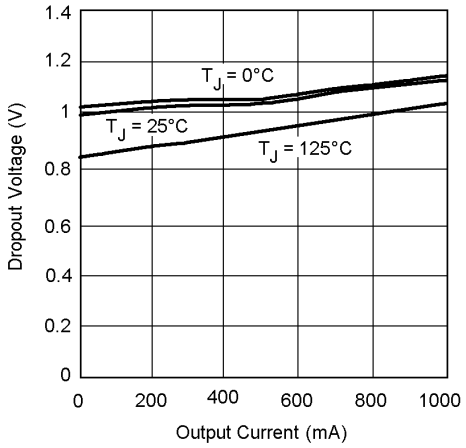


Figure 1. Dropout Voltage

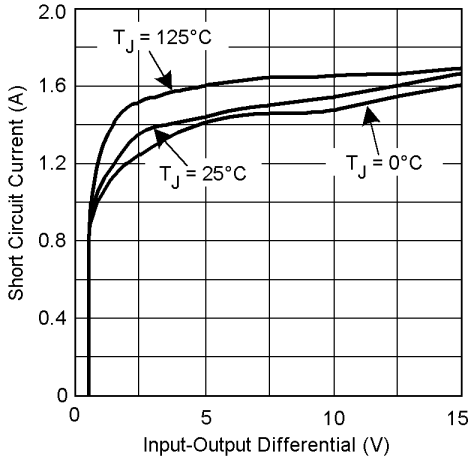


Figure 2. Short-Circuit Current

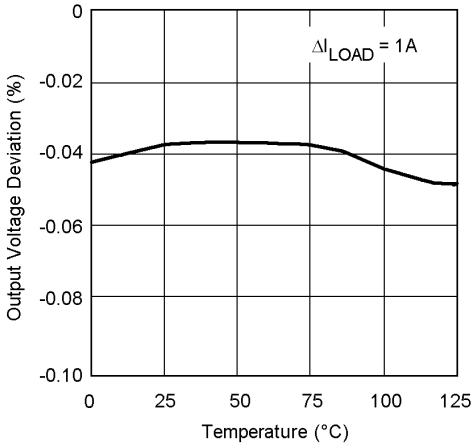


Figure 3. Load Regulation

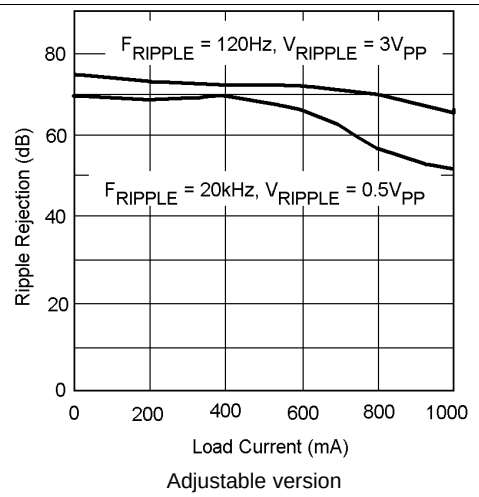


Figure 4. Ripple Regulation vs Current

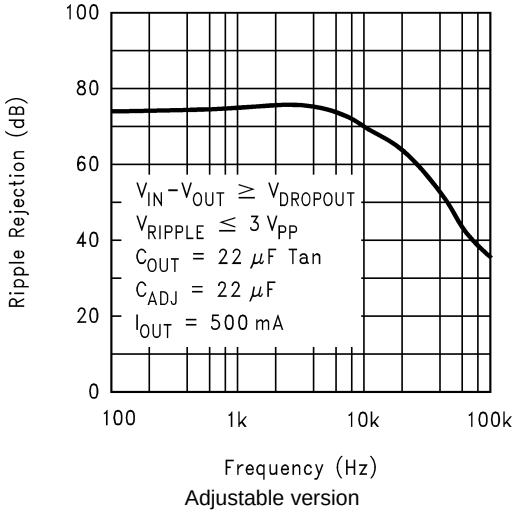


Figure 5. Ripple Rejection

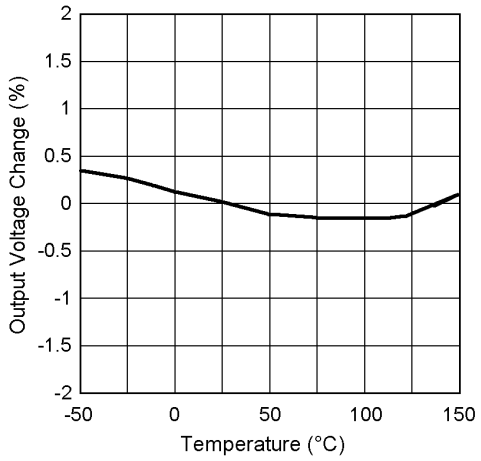


Figure 6. Temperature Stability

Typical Characteristics (continued)

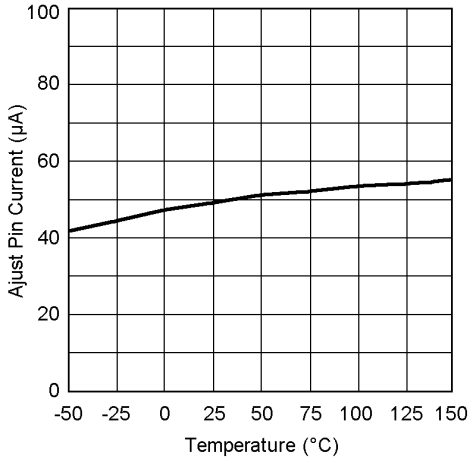
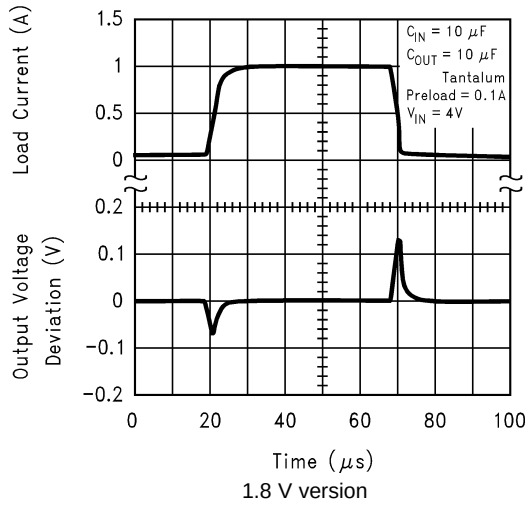
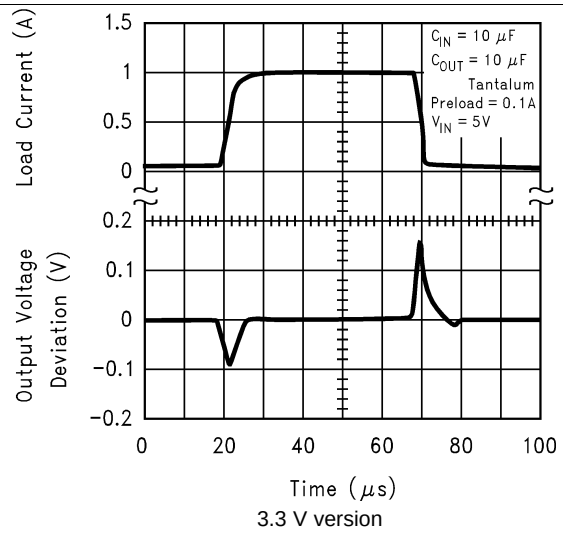


Figure 7. ADJUST Pin Current



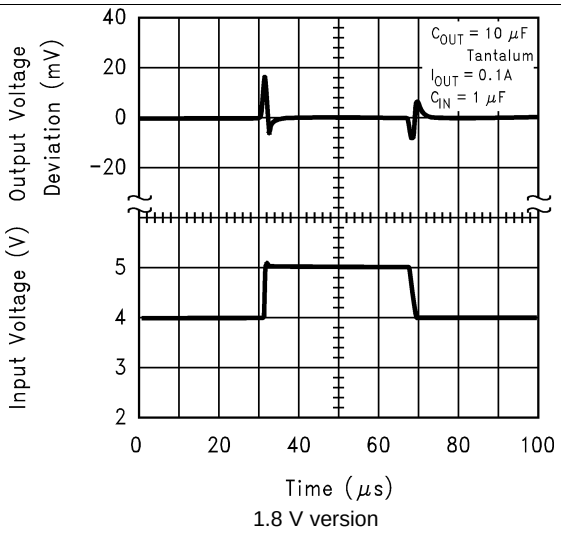
1.8 V version

Figure 8. Load Transient Response



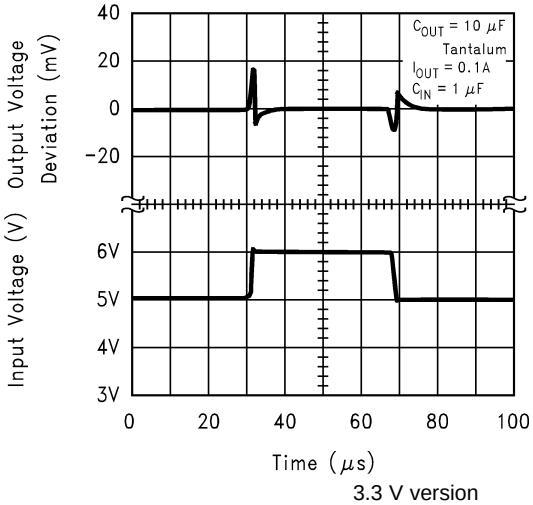
3.3 V version

Figure 9. Load Transient Response



1.8 V version

Figure 10. Line Transient Response



3.3 V version

Figure 11. Line Transient Response

7 Detailed Description

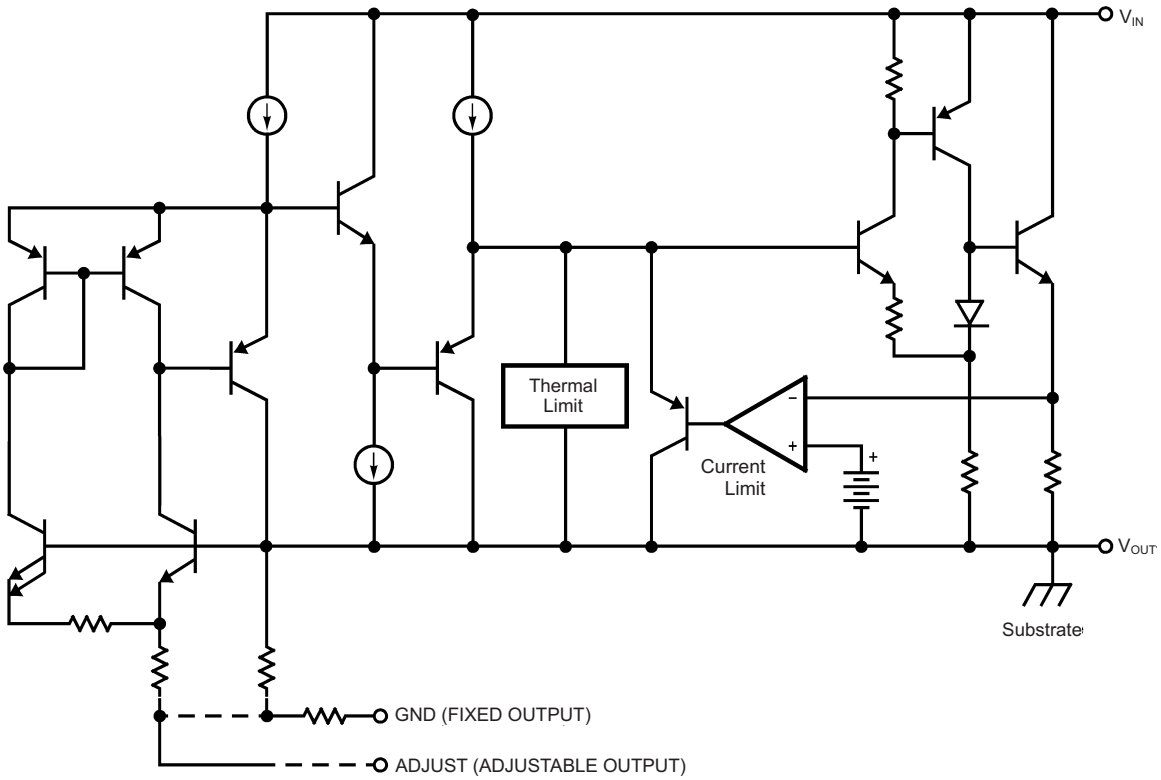
7.1 Overview

The LMS8117A device is a positive-voltage regulator available in 1.8-V, 3.3-V, and adjustable versions. For the adjustable version, the output voltage ranges from 1.25 V to 13.8 V and is set with only two external resistors. This device is capable of supplying up to 1-A output current for an input voltage up to 15 V.

Because this device has a low-dropout voltage of 1.25 V over a junction temperature from 0°C to 125°C, the input voltage can be as low as 2.5 V for proper regulation over the entire temperature range. The LMS8117A also features current limiting and thermal overload protection to help protect the device and is available in the space-saving SOT-223 and TO-252 packages.

The LMS8117A device is versatile in its applications, including uses in programmable output regulation and local on-card regulation. Or, by connecting a fixed resistor between the ADJUST and OUTPUT pins, the device can function as a precision current regulator. An optional output capacitor can be added to improve transient response. The ADJUST pin can be bypassed to achieve very high ripple-rejection ratios, which are difficult to achieve with standard regulators.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Protection

This device provides current limiting and thermal protection to protect the device against overload or damage from operating in excessive heat.

Feature Description (continued)

7.3.2 Programmable Feedback

The ADJUST pin for adjustable versions provide easy output voltage or current (not both) programming. For current regulation applications, a single resistor whose resistance value is 1.25 V/I_O and power rating is greater than $(1.25\ V)^2/R$ must be used. For voltage regulation applications, two resistors set the output voltage.

7.4 Device Functional Modes

7.4.1 Normal Operation

For the adjustable version, the OUTPUT pin sources current as necessary to make V_{OUT} 1.25 V greater than V_{REF} to provide output regulation. For the fixed version, the OUTPUT pin sources current as necessary to make V_{OUT} greater than the GND pin voltage by the specific fixed voltage (version dependent) to provide output regulation.

7.4.2 Operation With Low Input Voltage

The device requires up to 1.25-V headroom ($V_{IN} – V_{OUT}$) to operate in regulation. With less headroom, the device may dropout and OUTPUT voltage is equal to INPUT voltage minus the dropout voltage.

7.4.3 Operation at Light Loads

The device passes its bias current to the OUTPUT pin. The load or feeedback must consume this minimum current for regulation or the output may be too high.

7.4.4 Operation in Self Protection

When an overload occurs the device will shut down or reduce the output current to prevent device damage. The device will automatically reset from the overload. The output may be reduced or alternate between ON and OFF states until the overload is removed.

8 Application and Implementation

NOTE

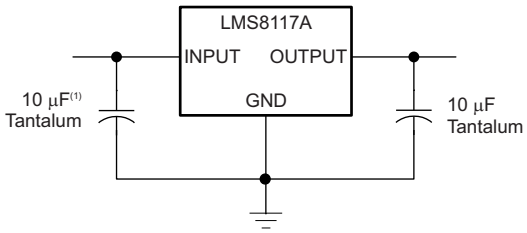
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LMS8117A is a versatile and high-performance linear regulator with a wide temperature range and tight line and load regulation operation. An output capacitor is required to further improve transient response and stability. For the adjustable version, the ADJUST pin can also be bypassed to achieve very high ripple-rejection ratios. The LMS8117A is versatile in its applications, including uses as a post regulator for DC-DC converters, batter chargers, and microprocessor supplies.

8.2 Typical Applications

8.2.1 Output Regulator



(1) Required if the regulator is placed far from the power supply filter.

Figure 12. Fixed Output Regulator

8.2.1.1 Design Requirements

The device component count is very minimal, employing two resistors as part of a voltage divider circuit for the adjustable version and an output capacitor for load regulation. A 10-µF tantalum capacitor on the input is suitable for almost all applications and is required if the regulator is located far from the power-supply filter. An optional bypass capacitor across R2 can also be used to improve PSRR.

8.2.1.2 Detailed Design Procedure

8.2.1.2.1 External Capacitors and Stability

8.2.1.2.1.1 Input Bypass Capacitor

TI recommends an input capacitor. A 10-µF tantalum on the input is a suitable input bypassing for almost all applications.

8.2.1.2.1.2 ADJUST Pin Bypass Capacitor

The ADJUST pin can be bypassed to ground with a bypass capacitor (C_{ADJ}) to improve ripple rejection. This bypass capacitor prevents ripple from being amplified as the output voltage is increased. At any ripple frequency, the impedance of the C_{ADJ} must be less than R1 to prevent the ripple from being amplified in Equation 1.

$$1 / (2 \times \pi \times f_{RIPPLE} \times C_{ADJ}) < R1 \quad (1)$$

The R1 is the resistor between the OUTPUT and the ADJUST pins. Its value is normally from 100 Ω to 200 Ω. For example, with R1 = 124 Ω and f_{RIPPLE} = 120 Hz, the C_{ADJ} must be > 11 µF.

Typical Applications (continued)

8.2.1.2.1.3 Output Capacitor

The output capacitor is critical in maintaining regulator stability, and must meet the required conditions for both minimum amount of capacitance and ESR (Equivalent Series Resistance). The minimum output capacitance required by the LMS8117A is 10 µF, if a tantalum capacitor is used. Any increase of the output capacitance merely improves the loop stability and transient response. The ESR of the output capacitor must be greater than 0.5 Ω and less than 5 Ω. In the case of the adjustable regulator, when the C_{ADJ} is used, a larger output capacitance (22-µF tantalum) is required.

8.2.1.2.2 Output Voltage

The LMS8117A adjustable version develops a 1.25-V reference voltage (V_{REF}) between the OUTPUT and the ADJUST pins. As shown in Figure 13, this voltage is applied across resistor R1 to generate a constant current I1. The current I_{ADJ} from the ADJUST pin could introduce error to the output. Because it is very small (60 µA) compared with the I1 and very constant with line and load changes, the error can be ignored. The constant current I1 then flows through the output set resistor R2 and sets the output voltage to the desired level.

For fixed voltage devices, R1 and R2 are integrated inside the devices.

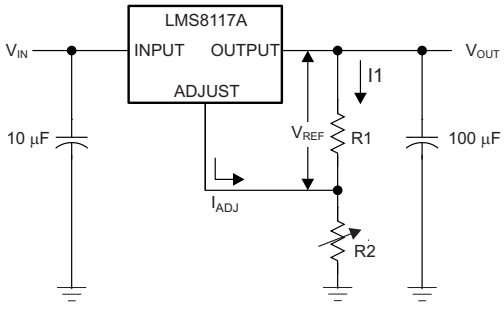


Figure 13. Basic Adjustable Regulator

V_{OUT} is calculated using Equation 2. I_{ADJ} is typically 60 µF and negligible in most applications.

$$V_{OUT} = V_{REF} \times (1 + R2 / R1) + (I_{ADJ} \times R2) \quad (2)$$

8.2.1.2.3 Load Regulation

The LMS8117A regulates the voltage that appears between its OUTPUT and GROUND pins, or between its OUTPUT and ADJUST pins. In some cases, line resistances can introduce errors to the voltage across the load. To obtain the best load regulation, a few precautions are required.

Figure 14 shows a typical application using a fixed output regulator. The R_T1 and R_T2 are the line resistances. It is obvious that the V_{LOAD} is less than the V_{OUT} by the sum of the voltage drops along the line resistances (as seen in Equation 3). In this case, the load regulation seen at the R_{LOAD} would be degraded from the data sheet specification. To improve this, the load must be tied directly to the OUTPUT pin on the positive side and directly tied to the GROUND pin on the negative side.

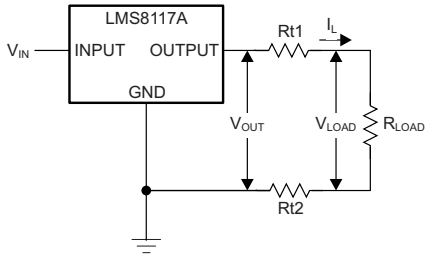


Figure 14. Basic Fixed Output Regulator

$$V_{LOAD} = V_{OUT} - I_L \times (R_T1 + R_T2) \quad (3)$$

Typical Applications (continued)

When the adjustable regulator is used (Figure 15), the best performance is obtained with the positive side of the resistor R1 tied directly to the OUTPUT pin of the regulator rather than near the load (as seen in Equation 4). This eliminates line drops from appearing effectively in series with the reference and degrading regulation. For example, a 5-V regulator with 0.05-Ω resistance between the regulator and load has a load regulation due to line resistance of 0.05 Ω × I_L. If R1 (125 Ω) is connected near the load, the effective line resistance is 0.05 Ω (1 + R2 / R1) or in this case, it is 4 times worse. In addition, the ground side of the resistor R2 can be returned near the ground of the load to provide remote ground sensing and improve load regulation.

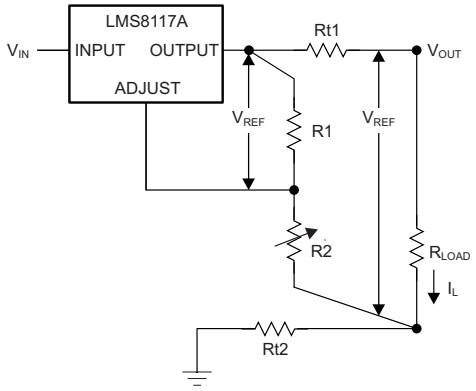


Figure 15. Best Load Regulation Using Adjustable Output Regulator

$$V_{LOAD} = V_{REF} \times (R1 + R2) / R1 – (I_L \times R_T1) \quad (4)$$

8.2.1.2.4 Protection Diodes

Under normal operation, the LMS8117A regulators do not require any protection diode. With the adjustable device, the internal resistance between the ADJUST and OUTPUT pins limit the current. No diode is required to divert the current around the regulator even with capacitor on the ADJUST pin. The ADJUST pin can take a transient signal of ±25 V with respect to the output voltage without damaging the device.

When a output capacitor is connected to a regulator and the input is shorted to ground, the output capacitor discharges into the output of the regulator. The discharge current depends on the value of the capacitor, the output voltage of the regulator, and rate of decrease of V_{IN}. In the LMS8117A regulators, the internal diode between the OUTPUT and INPUT pins can withstand microsecond surge currents of 10 A to 20 A. With an extremely large output capacitor (≥1000 µF), and with input instantaneously shorted to ground, the regulator could be damaged.

In this case, TI recommends an external diode between the OUTPUT and INPUT pins to protect the regulator, as shown in Figure 16.

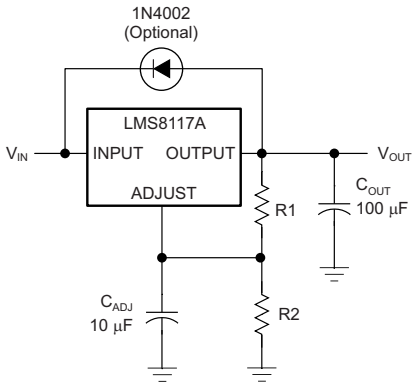
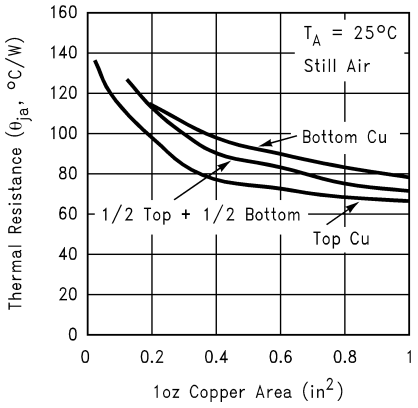


Figure 16. Regulator With Protection Diode

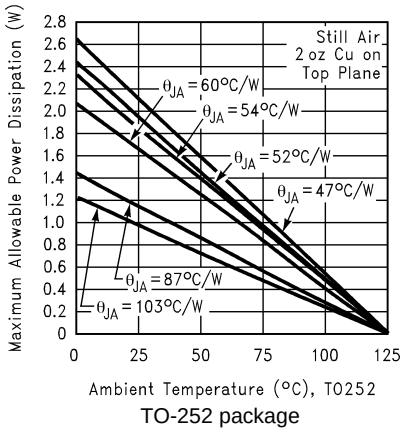
Typical Applications (continued)

8.2.1.3 Application Curves



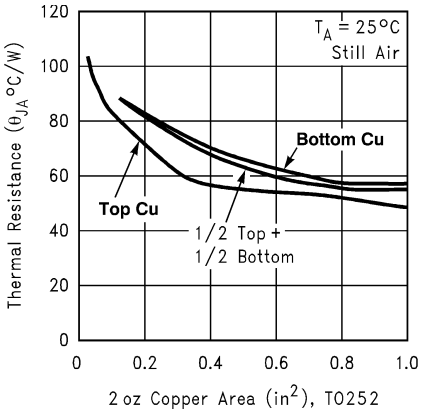
SOT-223 package

Figure 17. $R_{\theta JA}$ vs 1-oz Copper Area



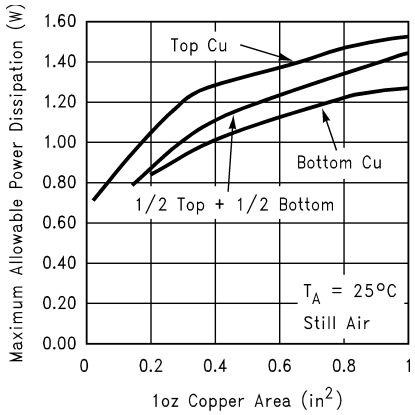
TO-252 package

Figure 18. $R_{\theta JA}$ vs 2-oz Copper Area



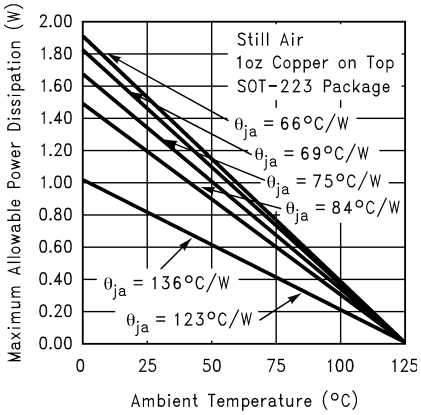
SOT-223 package

Figure 19. Maximum Allowable Power Dissipation vs Ambient Temperature



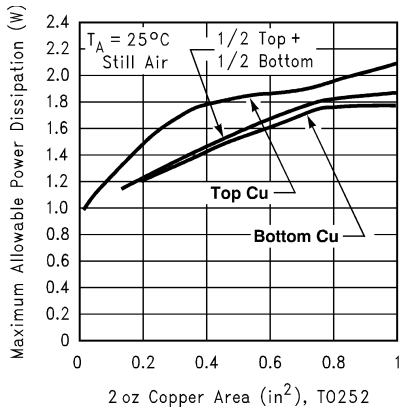
TO-252 package

Figure 20. Maximum Allowable Power Dissipation vs Ambient Temperature



SOT-223 package

Figure 21. Maximum Allowable Power Dissipation vs 1-oz Copper Area



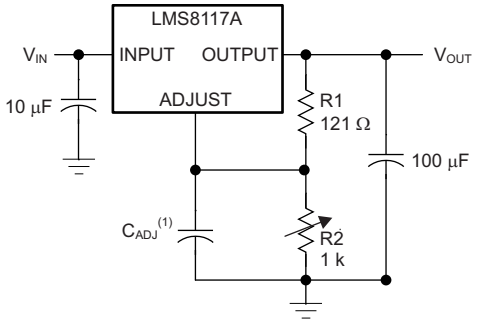
TO-252 package

Figure 22. Maximum Allowable Power Dissipation vs 2-oz Copper Area

Typical Applications (continued)

8.2.2 Other Application Circuits

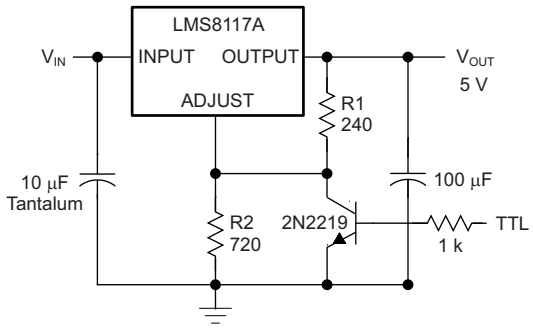
Figure 23 and Figure 24 show application circuit examples using the LMS8117A devices. Customers must fully validate and test any circuit before implementing a design based on an example in this section. Unless otherwise noted, the design procedures in *Output Regulator* are applicable.



(1) C_{ADJ} is optional, however it will improve ripple rejection.

Figure 23. 1.25-V to 10-V Adjustable Regulator With Improved Ripple Rejection

$$V_{OUT} = 1.25 \times (1 + R2 / R1) \quad (5)$$



(1) Minimum output is approximately 1.25 V.

Figure 24. 5-V Logic Regulator With Electronic Shutdown

9 Power Supply Recommendations

The input supply to the LMS8117A must be kept at a voltage level such that its maximum rating is not exceeded. The minimum dropout voltage must also be met, with extra headroom when possible, to keep the device in regulation. TI recommends an input capacitor; see *External Capacitors and Stability* for more information on capacitor selection.

10 Layout

10.1 Layout Guidelines

- TI recommends bypassing the input pin to ground with a bypass capacitor.
- The optimum placement of the bypass capacitor is as close as possible to the input pin and the system ground. Take care to minimize the loop area formed by the bypass capacitor connection, the input pin, and the system GND.
- TI recommends using wide trace lengths to eliminate I × R drop and heat dissipation.

10.2 Layout Example

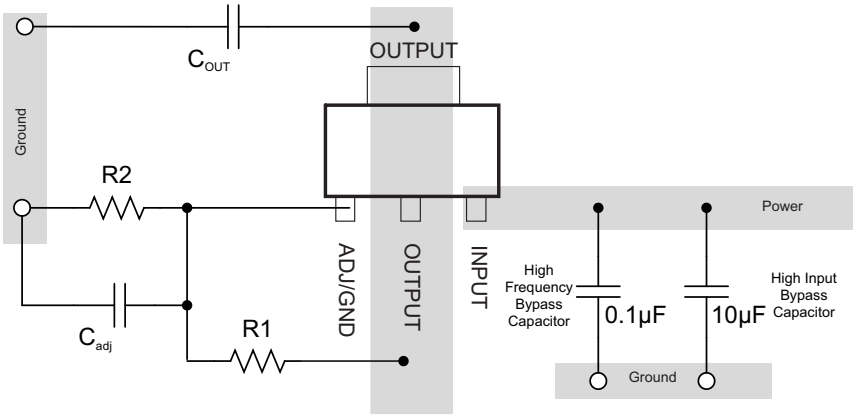


Figure 25. SOT-223 Layout Example for LMS8117A Adjustable Version (Schematic View)

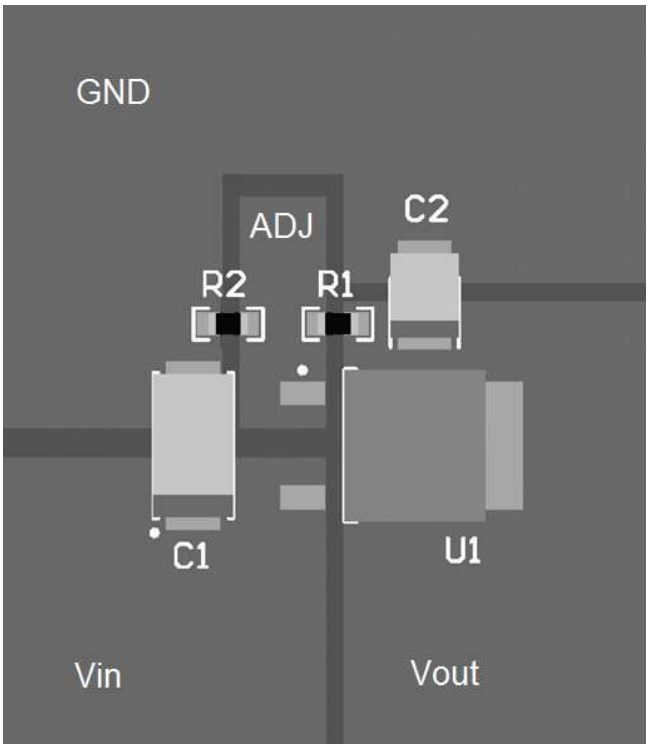


Figure 26. TO-252 Layout Example for LMS8117A Adjustable Version (PCB View)

10.3 Thermal Considerations

10.3.1 Heat Sink Requirements

When an integrated circuit operates with an appreciable current, its junction temperature is elevated. It is important to quantify its thermal limits to achieve acceptable performance and reliability. This limit is determined by summing the individual parts consisting of a series of temperature rises from the semiconductor junction to the operating environment. A one-dimensional steady-state model of conduction heat transfer is demonstrated in Figure 27. The heat generated at the device junction flows through the die to the die attach pad, through the lead frame to the surrounding case material, to the printed-circuit board, and eventually to the ambient environment.

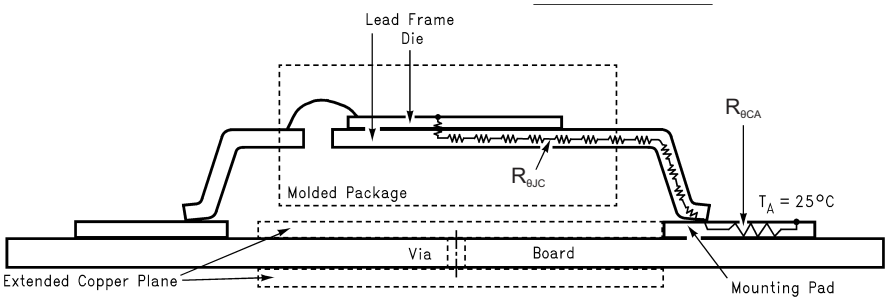
There are several variables that may affect the thermal resistance and in turn the need for a heat sink, which include the following.

Component variables ($R_{\theta JC}$)

- Leadframe size and material
- Number of conduction pins
- Die size
- Die attach material
- Molding compound size and material

Application variables ($R_{\theta CA}$)

- Mounting pad size, material, and location
- Placement of mounting pad
- PCB size and material
- Traces length and width
- Adjacent heat sources
- Volume of air
- Ambient temperature
- Shape of mounting pad



The case temperature is measured at the point where the leads contact the mounted pad surface.

Figure 27. Cross-Sectional View of Integrated Circuit Mounted on a Printed-Circuit Board

The LMS8117A regulator has internal thermal shutdown to protect the device from overheating. Under all possible operating conditions, the junction temperature of the LMS8117A must be within 0°C to 125°C. A heat sink may be required depending on the maximum power dissipation and maximum ambient temperature of the application. To determine if a heat sink is required, the power dissipated by the regulator (P_D) is calculated using Equation 6.

$$I_{IN} = I_L + I_G \quad (6)$$

$$P_D = (V_{IN} - V_{OUT}) \times I_L + (V_{IN} \times I_G) \quad (7)$$

Figure 28 shows the voltages and currents which are present in the circuit.

Thermal Considerations (continued)

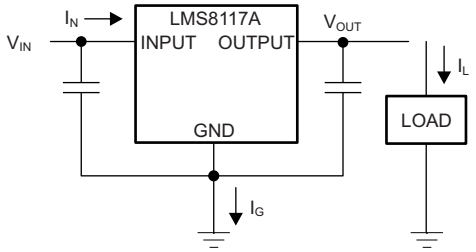


Figure 28. Power Dissipation Diagram

The next parameter which must be calculated is the maximum allowable temperature rise ($T_{R(MAX)}$) in Equation 8.

$$T_{R(MAX)} = T_{J(MAX)} - T_{A(MAX)}$$

where

- $T_{J(MAX)}$ is the maximum allowable junction temperature (125°C)
- $T_{A(MAX)}$ is the maximum ambient temperature encountered in the application (8)

Using the calculated values for $T_{R(MAX)}$ and P_D, the maximum allowable value for the junction-to-ambient thermal resistance ($R_{\theta JA}$) can be calculated with Equation 9.

$$R_{\theta JA} = T_{R(MAX)} / P_D \quad (9)$$

If the maximum allowable value for $R_{\theta JA}$ is found to be ≥61.4°C/W for SOT-223 package or ≥56.1°C/W for TO-252 package, no heat sink is required because the package alone dissipates enough heat to satisfy these requirements. If the calculated value for $R_{\theta JA}$ falls below these limits, a heat sink is required.

As a design aid, Table 1 shows the value of the $R_{\theta JA}$ of SOT-223 and TO-252 for different heat sink area. The copper patterns that we used to measure these $R_{\theta JA}$ are shown Figure 29 and Figure 30. Figure 17 and Figure 18 reflect the same test results as what are in the Table 1.

Figure 19 and Figure 20 show the maximum allowable power dissipation versus ambient temperature for the SOT-223 and TO-252 device packages. Figure 21 and Figure 22 show the maximum allowable power dissipation versus copper area ($in.^2$) for the SOT-223 and TO-252 device packages. For power enhancement techniques to be used with SOT-223 and TO-252 packages, see *AN–1028 Maximum Power Enhancement Techniques for Power Packages* (SNVA036).

Table 1. $R_{\theta JA}$ Different Heat Sink Area

LAYOUT	COPPER AREA (in^2)		THERMAL RESISTANCE: $R_{\theta JA}$ (°C/W)	
	TOP SIDE(1)	BOTTOM SIDE	SOT-223	T0-252
1	0.0123	0	136	103
2	0.066	0	123	87
3	0.3	0	84	60
4	0.53	0	75	54
5	0.76	0	96	52
6	1	0	66	47
7	0	0.2	115	64
8	0	0.4	98	70
9	0	0.6	89	63
10	0	0.8	82	57
11	0	1	79	57
12	0.066	0.066	125	89
13	0.175	0.175	93	72

(1) Tab of device is attached to top-side copper.

Thermal Considerations (continued)

Table 1. $R_{\theta JA}$ Different Heat Sink Area (continued)

LAYOUT	COPPER AREA (in^2)		THERMAL RESISTANCE: $R_{\theta JA}$ (°C/W)	
	TOP SIDE(1)	BOTTOM SIDE	SOT-223	T0-252
14	0.284	0.284	83	61
15	0.392	0.392	75	55
16	0.5	0.5	70	53

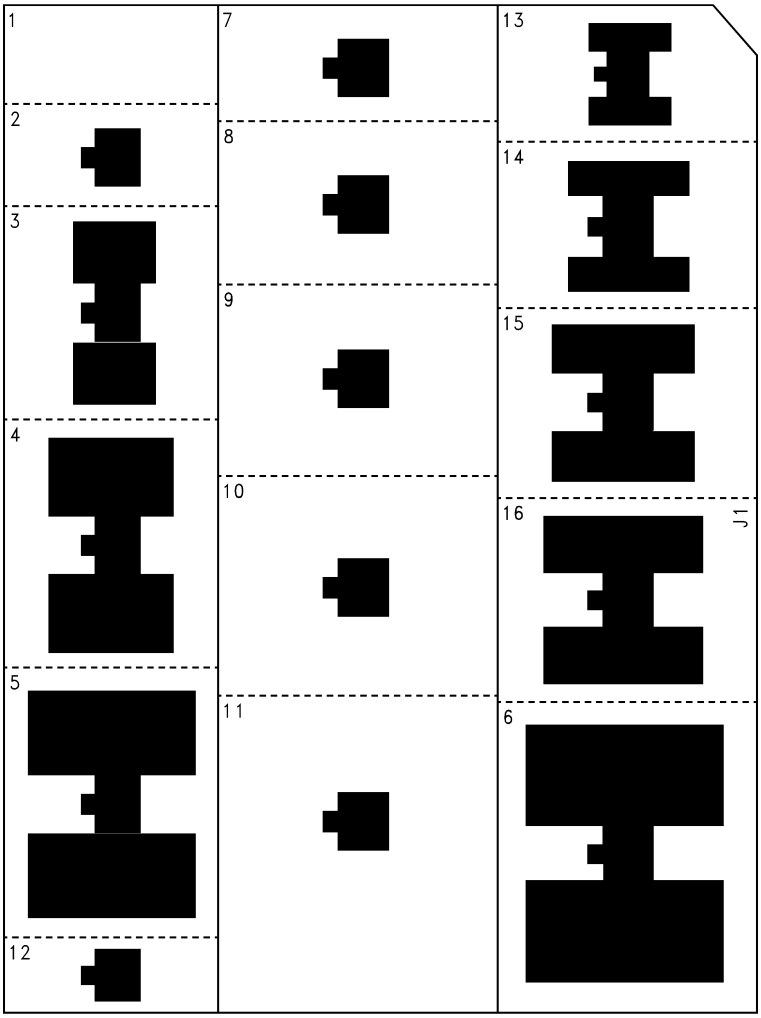


Figure 29. Top View of the Thermal Test Pattern in Actual Scale

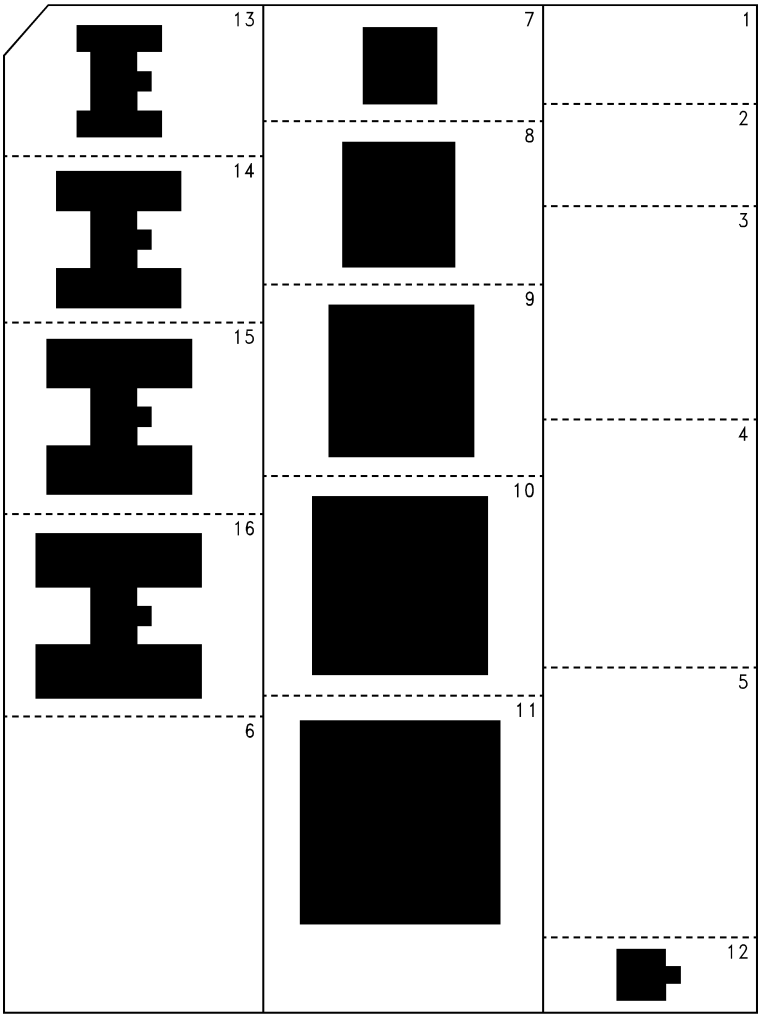


Figure 30. Bottom View of the Thermal Test Pattern in Actual Scale

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following:

AN–1028 Maximum Power Enhancement Techniques for Power Packages (SNVA036)

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

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All other trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMS8117ADT-3.3/NOPB	ACTIVE	TO-252	NDP	3	75	RoHS & Green	SN	Level-2-260C-1 YEAR	0 to 125	LMS8117 ADT-3.3	Samples
LMS8117ADT-ADJ/NOPB	ACTIVE	TO-252	NDP	3	75	RoHS & Green	SN	Level-2-260C-1 YEAR	0 to 125	LMS8117 ADT-ADJ	Samples
LMS8117ADTX-3.3/NOPB	ACTIVE	TO-252	NDP	3	2500	RoHS & Green	SN	Level-2-260C-1 YEAR	0 to 125	LMS8117 ADT-3.3	Samples
LMS8117ADTX-ADJ/NOPB	ACTIVE	TO-252	NDP	3	2500	RoHS & Green	SN	Level-2-260C-1 YEAR	0 to 125	LMS8117 ADT-ADJ	Samples
LMS8117AMP-1.8/NOPB	ACTIVE	SOT-223	DCY	4	1000	RoHS & Green	SN	Level-1-260C-UNLIM	0 to 125	LS00	Samples
LMS8117AMP-3.3/NOPB	ACTIVE	SOT-223	DCY	4	1000	RoHS & Green	SN	Level-1-260C-UNLIM	0 to 125	LS01	Samples
LMS8117AMP-ADJ/NOPB	ACTIVE	SOT-223	DCY	4	1000	RoHS & Green	SN	Level-1-260C-UNLIM	0 to 125	LS0A	Samples
LMS8117AMPX-1.8/NOPB	ACTIVE	SOT-223	DCY	4	2000	RoHS & Green	SN	Level-1-260C-UNLIM	0 to 125	LS00	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

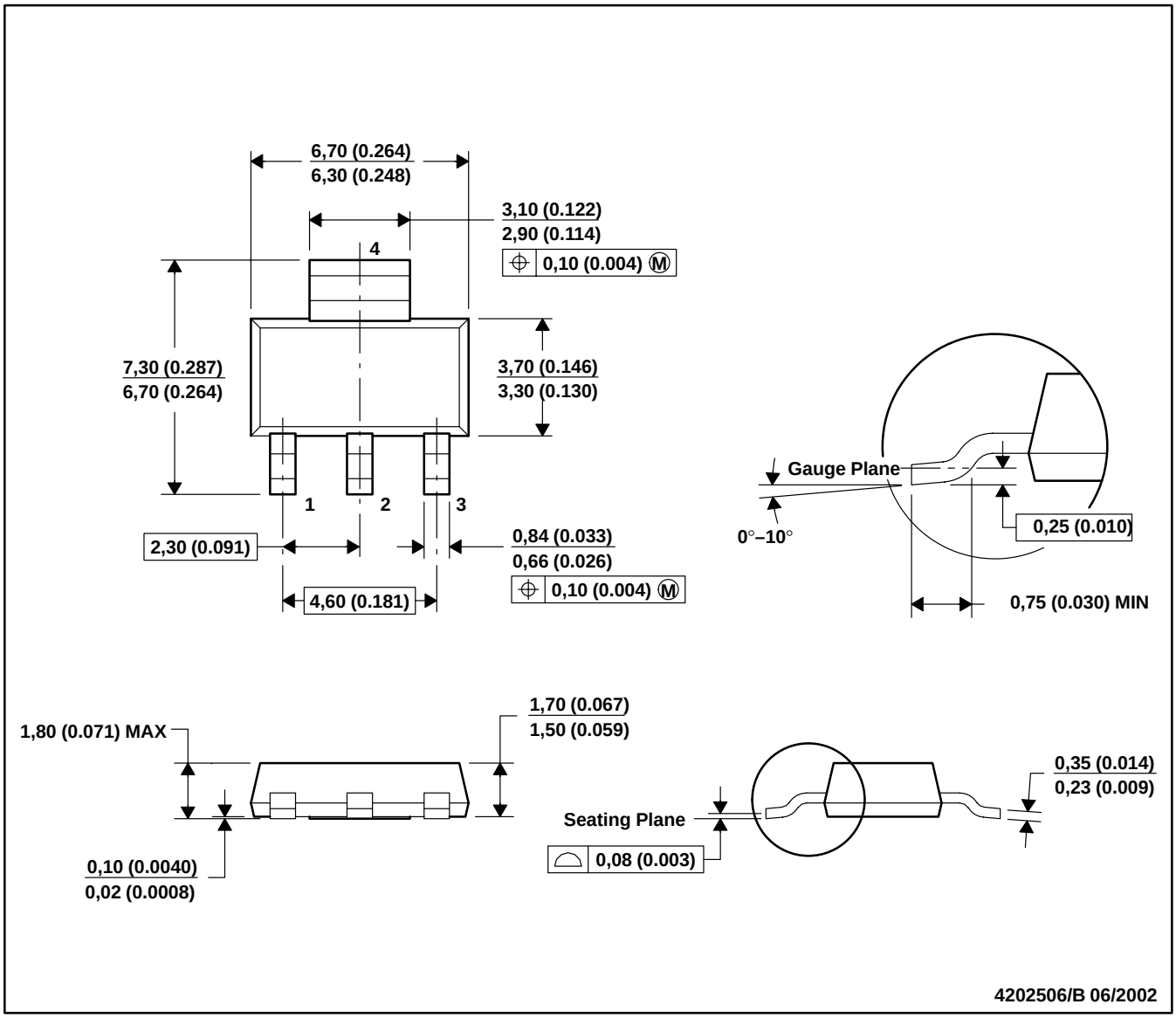
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

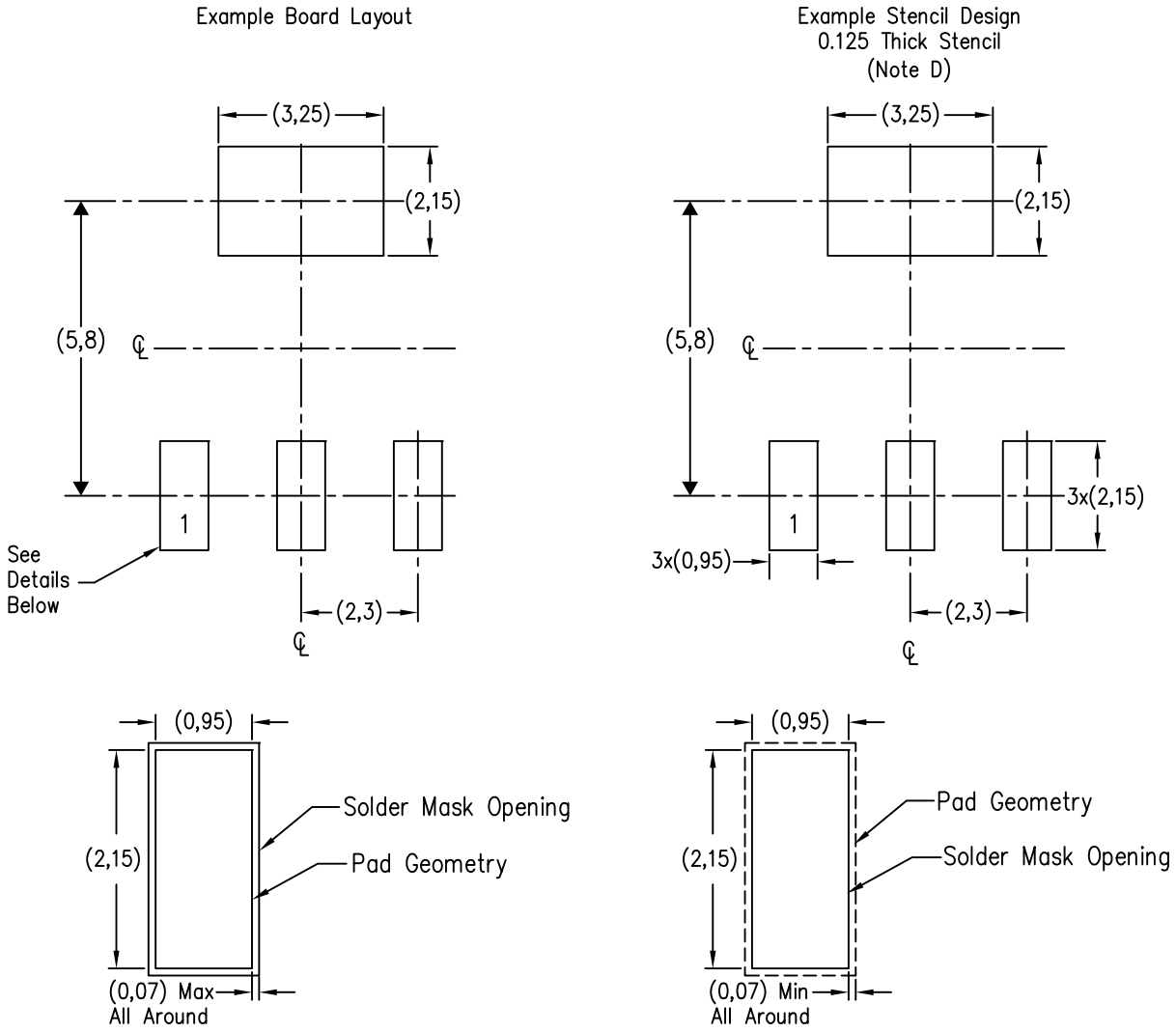
MPDS094A – APRIL 2001 – REVISED JUNE 2002

DCY (R-PDSO-G4) **PLASTIC SMALL-OUTLINE**



NOTES: A. All linear dimensions are in millimeters (inches).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC TO-261 Variation AA.

DCY (R–PDSO–G4) PLASTIC SMALL OUTLINE



NOTES:

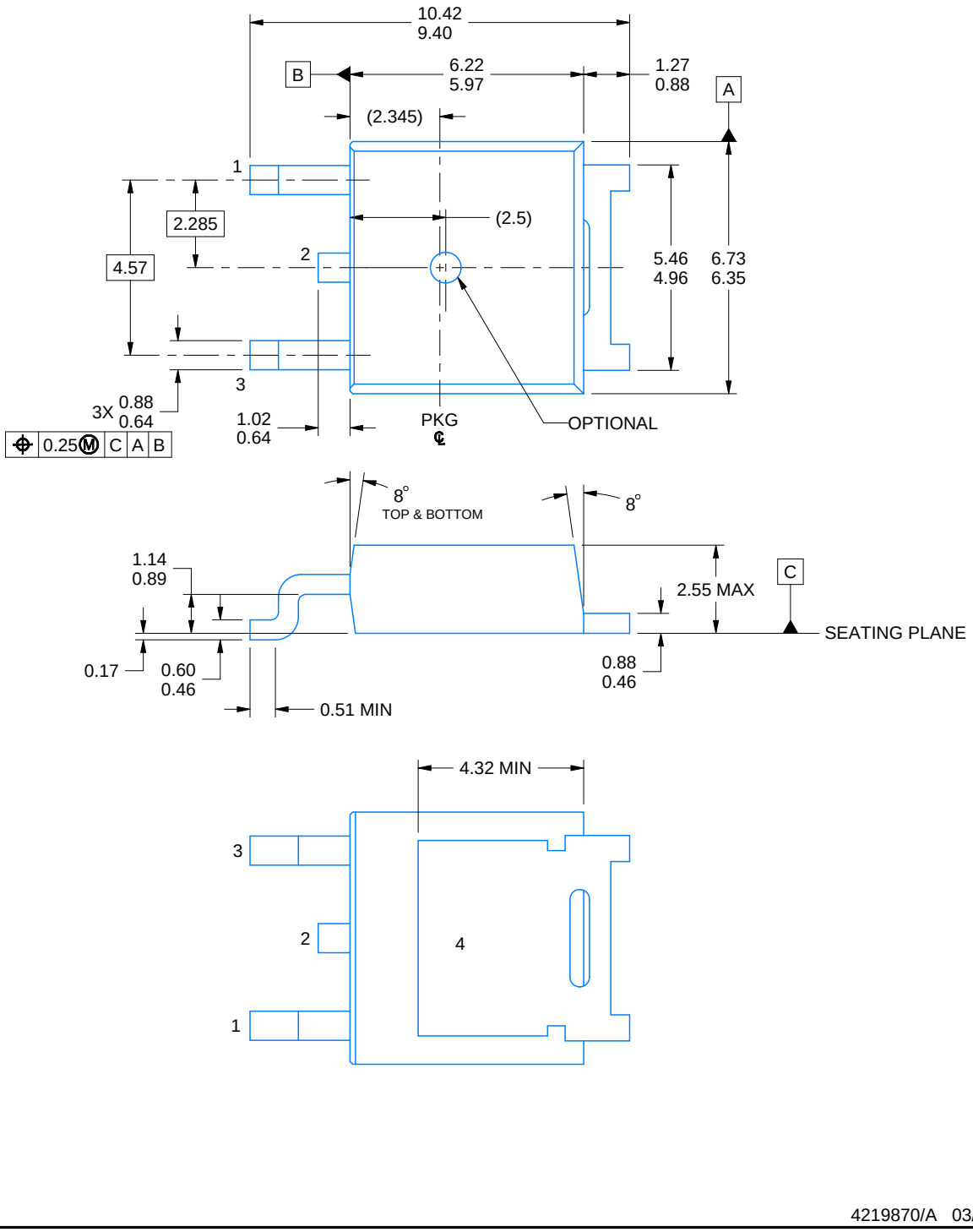
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil recommendations. Refer to IPC 7525 for stencil design considerations.

NDP0003B

PACKAGE OUTLINE

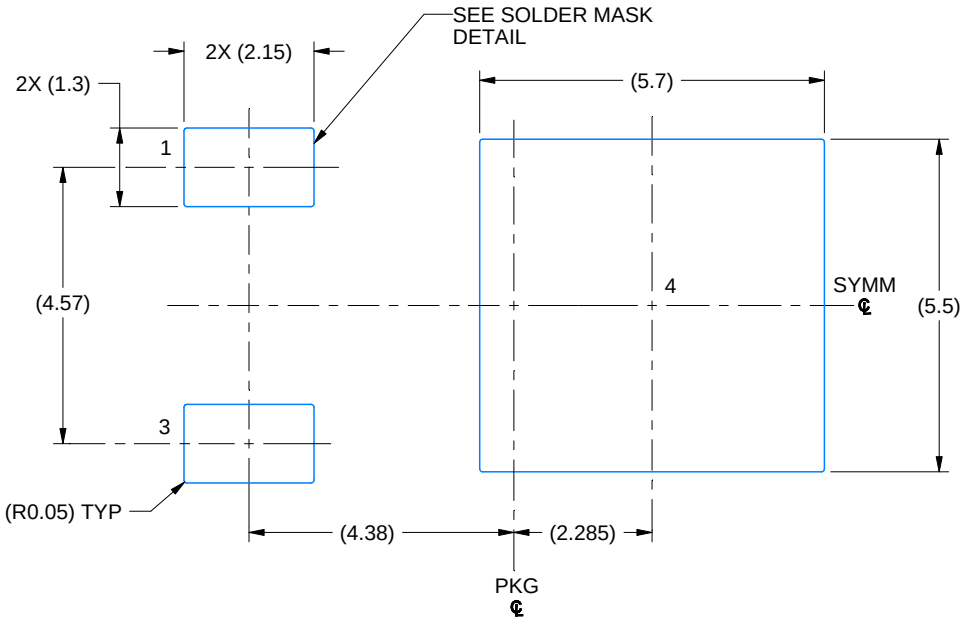
TO-252 - 2.55 mm max height

TRANSISTOR OUTLINE

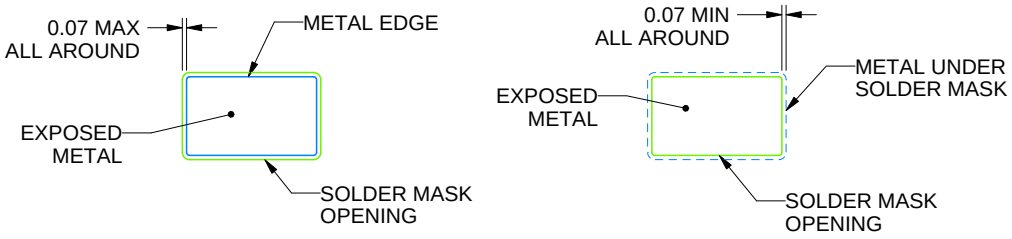


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration TO-252.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 8X

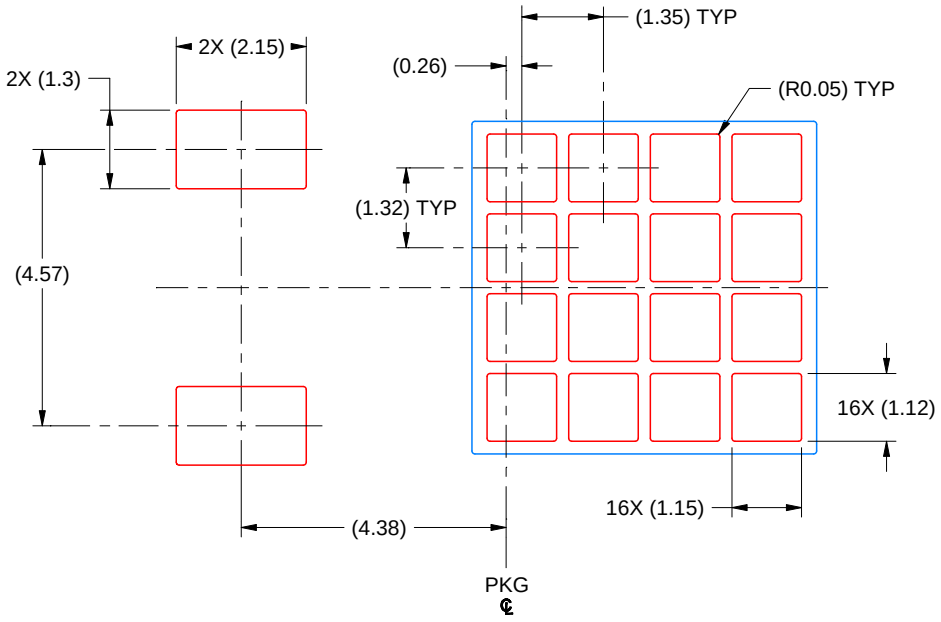


SOLDER MASK DETAIL

4219870/A 03/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002(www.ti.com/lit/slm002) and SLMA004 (www.ti.com/lit/slma004).
5. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 8X

4219870/A 03/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

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