LP3981 Micropower, 300-mA Ultra-Low-Dropout CMOS Voltage Regulator

1 Features

- 2.5-V to 6-V Input Range
- 300-mA Output Current
- 60-dB PSRR at 1 kHz
- ≤ 1-µA Quiescent Current When Shut Down
- Fast Turnon Time: 120 µs (typical) with C_{BYPASS} = 0.01 µF
- 132-mV Typical Dropout with 300-mA Load
- 35-µVrms Output Noise Over 10 Hz to 100 kHz
- Logic Controlled Enable
- Stable With Ceramic and High-Quality Tantalum Capacitors
- Thermal Shutdown and Short-Circuit Current Limit
- Low Thermal Resistance in WSON-6 Package Gives Excellent Power Capability

2 Applications

- CDMA Cellular Handsets
- Wideband CDMA Cellular Handsets
- GSM Cellular Handsets
- Portable Information Appliances

3 Description

Performance of the LP3981 device is optimized for battery-powered systems to deliver ultra-low-noise, extremely low dropout voltage, and low quiescent current. Regulator ground current increases only slightly in dropout, further prolonging the battery life.

Power supply rejection is better than 60 dB at low frequencies. This high power supply rejection is maintained down to lower input voltage levels common to battery-operated circuits.

The device is ideal for mobile phone and similar battery-powered wireless applications. It provides up to 300 mA, from a 2.5-V to 6-V input, consuming less than 1 µA in disable mode.

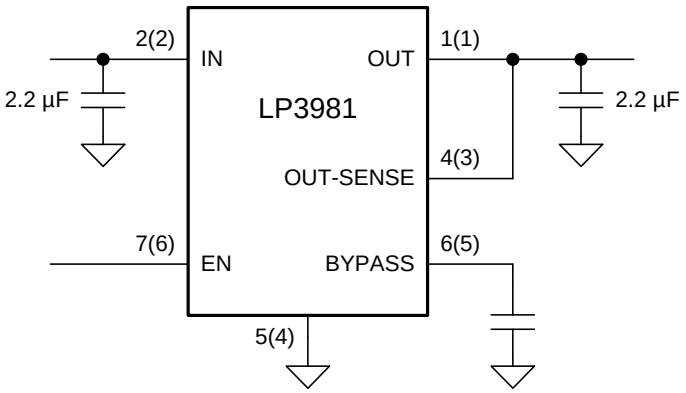
The LP3981 is available in 8-pin VSSOP-8 and 6-pin WSON packages. Performance is specified for −40°C to +125°C temperature range. The device available in the following output voltages: 2.5 V, 2.7 V, 2.8 V, 2.83 V, 3 V, 3.03 V and 3.3 V as standard. Other output options can be made available; contact your local TI sales office for more information.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LP3981	WSON (6)	4.00 mm x 3.00 mm
	VSSOP (8)	3.00 mm x 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application Circuit



Note: Pin numbers in parenthesis indicate WSON package.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision G (May 2013) to Revision H **Page**

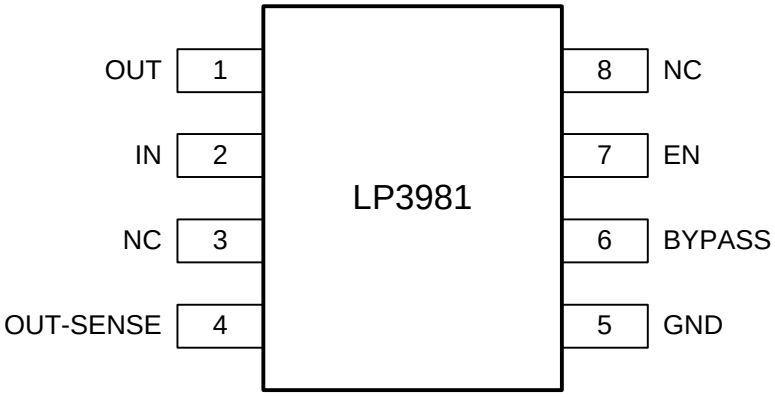
- Added *Device Information* and *Pin Configuration and Functions* sections, ESD Rating table, *Feature Description*, *Device Functional Modes*, *Application and Implementation*, *Power Supply Recommendations*, *Layout*, *Device and Documentation Support* , and *Mechanical, Packaging, and Orderable Information* sections ... 1
- Update pin names to TI nomenclature ... 1
- Deleted Ordering Information table - duplicative of POA ... 1
- Deleted Lead temperature spec from Abs Max table - it is in POA. ... 4
- Deleted rows for max power dissipation - info in *Power Dissipation and Device Operation* ... 4
- Deleted rows for max power dissipation - info in *Power Dissipation and Device Operation* ... 4
- Added 2 new paragraphs to *Power Dissipation and Device Operation* subsection. ... 13

Changes from Revision F (May 2013) to Revision G **Page**

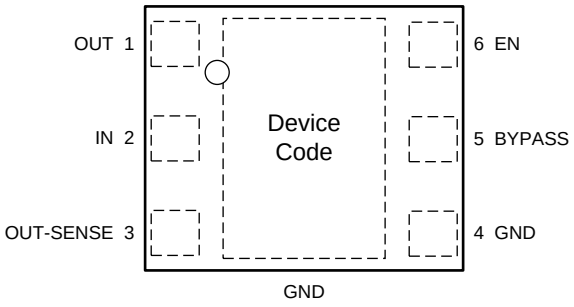
- Changed layout of National Data Sheet to TI format ... 10

5 Pin Configuration and Functions

DGK Package
8-Pin VSSOP
Top View



NGC Package
6-Pin WSON With Exposed Thermal Pad
Top View



Pin Descriptions

PIN			TYPE	DESCRIPTION
NAME	VSSOP	WSON		
BYPASS	6	5	—	Optional bypass capacitor for noise reduction.
EN	7	6	I	Enable input logic, enable high.
GND	5	4	G	Common ground. Connect to PAD.
IN	2	2	I	Input voltage of the LDO.
NC	3, 8	—	—	No internal connection.
OUT	1	1	O	Output voltage of the LDO.
OUT-SENSE	4	3	O	Output. Voltage sense pin. Must be connected to OUT for proper operation.
THERMAL PAD	—	√	—	Common ground. Connect to pin 4.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)(3)

	MIN	MAX	UNIT
IN, EN	−0.3	6.5	V
OUT, OUT-SENSE	−0.3 to V_{IN} + 0.3	6.5	V
Junction temperature		150	°C
Storage temperature, T_{stg}	−65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to the potential at the GND pin.
(3) If Military/Aerospace specified devices are required, contact the TI Sales Office/Distributors for availability and specifications.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Machine model	±200	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)(2)

	MIN	NOM	MAX	UNIT
V_{IN}	2.7		6	V
V_{EN}	0		V_{IN}	V
Junction temperature	–40		125	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to the potential at the GND pin.

6.4 Thermal Information

THERMAL METRIC(1)		LP3981		UNIT
		DGK (VSSOP)	NGC (WSON)	
		8 PINS	6 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance, High K	177	56.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	67.7	76.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	97.4	30.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	10.8	3.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	96	31	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	10.7	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

Unless otherwise specified: V_{EN} = 1.2 V, V_{IN} = V_{OUT} + 0.5 V, C_{IN} = 2.2 µF, C_{BP} = 0.033 µF, I_{OUT} = 1 mA, C_{OUT} = 2.2 µF. All values are for T_J = 25°C, unless otherwise specified.(1)(2)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ΔV_{OUT}	Output voltage tolerance		−2		2	% of $V_{OUT(nom)}$
		T_J = –40°C to +125°C	–3		3	
	Line regulation error	V_{IN} = V_{OUT} + 0.5 V to 6 V, T_A < 85°C	−0.1	0.005	0.1	%/V
		V_{IN} = V_{OUT} + 0.5 V to 6 V, T_J ≤125°C	–0.2		0.2	
	Load regulation error(3)	I_{OUT} = 1 mA to 300 mA		0.0003		%/mA
		I_{OUT} = 1 mA to 300 mA T_J = –40°C to +125°C			0.005	
PSRR	Power supply rejection ratio(4)	V_{IN} = $V_{OUT(nom)}$ + 1 V, f = 1 kHz, I_{OUT} = 50 mA (Figure 16)		50		dB
		V_{IN} = $V_{OUT(nom)}$ + 1 V, f = 10 kHz, I_{OUT} = 50 mA (Figure 16)		55		
I_Q	Quiescent current	V_{EN} = 1.2 V, I_{OUT} = 1 mA		70		µA
		V_{EN} = 1.2 V, I_{OUT} = 1 mA T_J = –40°C to +125°C			120	
		V_{EN} = 1.2 V, I_{OUT} = 1 mA to 300 mA, V_{OUT} = 2.5 V(5)		170		
		V_{EN} = 1.2 V, I_{OUT} = 1 mA to 300 mA, V_{OUT} = 2.5 V T_J = –40°C to +125°C(5)			210	
		V_{EN} = 0.4 V		0.003		
		V_{EN} = 0.4 V, T_J = –40°C to +125°C			1.5	
	Dropout voltage (6)	I_{OUT} = 1 mA		0.5		mV
		I_{OUT} = 1 mA, T_J = –40°C to +125°C			5	
		I_{OUT} = 200 mA		88		
		I_{OUT} = 200 mA, T_J = –40°C to +125°C			133	
		I_{OUT} = 300 mA		132		
		I_{OUT} = 300 mA, T_J = –40°C to +125°C			200	
I_{SC}	Short-circuit current limit	Output grounded (steady state)		600		mA
e_n	Output noise voltage	BW = 10 Hz to 100 kHz, C_{BP} = 0.033 µF		35		μV_{RMS}
T_{SD}	Thermal shutdown temperature			160		°C
	Thermal shutdown hysteresis			20		
$I_{OUT(PK)}$	Peak output current	V_{OUT} ≥ V_{OUT} (nom) – 5%	300	455		mA
I_{EN}	Maximum input current at V_{EN}	V_{EN} = 0 and V_{IN}		0.001		µA
V_{IL}	Logic low input threshold	V_{IN} = 2.7 V to 6 V, T_J = –40°C to +125°C			0.4	
V_{IH}	Logic high input threshold	V_{IN} = 2.7 V to 6 V, T_J = –40°C to +125°C	1.4			

(1) Minimum (MIN) and maximum (MAX) limits are ensured by design, test, or statistical analysis. Typical (TYP) numbers are not verified, but do represent the most likely norm.
(2) The target output voltage, which is labeled $V_{OUT(nom)}$, is the desired voltage option.
(3) An increase in the load current results in a slight decrease in the output voltage and vice versa.
(4) Specified by design. Not production tested.
(5) For V_{OUT} > 2.5 V, increase $I_{Q(MAX)}$ by 2.5 µA for every 0.1 V increase in $V_{OUT(nom)}$; that is, $I_{Q(MAX)}$ = 210 µA + (($V_{OUT(NOM)}$ – 2.5) × 25) µA .
(6) Dropout voltage is the input-to-output voltage difference at which the output voltage is 100 mV below its nominal value. This specification does not apply for input voltages below 2.5 V.

Electrical Characteristics (continued)

Unless otherwise specified: V_{EN} = 1.2 V, V_{IN} = V_{OUT} + 0.5 V, C_{IN} = 2.2 µF, C_{BP} = 0.033 µF, I_{OUT} = 1 mA, C_{OUT} = 2.2 µF. All values are for T_J = 25°C, unless otherwise specified.(1)(2)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT CAPACITANCE						
C_{OUT}	Output capacitor	Capacitance	2.2		22	µF
		ESR	5		500	mΩ

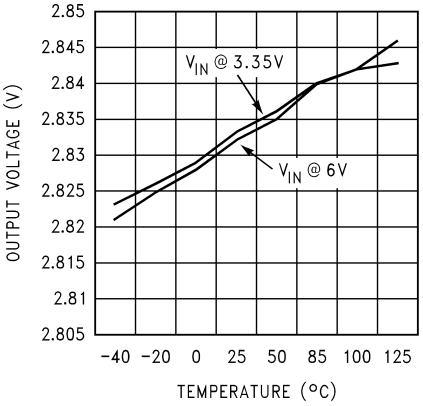
6.6 Timing Requirements

		MIN	NOM	MAX	UNIT
t_{ON}	Turnon time (1) (2) C_{BYPASS} = 0.033 µF	240			µs
	C_{BYPASS} = 0.033 µF, T_J = –40°C to +125°C			350	

(1) Specified by design. Not production tested.
(2) Turnon time is time measured between the enable input just exceeding V_{IH} and the output voltage just reaching 95% of its nominal value.

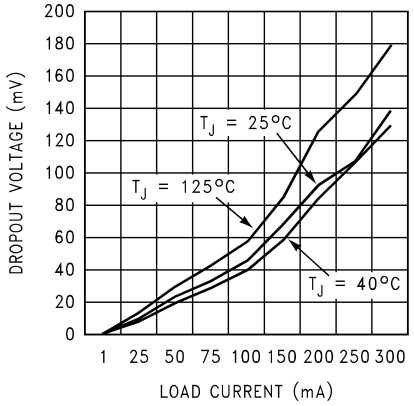
6.7 Typical Characteristics

Unless otherwise specified, $C_{IN} = C_{OUT} = 2.2\ \mu F$ ceramic, $C_{BP} = 0.033\ \mu F$, $V_{IN} = V_{OUT} + 0.5\ V$, $T_A = 25°C$, EN pin is tied to V_{IN}.



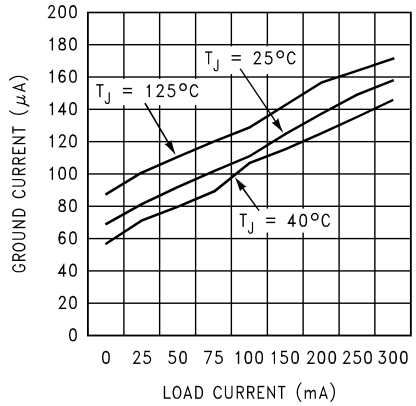
V_{OUT} = 2.83 V

Figure 1. Output Voltage vs. Temperature



V_{OUT} = 2.85 V

Figure 2. Dropout Voltage vs. Temperature



V_{OUT} = 2.85 V

Figure 3. Ground Current vs. Load Current

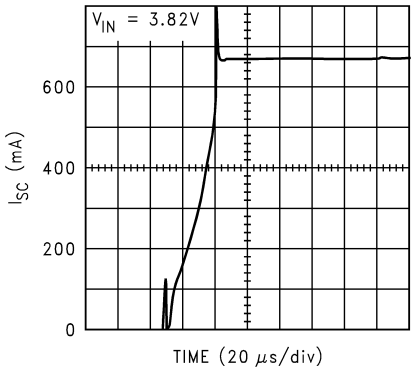


Figure 4. Output Short Circuit Current

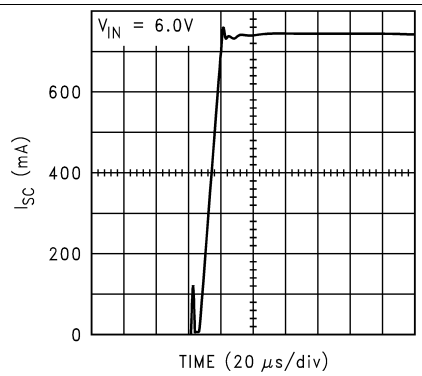
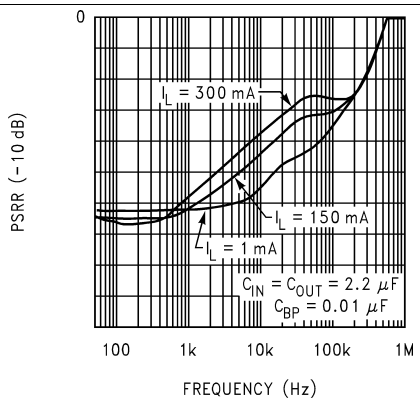


Figure 5. Output Short Circuit Current

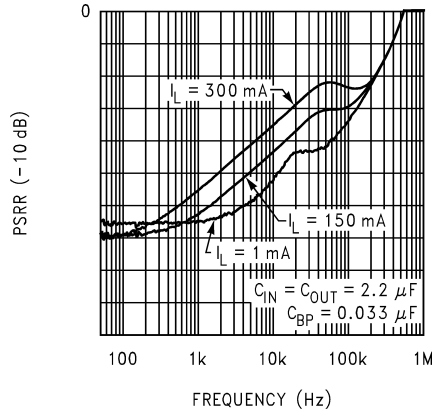


$V_{IN} = V_{OUT} + 1\ V$

Figure 6. Ripple Rejection

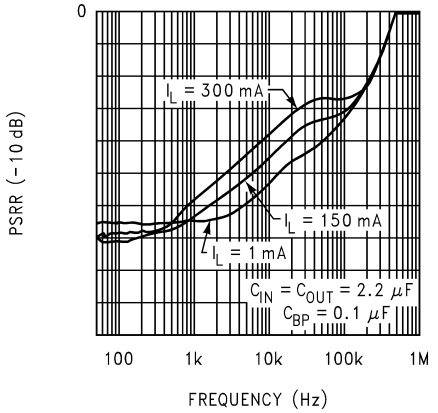
Typical Characteristics (continued)

Unless otherwise specified, $C_{IN} = C_{OUT} = 2.2\ \mu F$ ceramic, $C_{BP} = 0.033\ \mu F$, $V_{IN} = V_{OUT} + 0.5\ V$, $T_A = 25°C$, EN pin is tied to V_{IN}.



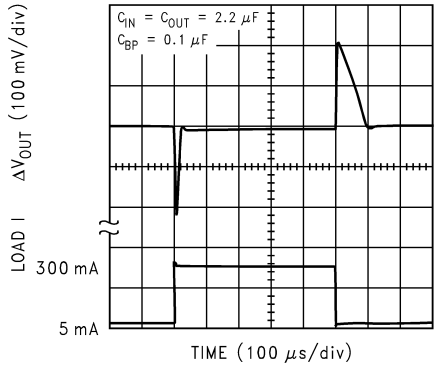
$V_{IN} = V_{OUT} + 1\ V$

Figure 7. Ripple Rejection



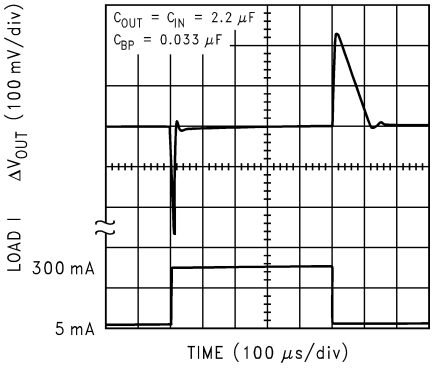
$V_{IN} = V_{OUT} + 1\ V$

Figure 8. Ripple Rejection



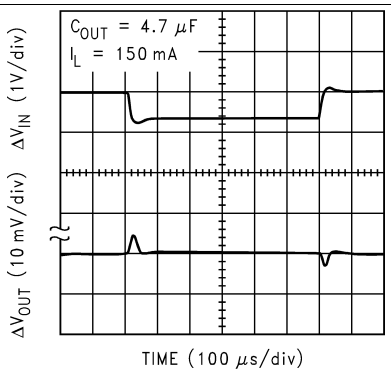
$V_{IN} = 3.5\ V$

Figure 9. Load Transient Response



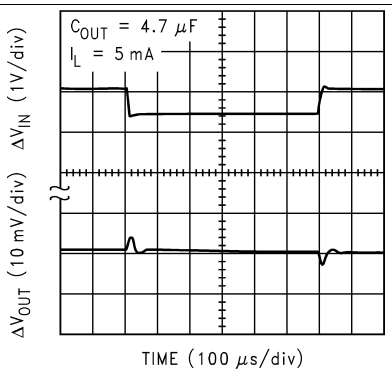
$V_{IN} = 3.5\ V$

Figure 10. Load Transient Response



$V_{IN} = V_{OUT} + 1\ V$ To $V_{OUT} + 1.6\ V$

Figure 11. Line Transient Response



$V_{IN} = V_{OUT} + 1\ V$ to $V_{OUT} + 1.6\ V$

Figure 12. Line Transient Response

Typical Characteristics (continued)

Unless otherwise specified, $C_{IN} = C_{OUT} = 2.2$ µF ceramic, $C_{BP} = 0.033$ µF, $V_{IN} = V_{OUT} + 0.5$ V, $T_A = 25°C$, EN pin is tied to V_{IN}.

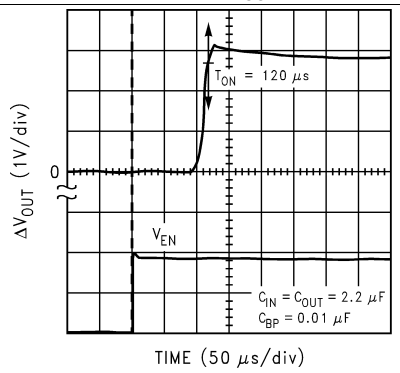


Figure 13. Enable Response (t_{ON})

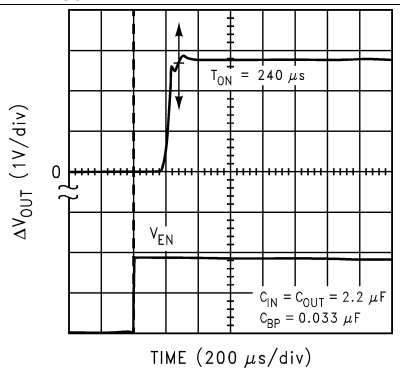


Figure 14. Enable Response (t_{ON})

7 Parameter Measurement Information

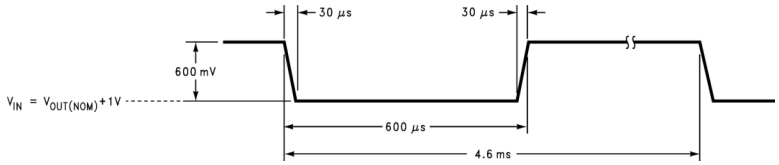


Figure 15. Line Transient Response Input Perturbation

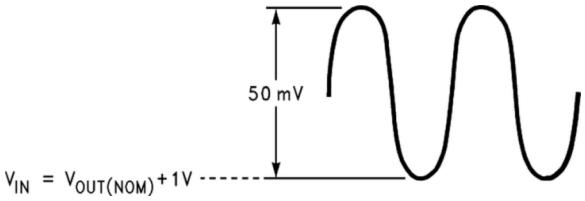


Figure 16. PSRR Input Perturbation

8 Detailed Description

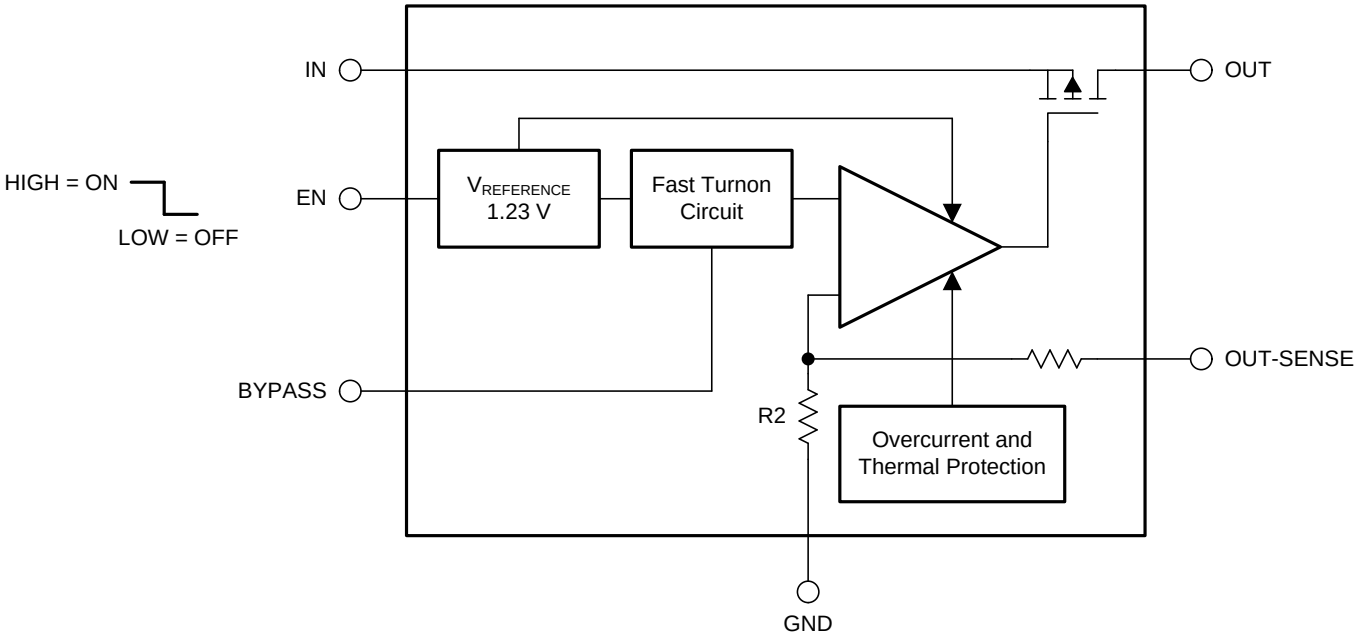
8.1 Overview

The LP3981 family of fixed-output, ultra-low-dropout, and low-noise regulators offers exceptional performance for battery-powered applications. Available for voltages from 2.5-V to 3.3-V, the family is capable of delivering 300-mA continuous load current.

The LP3981 contains several features to facilitate battery-powered designs:

- Low dropout voltage , typical dropout of 132-mV at 300-mA load current.
- Low quiescent current and low ground current. Ground current is typically 170 µA at 150-mA load, and 70 µA at 1-mA load.
- A shutdown feature is available , allowing the regulator to consume only 0.003 µA typically when the EN pin is pulled low.
- Power supply rejection is 60-dB at 1 kHZ.
- Low noise; BYPASS pin allows for low-noise operation, with typically 35-μV_{RMS} output noise over 10 Hz to 100 kHz.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 On/Off Input Operation

The LP3981 is turned off by pulling the EN pin low, and turned on by pulling it high. If this feature is not used, the EN pin must be tied to V_{IN} to keep the regulator output on at all time. To assure proper operation, the signal source used to drive the EN input must be able to swing above and below the specified turnon and turnoff voltage thresholds listed in *Electrical Characteristics* under V_{IL} and V_{IH}.

8.3.2 Fast On-Time

The LP3981 utilizes a speed up circuitry to ramp up the internal V_{REF} voltage to its final value to achieve a fast output turn on time.

8.4 Device Functional Modes

8.4.1 Operation with $V_{OUT(TARGET)}$ + 0.3 V ≤ V_{IN} ≤ 6 V

The device operate if the input voltage is equal to, or exceeds $V_{OUT(TARGET)}$ + 0.3 V. At input voltages below the minimum V_{IN} requirement, the devices do not operate correctly and output voltage may not reach target value.

8.4.2 Operation With EN Control

If the voltage on the EN pin is less than 0.4 V, the device is disabled, and in this state the shutdown current does not exceed 1.5 µA. Raising EN above 1.4 V initiates the start-up sequence of the device.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers must validate and test their design implementation to confirm system functionality.

9.1 Application Information

The LP3981 can provide 300-mA output current with 2.5-V to 6-V input. It is stable with a 2.2-µF ceramic output capacitor. An optional external bypass capacitor reduces the output noise without slowing down the load transient response. Typical output noise is 35 μV_{RMS} at frequencies from 10 Hz to 100 kHz. Typical power supply rejection is 60 dB at 1 kHz.

9.2 Typical Application

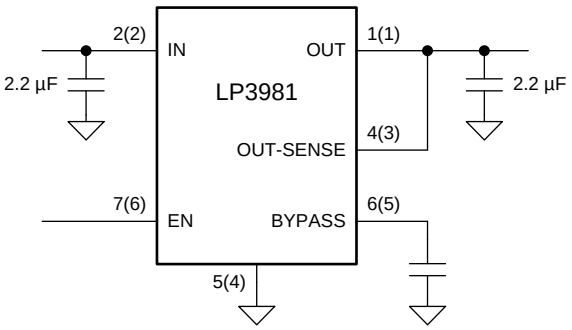


Figure 17. LP3981 Typical Application

9.2.1 Design Requirements

Example requirements for typical voltage inverter applications:

Table 1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage	3.5 V, ±10%
Output voltage	2.5 V, ±5%
Output current	300 mA (maximum)
RMS noise, 10 Hz to100 kHz	35 μV_{RMS}
PSRR at 1 kHz	60 dB

9.2.2 Detailed Design Procedure

9.2.2.1 Power Dissipation and Device Operation

The permissible power dissipation for any package is a measure of the capability of the device to pass heat from the power source, the junctions of the device, to the ultimate heat sink, the ambient environment. Thus, the power dissipation is dependant on the ambient temperature and the thermal resistance across the various interfaces between the die and ambient air.

As stated in the notes for *Absolute Maximum Ratings* and *Recommended Operating Conditions*, the allowable power dissipation for the device in a given package can be calculated using Equation 1:

$$P_D = \frac{T_{J(MAX)} - T_A)}{R_{\theta JA}} \quad (1)$$

With an $R_{\theta JA}$ = 56.5°C/W, the device in the WSON package returns a value of 1.77 W with a maximum junction temperature of 125°C and an ambient temperature of 25°C. The device in a VSSOP package returns a figure of 0.565 W ($R_{\theta JA}$ = 177°C/W).

The actual power dissipation across the device can be represented by Equation 2:

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (2)$$

This establishes the relationship between the power dissipation allowed due to thermal considerations, the voltage drop across the device, and the continuous current capability of the device. The device can deliver 300 mA but care must be taken when choosing the continuous current output for the device under the operating load conditions.

The RθJA value is not a characteristic of the package by itself but of the package, the printed circuit board (PCB), and other environmental factors. Equation 2 is only valid when the application configuration matches the EIA/JEDEC JESD51-7 (High-K) configuration in which $R_{\theta JA}$ was either measured or modeled. Few, if any, user applications conform to the PCB configuration defined by the EIA/JEDEC standards. As a result, the $R_{\theta JA}$ values are useful only when comparing assorted packages that have been measured or modeled to the EIA/JEDEC standards, but are of little use to estimate real world junction temperatures.

The EIA/JEDEC standard JESD51-2 provides methodologies to estimate the junction temperature from external measurements (ψ_{JB} references the temperature at the PCB, and ψ_{JT} references the temperature at the top surface of the package) when operating under steady-state power dissipation conditions. These methodologies have been determined to be relatively independent of the PCB attached to the package when compared to the more typical $R_{\theta JA}$. Refer to *Semiconductor and IC Package Thermal Metrics* application report, SPRA953, for specifics.

9.2.2.2 External Capacitors

Like any low-dropout regulator, the LP3981 requires external capacitors for regulator stability. The LP3981 is specifically designed for portable applications requiring minimum board space and smallest components. These capacitors must be correctly selected for good performance.

9.2.2.3 Input Capacitor

An input capacitance of ≅ 2.2 µF is required between the LP3981 input pin and ground (the amount of the capacitance may be increased without limit).

This capacitor must be located a distance of not more than 1 cm from the input pin and returned to a clean analog ground. Any good quality ceramic, tantalum, or film capacitor may be used at the input.

NOTE

Tantalum capacitors can suffer catastrophic failures due to surge current when connected to a low-impedance source of power (like a battery or a very large capacitor). If a tantalum capacitor is used at the input, it must be specified by the manufacturer to have a surge current rating sufficient for the application.

There are no requirements for the ESR on the input capacitor, but tolerance and temperature coefficient must be considered when selecting the capacitor to ensure the capacitance is ≅ 2.2 µF over the entire operating temperature range.

9.2.2.4 Output Capacitor

The LP3981 is designed specifically to work with very small ceramic output capacitors. A ceramic capacitor (dielectric types Z5U, Y5V or X7R) in the 2.2-µF to 22-µF range with 5-mΩ to 500-mΩ ESR is suitable in the LP3981 application circuit.

It is also possible to use tantalum or film capacitors at the output, but these are not as attractive for reasons of size and cost (see *Capacitor Characteristics*).

The output capacitor must meet the requirement for minimum amount of capacitance and also have an equivalent series resistance (ESR) value which is within a stable range (5 mΩ to 500 mΩ).

9.2.2.5 No-Load Stability

The LP3981 remains stable and in regulation with no external load. This is specially important in CMOS RAM keep-alive applications.

9.2.2.6 Noise Bypass Capacitor

Connecting a 0.033-µF capacitor between the BYPASS pin and ground significantly reduces noise on the regulator output. This capacitor is connected directly to a high impedance node in the bad gap reference circuit. Any significant loading on this node causes a change on the regulated output voltage. For this reason, DC leakage current through this pin must be kept as low as possible for best output voltage accuracy.

The types of capacitors best suited for the noise bypass capacitor are ceramic and film. Hight-quality ceramic capacitors with either NPO or COG dielectric typically have very low leakage. Polypropolene and polycarbonate film capacitors are available in small surface-mount packages and typically have extremely low leakage current.

Unlike many other LDOs, addition of a noise reduction capacitor does not effect the transient response of the device.

9.2.2.7 Capacitor Characteristics

The LP3981 is designed to work with ceramic capacitors on the output to take advantage of the benefits they offer: for capacitance values in the range of 1 µF to 4.7 µF, ceramic capacitors are the smallest, least expensive and have the lowest ESR values (which makes them best for eliminating high frequency noise). The ESR of a typical 1µF ceramic capacitor is in the range of 20 mΩ to 40 mΩ, which easily meets the ESR requirement for stability by the LP3981.

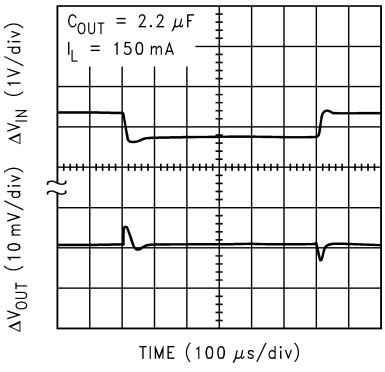
Capacitance of a ceramic capacitor can vary with temperature. Most large value ceramic capacitors (≅ 2.2 µF) are manufactured with Z5U or Y5V temperature characteristics, which results in the capacitance dropping by more than 50% as the temperature goes from 25°C to 85°C.

A better choice for temperature coefficient in a ceramic capacitor is X7R, which holds the capacitance within ±15%.

Tantalum capacitors are less desirable than ceramic for use as output capacitors because they are more expensive when comparing equivalent capacitance and voltage ratings in the 1-µF to 4.7-µF range.

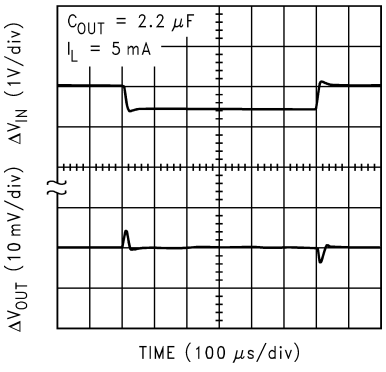
Another important consideration is that tantalum capacitors have higher ESR values than equivalently sized ceramics. This means that while it may be possible to find a tantalum capacitor with an ESR value within the stable range, it would have to be larger in capacitance (which means bigger and more costly) than a ceramic capacitor with the same ESR value. It must also be noted that the ESR of a typical tantalum increases about 2:1 as the temperature goes from 25°C down to −40°C, so some guard band must be allowed.

9.2.3 Application Curves



$V_{IN} = V_{OUT}$ + 1 V to V_{OUT} + 1.6 V

Figure 18. Line Transient Response



$V_{IN} = V_{OUT}$ + 1V to V_{OUT} + 1.6 V

Figure 19. Line Transient Response

10 Power Supply Recommendations

The LP3981 is designed to operate from an input voltage supply range between 2.5 V and 6 V. The input voltage range provides adequate headroom in order for the device to have a regulated output. This input supply must be well regulated. If the input supply is noisy, additional input capacitors with low ESR can help to improve the output noise performance.

11 Layout

11.1 Layout Guidelines

For best overall performance, place all circuit components on the same side of the circuit board and as near as practical to the respective LDO pin connections. Place ground return connections to the input and output capacitor, and to the LDO ground pin as close to each other as possible, connected by a wide, component-side, copper surface. The use of vias and long traces to create LDO circuit connections is strongly discouraged and negatively affects system performance. This grounding and layout scheme minimizes inductive parasitics, and thereby reduces load-current transients, minimizes noise, and increases circuit stability. A ground reference plane is also recommended and is either embedded in the PCB itself or located on the bottom side of the PCB opposite the components. This reference plane serves to assure accuracy of the output voltage, shield noise, and behaves similar to a thermal plane to spread (or sink) heat from the LDO device. In most applications, this ground plane is necessary to meet thermal requirements.

11.2 Layout Example

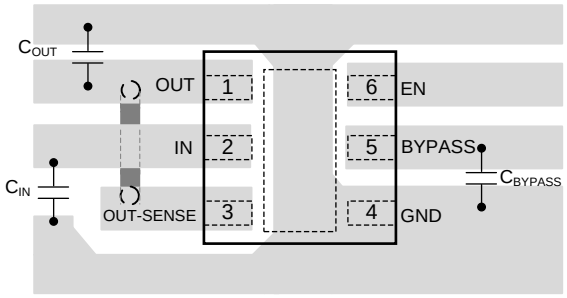


Figure 20. LP3981 Layout Example

12 Device and Documentation Support

12.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.2 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LP3981ILD-2.5/NOPB	ACTIVE	WSON	NGC	6	1000	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 125	LO1UB	Samples
LP3981ILD-3.0/NOPB	ACTIVE	WSON	NGC	6	1000	RoHS & Green	NIPDAU | SN	Level-3-260C-168 HR		L017B	Samples
LP3981ILD-3.3/NOPB	ACTIVE	WSON	NGC	6	1000	RoHS & Green	NIPDAU | SN	Level-3-260C-168 HR	-40 to 125	LO1XB	Samples
LP3981ILDX-2.5/NOPB	ACTIVE	WSON	NGC	6	4500	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 125	LO1UB	Samples
LP3981ILDX-2.7/NOPB	ACTIVE	WSON	NGC	6	4500	RoHS & Green	NIPDAU | SN	Level-3-260C-168 HR	-40 to 125	LO1VB	Samples
LP3981ILDX-2.8/NOPB	ACTIVE	WSON	NGC	6	4500	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 125	L01ZB	Samples
LP3981ILDX-2.83/NOPB	ACTIVE	WSON	NGC	6	4500	RoHS & Green	NIPDAU | SN	Level-3-260C-168 HR	-40 to 125	LO1SB	Samples
LP3981ILDX-3.03/NOPB	ACTIVE	WSON	NGC	6	4500	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 125	LO1YB	Samples
LP3981IMM-2.5/NOPB	ACTIVE	VSSOP	DGK	8	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LFKB	Samples
LP3981IMM-2.7/NOPB	ACTIVE	VSSOP	DGK	8	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LFLB	Samples
LP3981IMM-2.8/NOPB	ACTIVE	VSSOP	DGK	8	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LFTB	Samples
LP3981IMM-3.0/NOPB	ACTIVE	VSSOP	DGK	8	1000	RoHS & Green	SN	Level-1-260C-UNLIM		LF3B	Samples
LP3981IMM-3.03/NOPB	ACTIVE	VSSOP	DGK	8	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LFPB	Samples
LP3981IMM-3.3/NOPB	ACTIVE	VSSOP	DGK	8	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LFNB	Samples
LP3981IMMX-2.5/NOPB	ACTIVE	VSSOP	DGK	8	3500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LFKB	Samples
LP3981IMMX-3.3/NOPB	ACTIVE	VSSOP	DGK	8	3500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LFNB	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

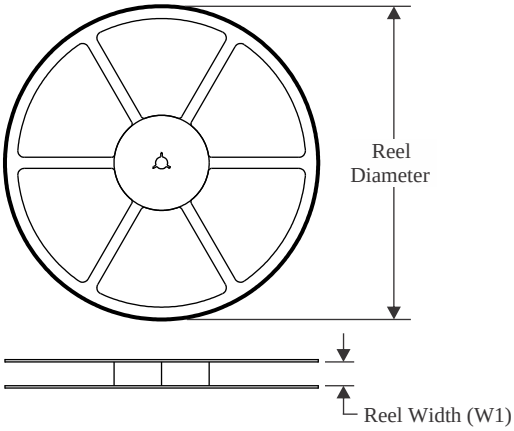
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

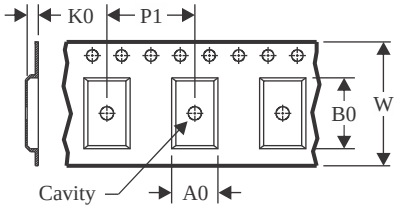
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

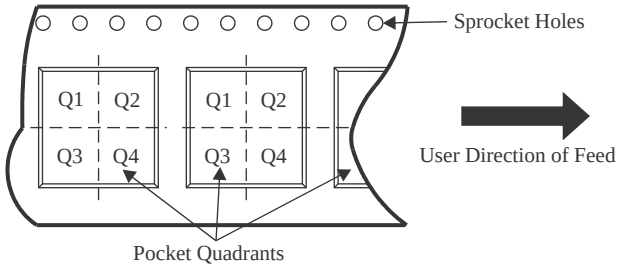


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

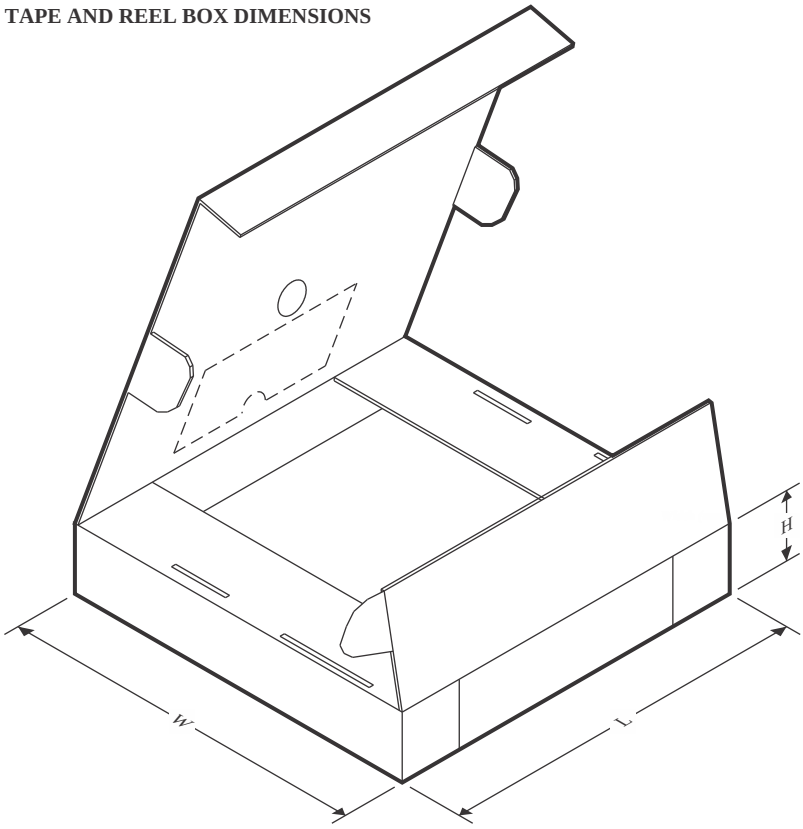
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

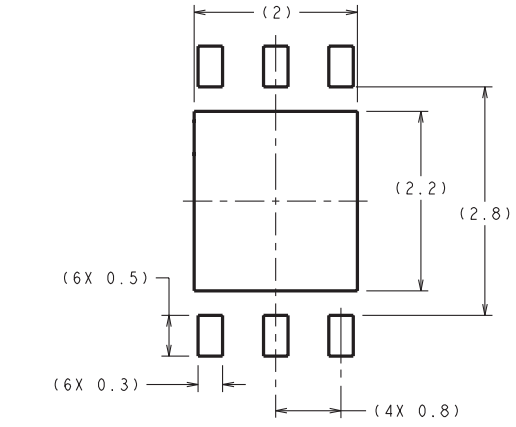
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP3981ILD-2.5/NOPB	WSON	NGC	6	1000	178.0	12.4	4.3	3.3	1.0	8.0	12.0	Q1
LP3981ILD-3.0/NOPB	WSON	NGC	6	1000	180.0	12.4	4.3	3.3	1.0	8.0	12.0	Q1
LP3981ILD-3.3/NOPB	WSON	NGC	6	1000	178.0	12.4	4.3	3.3	1.0	8.0	12.0	Q1
LP3981ILDX-2.5/NOPB	WSON	NGC	6	4500	330.0	12.4	4.3	3.3	1.0	8.0	12.0	Q1
LP3981ILDX-2.7/NOPB	WSON	NGC	6	4500	330.0	12.4	4.3	3.3	1.0	8.0	12.0	Q1
LP3981ILDX-2.8/NOPB	WSON	NGC	6	4500	330.0	12.4	4.3	3.3	1.0	8.0	12.0	Q1
LP3981ILDX-2.83/NOPB	WSON	NGC	6	4500	330.0	12.4	4.3	3.3	1.0	8.0	12.0	Q1
LP3981ILDX-3.03/NOPB	WSON	NGC	6	4500	330.0	12.4	4.3	3.3	1.0	8.0	12.0	Q1
LP3981IMM-2.5/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LP3981IMM-2.7/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LP3981IMM-2.8/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LP3981IMM-3.0/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LP3981IMM-3.03/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LP3981IMM-3.3/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LP3981IMMX-2.5/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LP3981IMMX-3.3/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



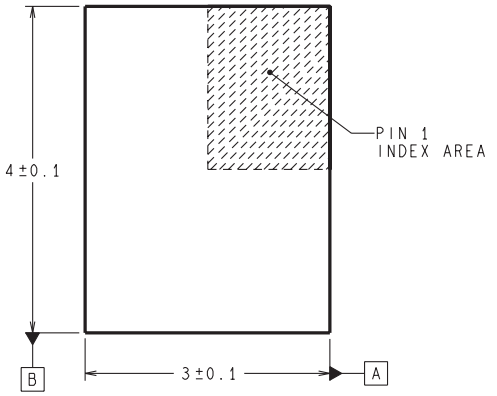
*All dimensions are nominal

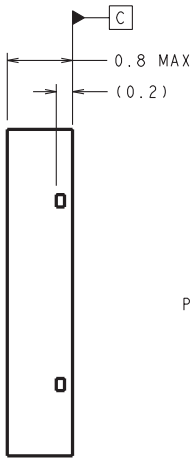
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP3981ILD-2.5/NOPB	WSON	NGC	6	1000	208.0	191.0	35.0
LP3981ILD-3.0/NOPB	WSON	NGC	6	1000	213.0	191.0	35.0
LP3981ILD-3.3/NOPB	WSON	NGC	6	1000	208.0	191.0	35.0
LP3981ILDX-2.5/NOPB	WSON	NGC	6	4500	356.0	356.0	36.0
LP3981ILDX-2.7/NOPB	WSON	NGC	6	4500	367.0	367.0	38.0
LP3981ILDX-2.8/NOPB	WSON	NGC	6	4500	356.0	356.0	36.0
LP3981ILDX-2.83/NOPB	WSON	NGC	6	4500	367.0	367.0	38.0
LP3981ILDX-3.03/NOPB	WSON	NGC	6	4500	356.0	356.0	36.0
LP3981IMM-2.5/NOPB	VSSOP	DGK	8	1000	208.0	191.0	35.0
LP3981IMM-2.7/NOPB	VSSOP	DGK	8	1000	208.0	191.0	35.0
LP3981IMM-2.8/NOPB	VSSOP	DGK	8	1000	208.0	191.0	35.0
LP3981IMM-3.0/NOPB	VSSOP	DGK	8	1000	208.0	191.0	35.0
LP3981IMM-3.03/NOPB	VSSOP	DGK	8	1000	208.0	191.0	35.0
LP3981IMM-3.3/NOPB	VSSOP	DGK	8	1000	208.0	191.0	35.0
LP3981IMMX-2.5/NOPB	VSSOP	DGK	8	3500	367.0	367.0	35.0
LP3981IMMX-3.3/NOPB	VSSOP	DGK	8	3500	367.0	367.0	35.0

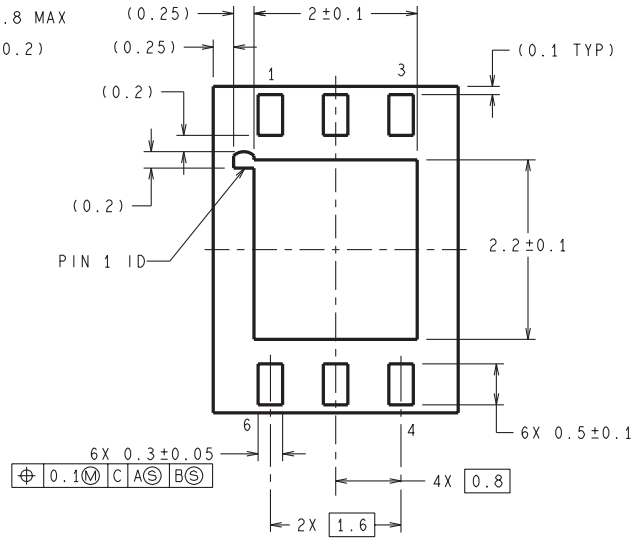


RECOMMENDED LAND PATTERN
1:1 RATIO WITH PKG SOLDER PADS

DIMENSIONS ARE IN MILLIMETERS







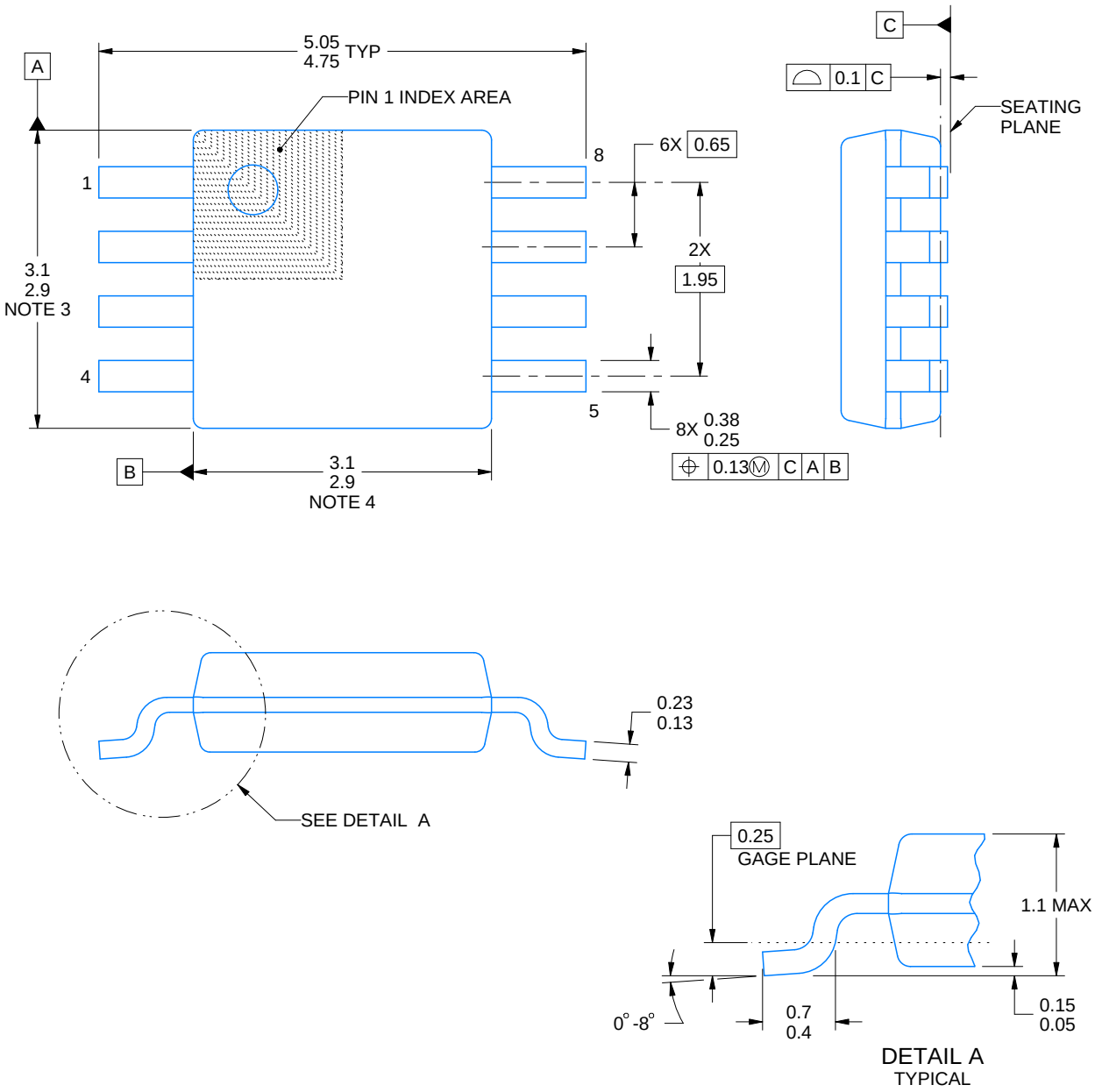
LDC06D (Rev B)

PACKAGE OUTLINE

DGK0008A

VSSOP - 1.1 mm max height

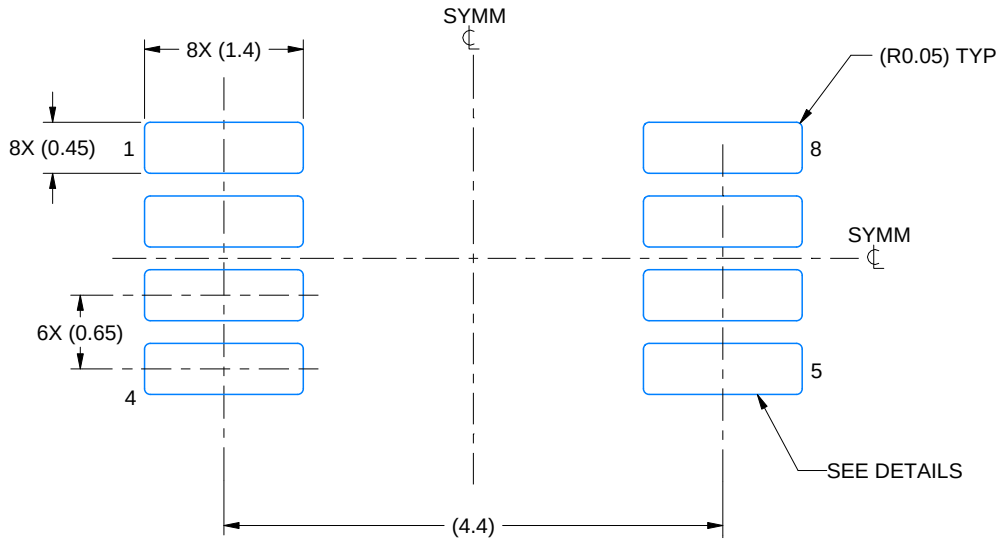
SMALL OUTLINE PACKAGE



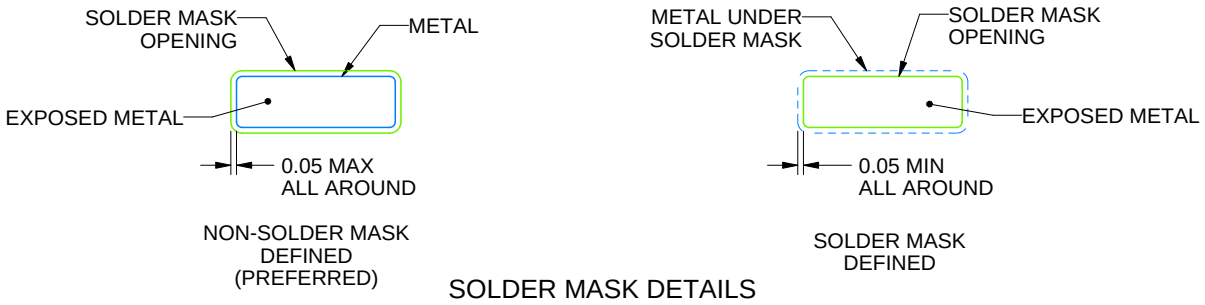
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

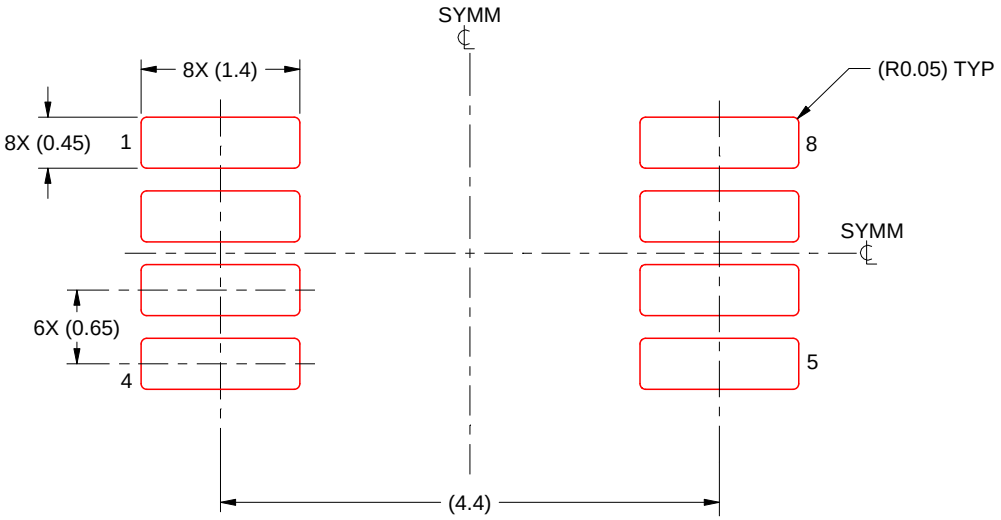


SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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