NCP4682, NCP4685

150 mA, Ultra Low Supply Current, Low Dropout Regulator

The NCP4682 and NCP4685 are CMOS Low Dropout Linear voltage regulators with 150 mA output current capability. The devices have high output voltage accuracy, a 1 μA (typ.) ultra low supply current and high ripple rejection. Current fold−back protection is integrated in the devices to protect against over current and short current conditions. A Chip Enable (NCP4682 only) function is included to save power by further lowering supply current, which is advantageous for battery powered applications. The NCP4685 is optimized for the lowest quiescent current possible in applications where the device is always on.

Features

- Operating Input Voltage Range: 1.70 V to 5.25 V
- Output Voltage Range: 1.2 V to 3.3 V (available in 0.1 V steps)
- Output Voltage Accuracy: ±0.8%
- Excellent Output Voltage Temperature Coefficient : ±40 ppm/°C
- Supply Current: 1.0 μA (excluding CE pull down current)
- Standby Current: 0.1 μA
- Dropout Voltage: 0.24 V (I_{OUT} = 150 mA, V_{OUT} = 2.8 V)
- Line Regulation: 0.02%/V Typ.
- Stable with Ceramic Capacitors: 0.1 μF or more
- Current Fold Back Protection
- Available in UDFN4 1.0 x 1.0 mm, SC−82AB, SOT23 Packages
- These are Pb−Free Devices

Typical Applications

- Battery−Powered Equipment
- Networking and Communication Equipment
- Cameras, DVRs, STB and Camcorders
- Home Appliances

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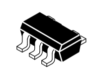
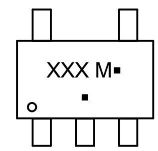
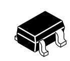
MARKING DIAGRAMS

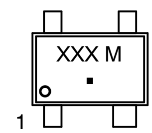


SOT−23−5
CASE 1212





SC−82AB
CASE 419C



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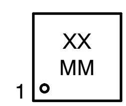
UDFN4
CASE 517BR



XXX, XX = Specific Device Code
M, MM = Date Code
▪ = Pb−Free Package

(*Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 19 of this data sheet.

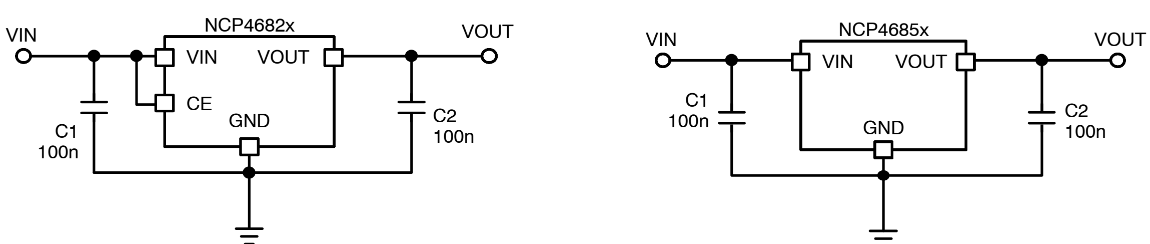


Figure 1. Typical Application Schematics

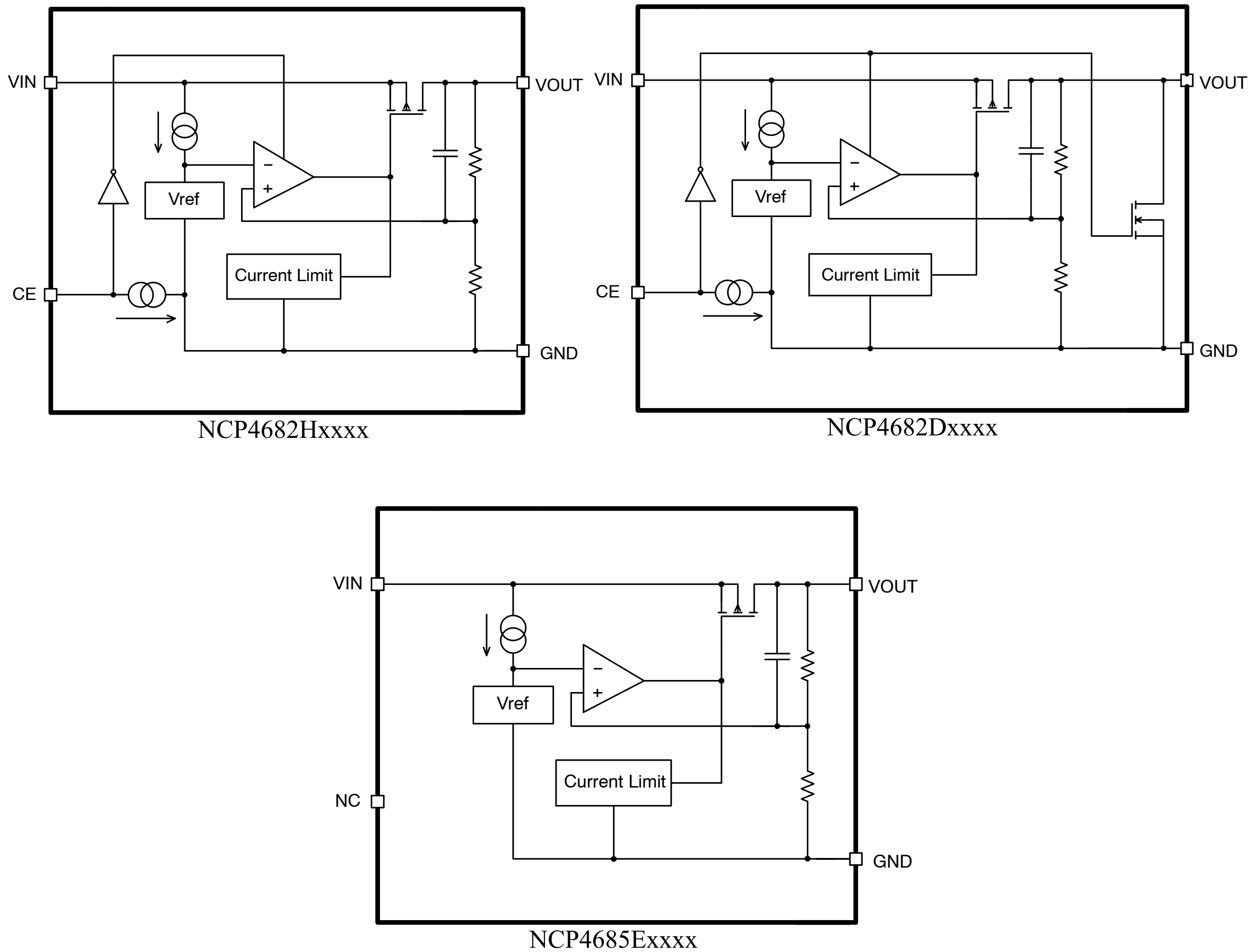


Figure 2. Simplified Schematic Block Diagram

PIN FUNCTION DESCRIPTION

Pin No. UDFN1010*	Pin No. SC−82AB	Pin No. SOT23	Pin Name	Description
1	3	5	V_{OUT}	Output pin
2	2	2	GND	Ground
3	1	3	CE/NC	Chip enable pin (Active “H”) / No connection
4	4	1	V_{IN}	Input pin
–	–	4	NC	No connection

*Tab is GND level. (They are connected to the reverse side of this IC.)
The tab is better to be connected to the GND, but leaving it open is also acceptable.

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input Voltage (Note 1)	V_{IN}	6.0	V
Output Voltage	V_{OUT}	−0.3 to V_{IN} + 0.3	V
Chip Enable Input	V_{CE}	6.0	V
Output Current	I_{OUT}	200	mA

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Dissipation UDFN1010	P_D	400	mW
Power Dissipation SC−82AB		380	
Power Dissipation SOT23		420	
Junction Temperature	T_J	−40 to 150	°C
Storage Temperature	T_{STG}	−55 to 125	°C
ESD Capability, Human Body Model (Note 2)	ESD_{HBM}	2000	V
ESD Capability, Machine Model (Note 2)	ESD_{MM}	200	V

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Refer to ELECTRICAL CHARACTERISTIS and APPLICATION INFORMATION for Safe Operating Area.
2. This device series incorporates ESD protection and is tested by the following methods:
   ESD Human Body Model tested per AEC−Q100−002 (EIA/JESD22−A114)
   ESD Machine Model tested per AEC−Q100−003 (EIA/JESD22−A115)
   Latchup Current Maximum Rating tested per JEDEC standard: JESD78.

THERMAL CHARACTERISTICS

Rating	Symbol	Value	Unit
Thermal Characteristics, UDFN 1.0 x 1.0 mm Thermal Resistance, Junction−to−Air	$R_{\theta JA}$	250	°C/W
Thermal Characteristics, SOT23 Thermal Resistance, Junction−to−Air	$R_{\theta JA}$	238	°C/W
Thermal Characteristics, SC−82AB Thermal Resistance, Junction−to−Air	$R_{\theta JA}$	263	°C/W

ELECTRICAL CHARACTERISTICS

−40°C ≤ T_A ≤ 85°C; $V_{IN} = V_{OUT(NOM)}$ + 1 V or 2.5 V, whichever is greater; I_{OUT} = 1 mA, $C_{IN} = C_{OUT}$ = 0.1 μF, unless otherwise noted. Typical values are at T_A = +25°C.

Parameter	Test Conditions		Symbol	Min	Typ	Max	Unit
Operating Input Voltage	(Note 3)		V_{IN}	1.70		5.25	V
Output Voltage	T_A = +25 °C	V_{OUT} ≥ 2.0 V	V_{OUT}	x0.992		x1.008	V
		V_{OUT} < 2.0 V		−16		16	mV
	−40°C ≤ T_A ≤ 85°C	V_{OUT} ≥ 2.0 V		x0.985		x1.015	V
		V_{OUT} < 2.0 V		−30		30	mV
Output Voltage Temp. Coefficient	−40°C ≤ T_A ≤ 85°C		ΔV_{OUT} / ΔT_A		±40		ppm/°C
Line Regulation	$V_{OUT(NOM)}$ + 0.5 V ≤ V_{IN} ≤ 5.0 V		$Line_{Reg}$		0.02	0.10	%/V
Load Regulation	I_{OUT} = 1 mA to 150 mA		$Load_{Reg}$		10	20	mV
Dropout Voltage	I_{OUT} = 150 mA	1.2 V ≤ V_{OUT} < 1.5 V	V_{DO}		0.76	1.05	V
		1.5 V ≤ V_{OUT} < 1.7 V			0.53	0.80	
		1.7 V ≤ V_{OUT} < 2.0 V			0.44	0.65	
		2.0 V ≤ V_{OUT} < 2.5 V			0.34	0.50	
		2.5 V ≤ V_{OUT} < 2.8 V			0.28	0.40	
		2.8 V ≤ V_{OUT} < 3.3 V			0.24	0.32	
Output Current			I_{OUT}	150			mA
Short Current Limit	V_{OUT} = 0 V		I_{SC}		40		mA
Quiescent Current			I_Q		1.0	1.5	μA

ELECTRICAL CHARACTERISTICS

$-40°C \le T_A \le 85°C$; $V_{IN} = V_{OUT(NOM)}$ + 1 V or 2.5 V, whichever is greater; I_{OUT} = 1 mA, $C_{IN} = C_{OUT}$ = 0.1 μF, unless otherwise noted. Typical values are at T_A = +25°C.

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
Standby Current	V_{CE} = 0 V, T_A = 25°C, NCP4682 only	I_{STB}		0.1	1.0	μA
CE Pin Threshold Voltage (NCP4682 only)	CE Input Voltage "H"	V_{CEH}	1.5			V
	CE Input Voltage "L"	V_{CEL}			0.3	
CE Pull Down Current	NCP4682 only	I_{CEPD}		0.3		μA
Power Supply Rejection Ratio	V_{IN} = 2.2 V, V_{OUT} = 1.2 V, ΔV_{IN} = 0.2 V_{pk-pk}, I_{OUT} = 30 mA, f = 1 kHz	PSRR		30		dB
Output Noise Voltage	f = 10 Hz to 100 kHz, I_{OUT} = 30 mA, V_{OUT} = 1.2 V, V_{IN} = 2.2 V	V_N		70		μV_{rms}
Low Output Nch Tr. On Resistance	V_{IN} = 4 V, V_{CE} = 0 V, NCP4682D only	R_{LOW}		30		Ω

3. The maximum Input Voltage of the Electrical Characteristics is 5.25 V. In case of exceeding this specification, the IC must be operated n condition that the Input Voltage is up to 5.50 V and total operation time is within 500 hours.

TYPICAL CHARACTERISTICS

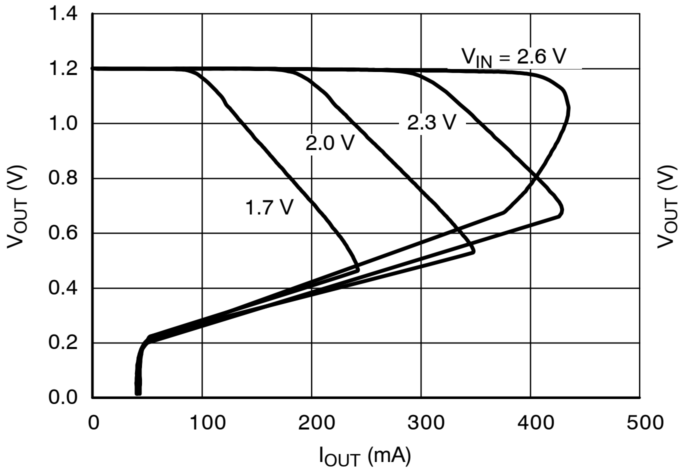


Figure 3. Output Voltage vs. Output Current 1.2 V Version (T_J = 25°C)

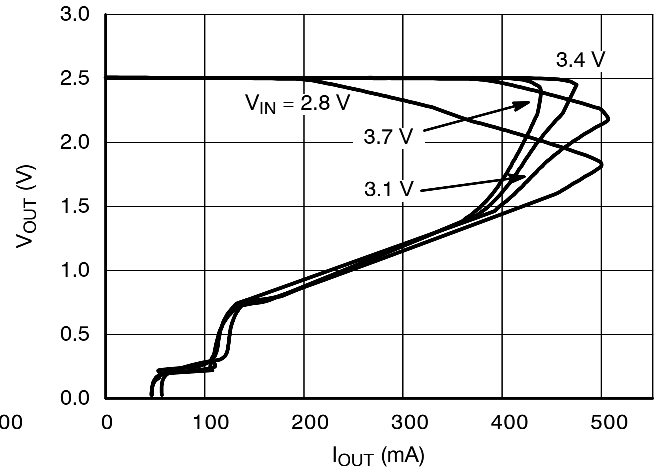


Figure 4. Output Voltage vs. Output Current 2.5 V Version (T_J = 25°C)

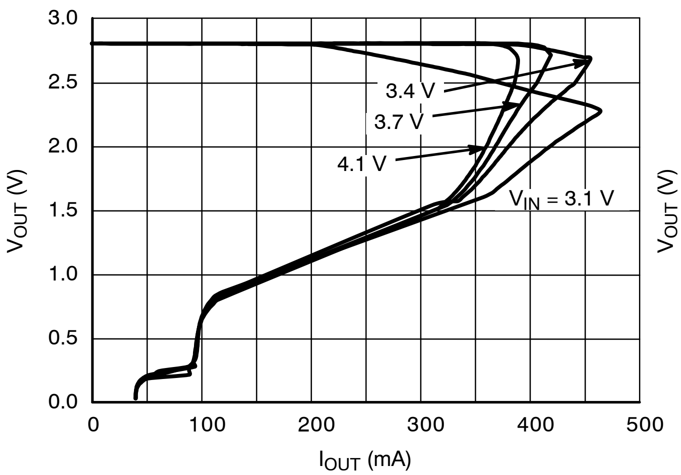


Figure 5. Output Voltage vs. Output Current 2.8 V Version (T_J = 25°C)

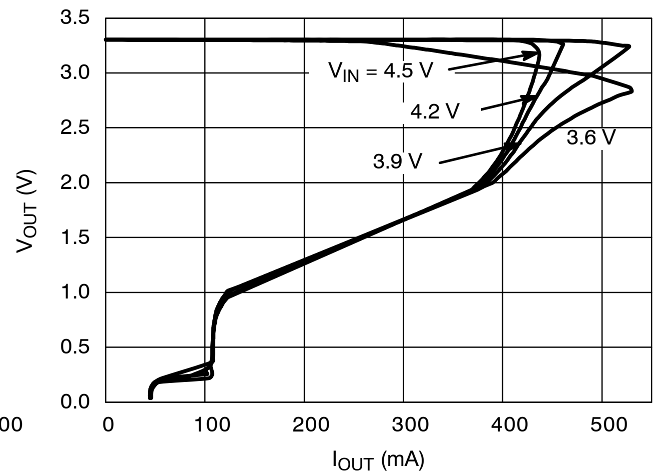


Figure 6. Output Voltage vs. Output Current 3.3 V Version (T_J = 25°C)

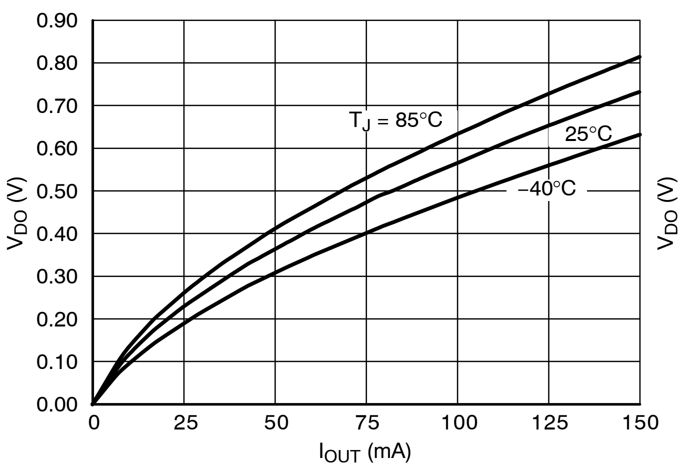


Figure 7. Dropout Voltage vs. Output Current 1.2 V Version

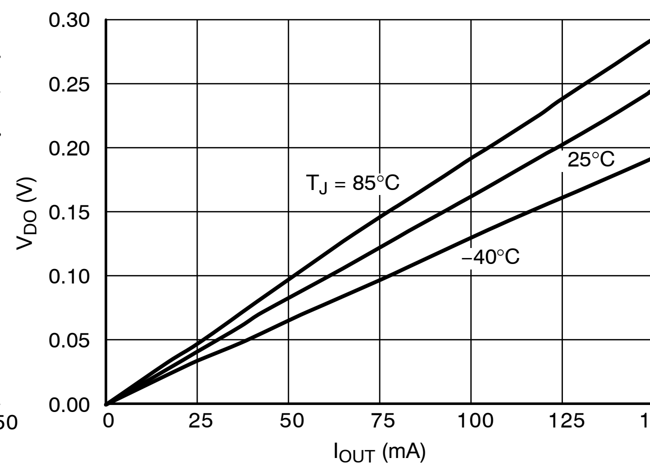


Figure 8. Dropout Voltage vs. Output Current 2.5 V Version

TYPICAL CHARACTERISTICS

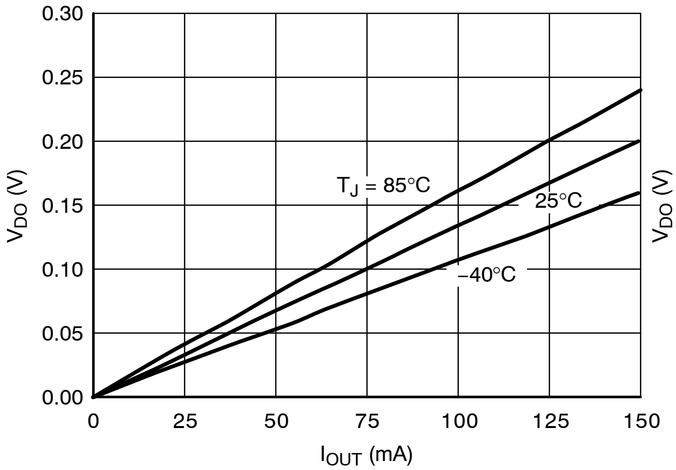


Figure 9. Dropout Voltage vs. Output Current 2.8 V Version

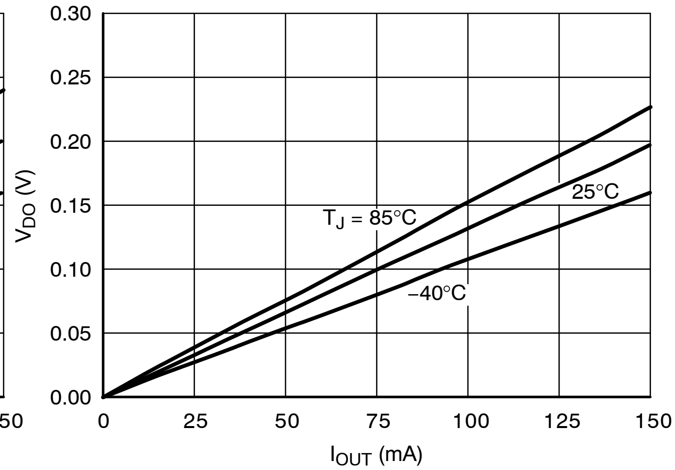


Figure 10. Dropout Voltage vs. Output Current 3.3 V Version

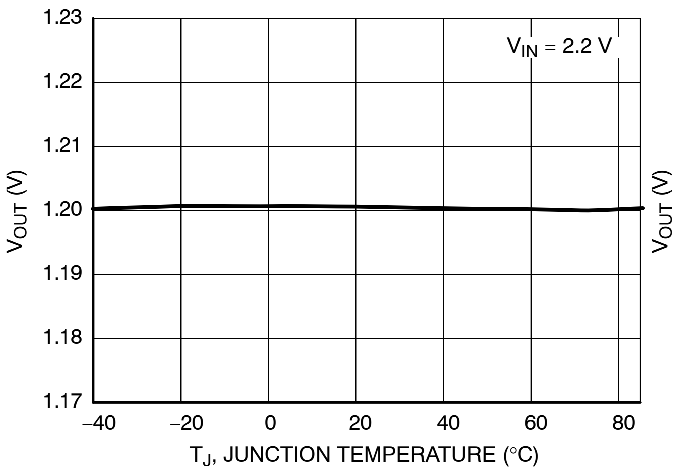


Figure 11. Output Voltage vs. Temperature, 1.2 V Version

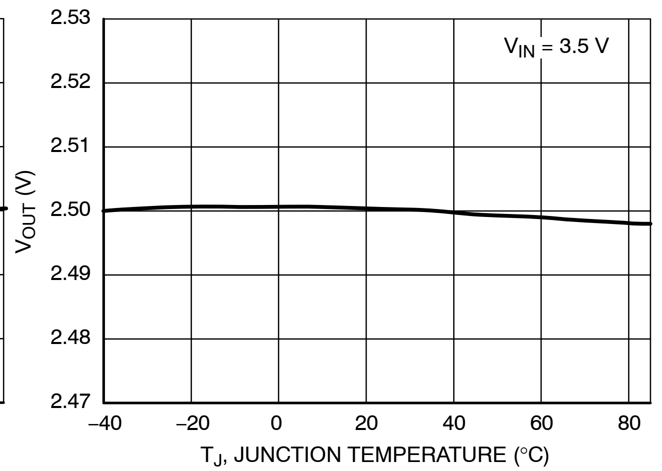


Figure 12. Output Voltage vs. Temperature, 2.5 V Version

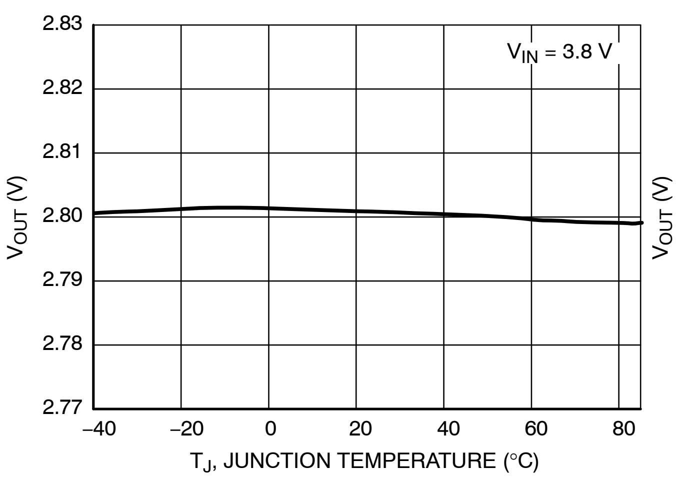


Figure 13. Output Voltage vs. Temperature, 2.8 V Version

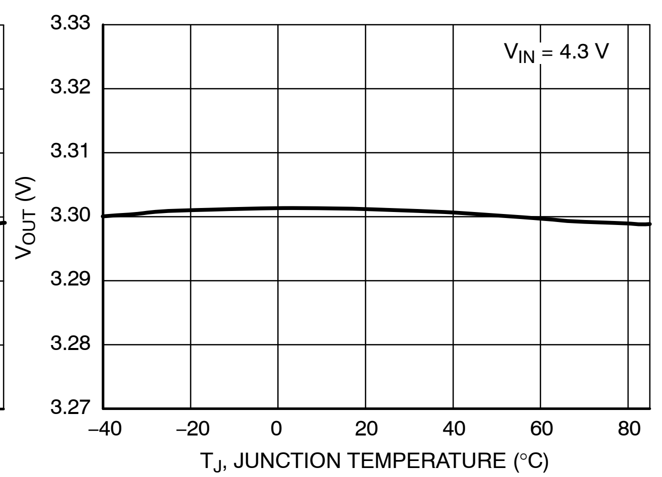


Figure 14. Output Voltage vs. Temperature, 3.3 V Version

TYPICAL CHARACTERISTICS

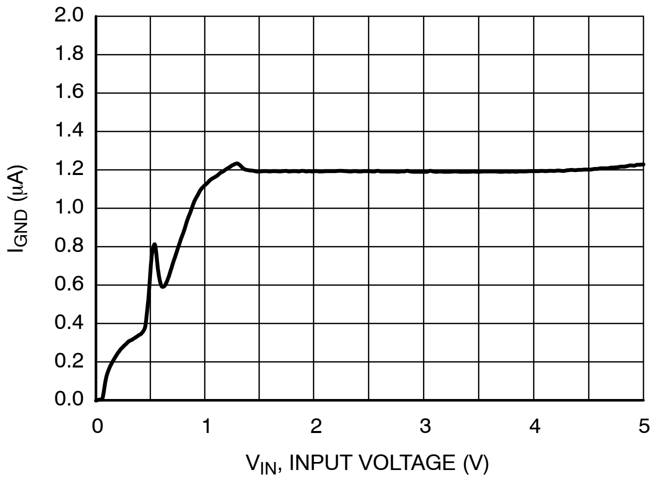


Figure 15. Supply Current vs. Input Voltage, 1.2 V Version

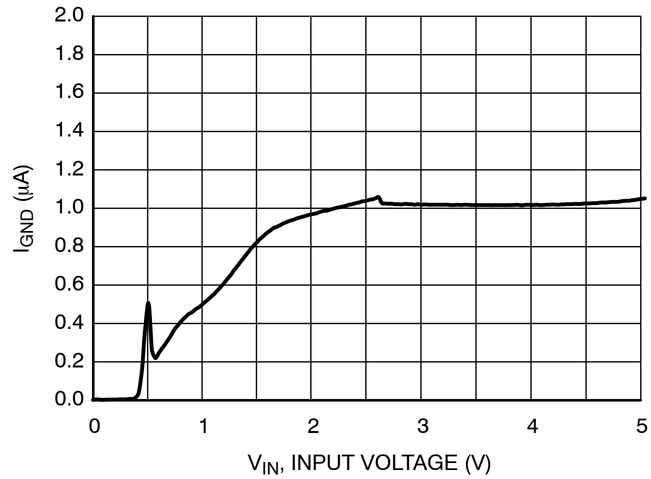


Figure 16. Supply Current vs. Input Voltage, 2.5 V Version

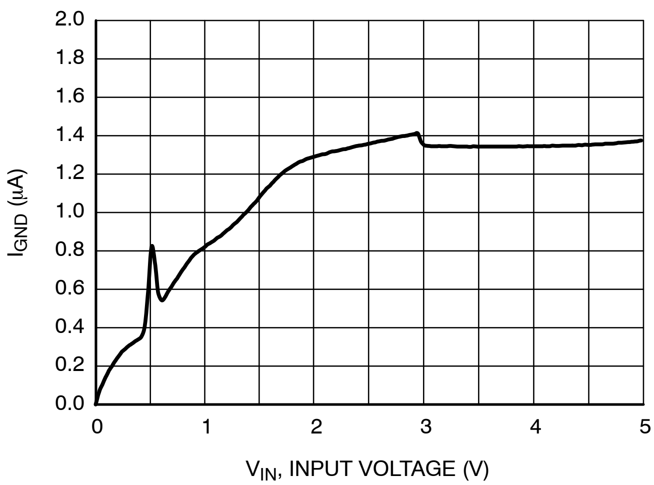


Figure 17. Supply Current vs. Input Voltage, 2.8 V Version

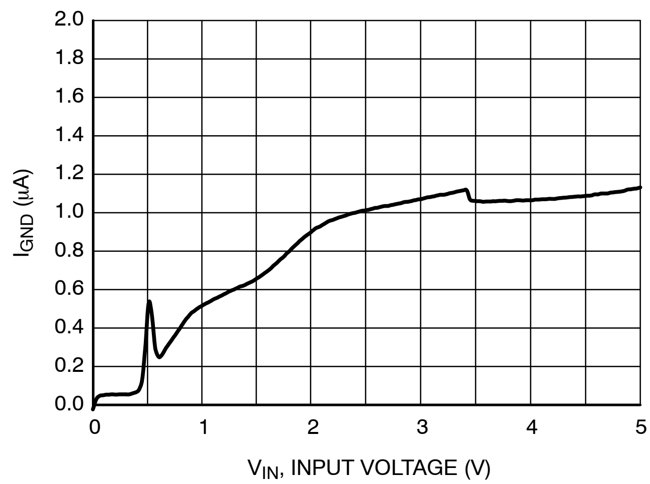


Figure 18. Supply Current vs. Input Voltage, 3.3 V Version

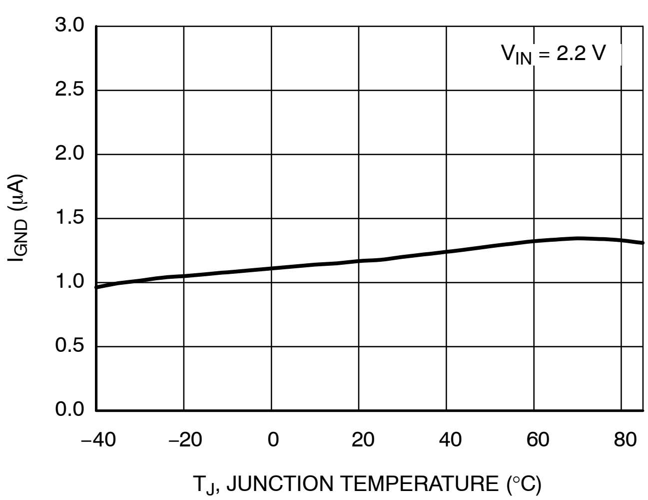


Figure 19. Supply Current vs. Temperature, 1.2 V Version

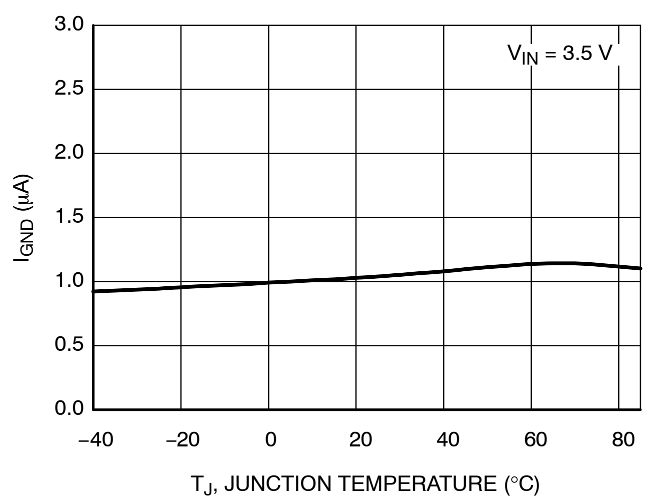


Figure 20. Supply Current vs. Temperature, 2.5 V Version

TYPICAL CHARACTERISTICS

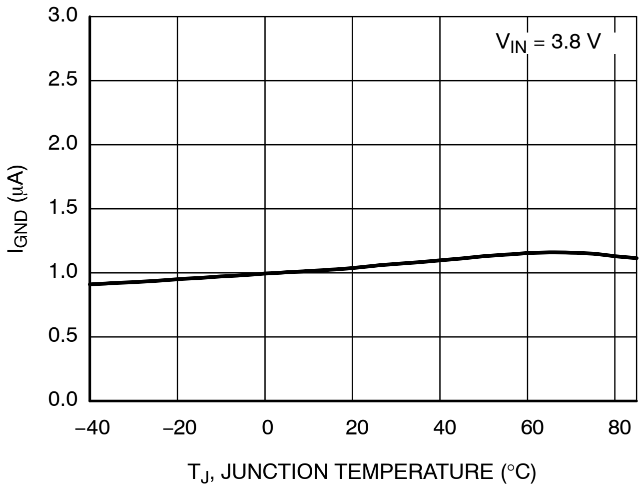


Figure 21. Supply Current vs. Temperature, 2.8 V Version

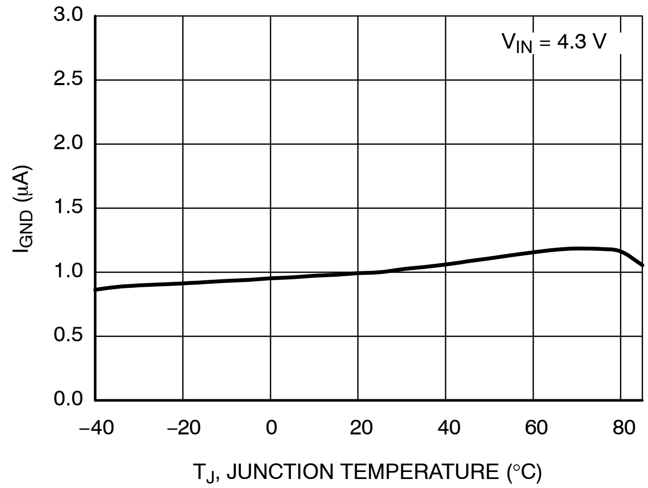


Figure 22. Supply Current vs. Temperature, 3.3 V Version

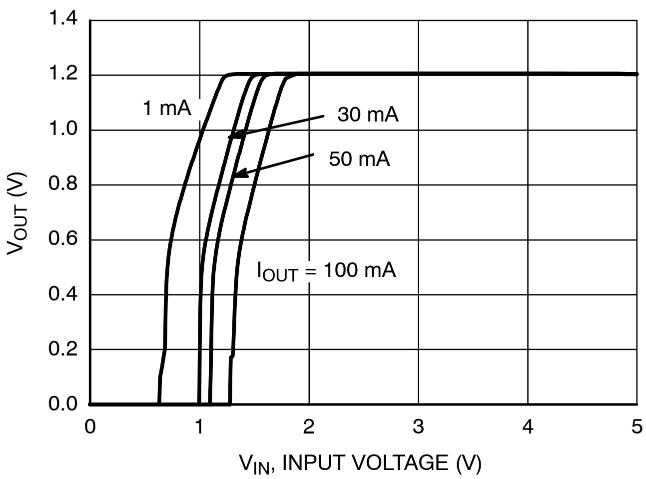


Figure 23. Output Voltage vs. Input Voltage, 1.2 V Version

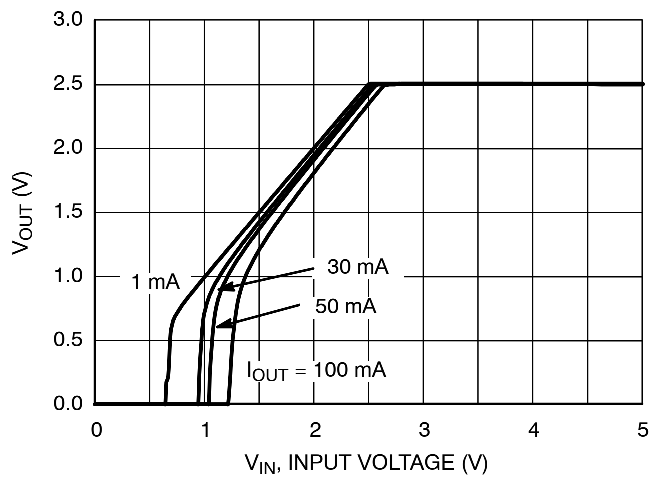


Figure 24. Output Voltage vs. Input Voltage, 2.5 V Version

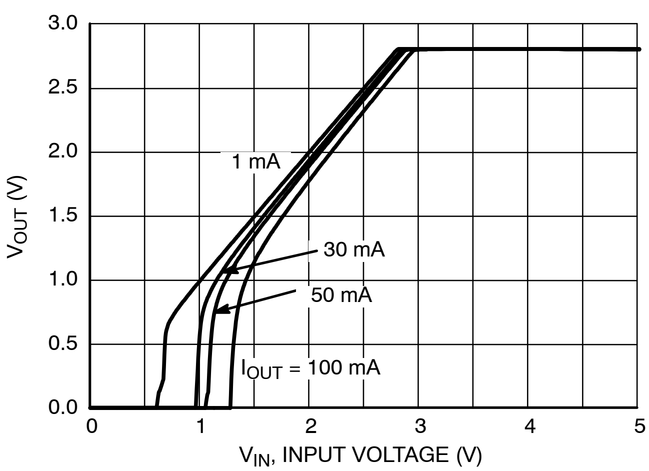


Figure 25. Output Voltage vs. Input Voltage, 2.8 V Version

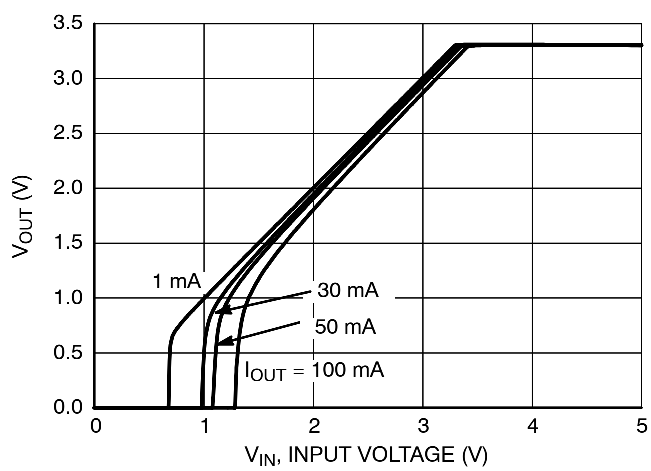


Figure 26. Output Voltage vs. Input Voltage, 3.3 V Version

TYPICAL CHARACTERISTICS

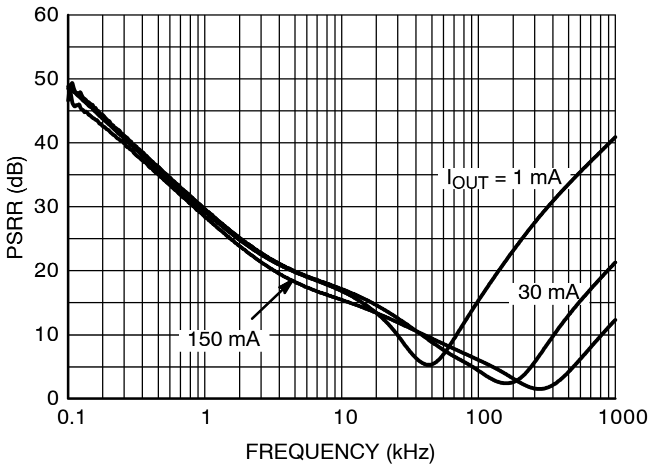


Figure 27. PSRR, 1.2 V Version, V_{IN} = 2.2 V

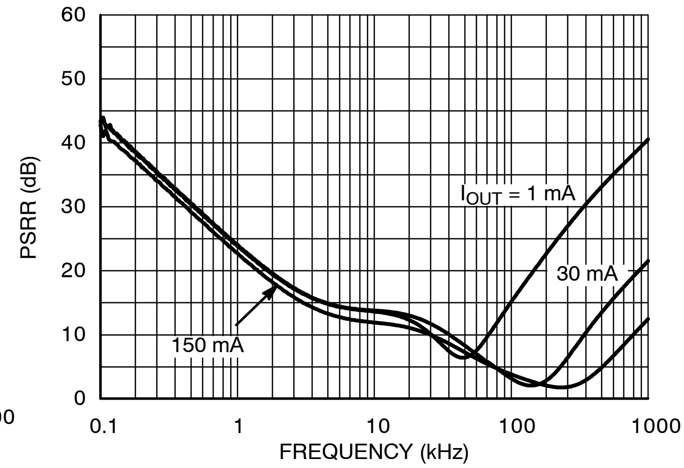


Figure 28. PSRR, 2.5 V Version, V_{IN} = 3.5 V

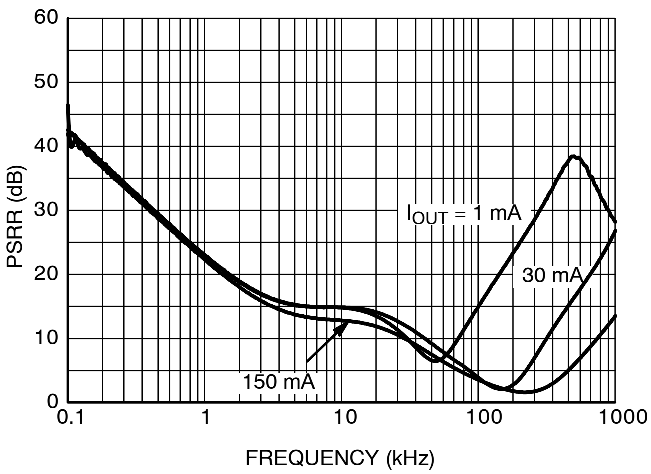


Figure 29. PSRR, 2.8 V Version, V_{IN} = 3.8 V

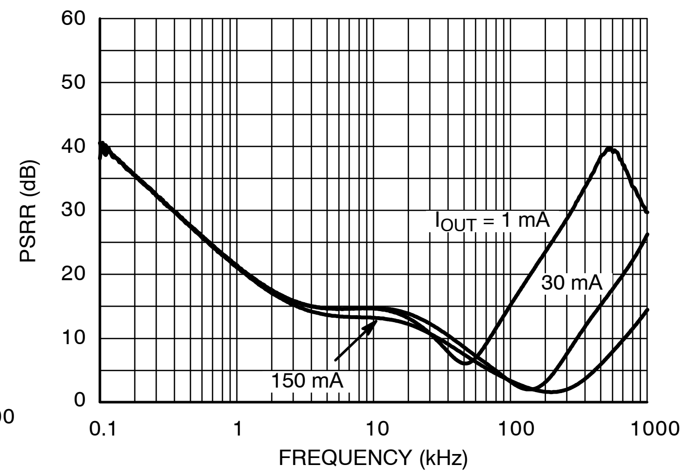


Figure 30. PSRR, 3.3 V Version, V_{IN} = 4.3 V

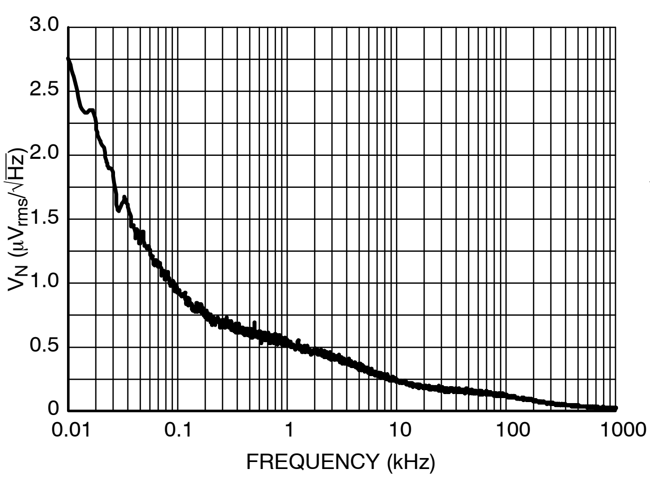


Figure 31. Output Voltage Noise, 1.2 V Version, V_{IN} = 2.2 V, I_{OUT} =30 mA

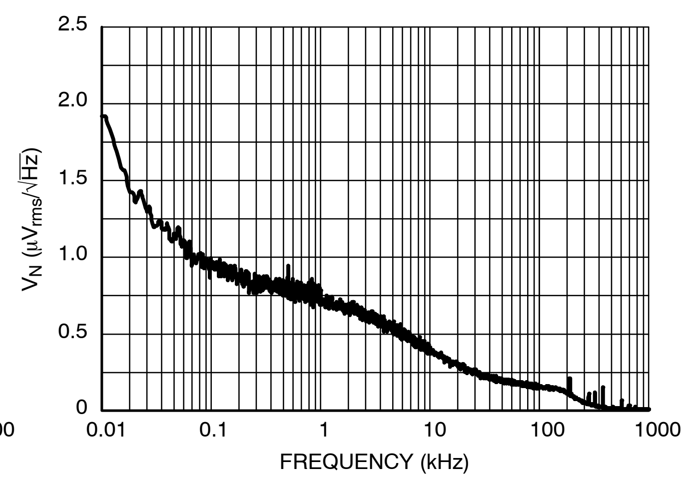


Figure 32. Output Voltage Noise, 2.5 V Version, V_{IN} = 3.5 V, I_{OUT} =30 mA

TYPICAL CHARACTERISTICS

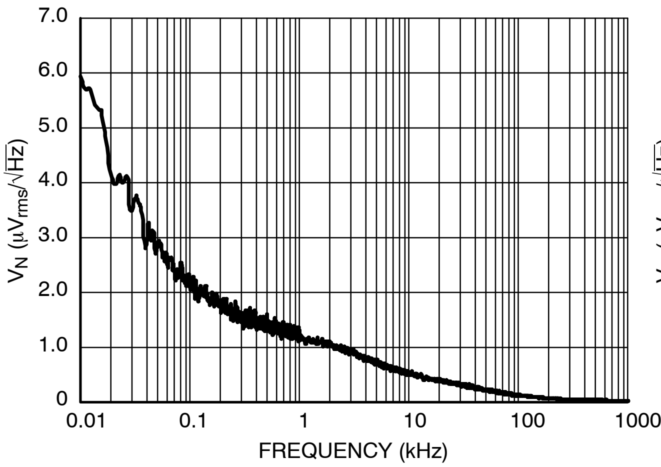


Figure 33. Output Voltage Noise, 2.8 V Version, V_{IN} = 3.8 V, I_{OUT} =30 mA

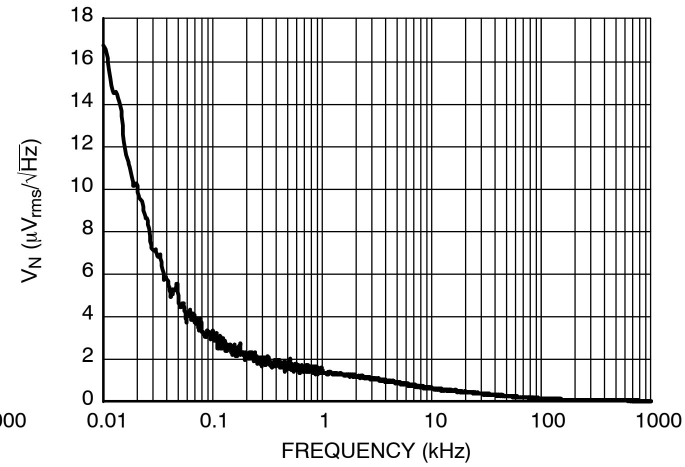


Figure 34. Output Voltage Noise, 3.3 V Version, V_{IN} = 4.3 V, I_{OUT} =30 mA

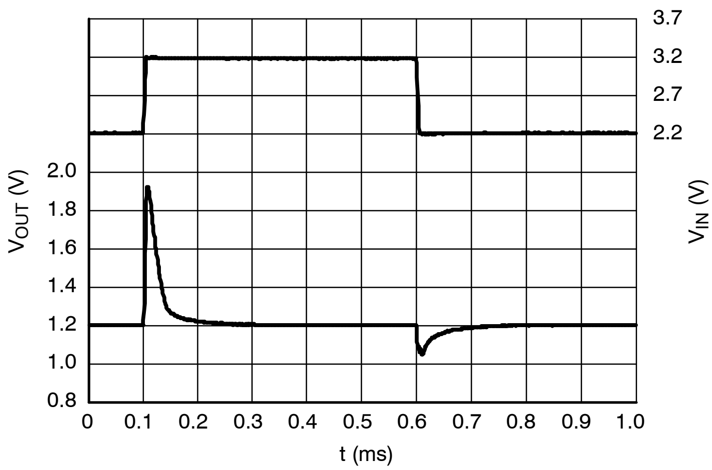


Figure 35. Line Transients, 1.2 V Version, $t_R = t_F$ = 5 μs, I_{OUT} = 30 mA

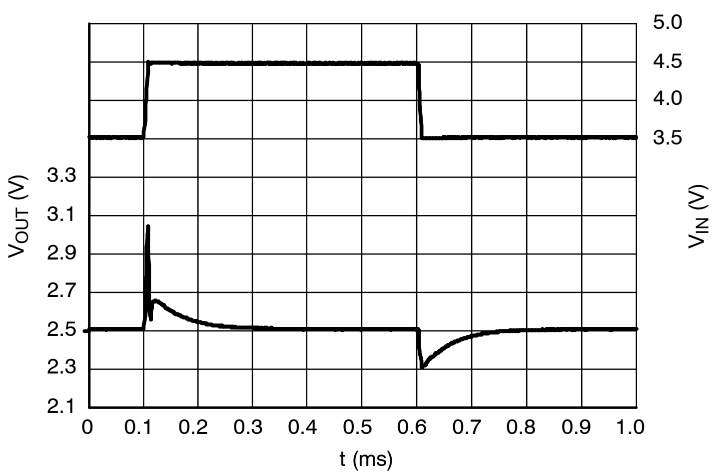


Figure 36. Line Transients, 2.5 V Version, $t_R = t_F$ = 5 μs, I_{OUT} = 30 mA

TYPICAL CHARACTERISTICS

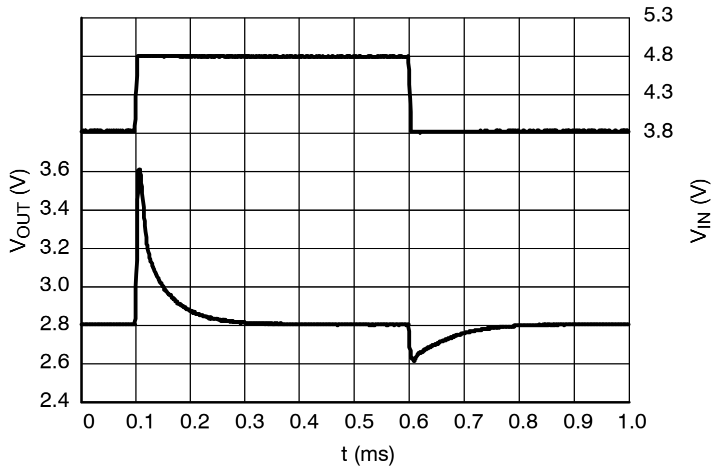


Figure 37. Line Transients, 2.8 V Version, $t_R = t_F = 5\ \mu s$, $I_{OUT} = 30$ mA

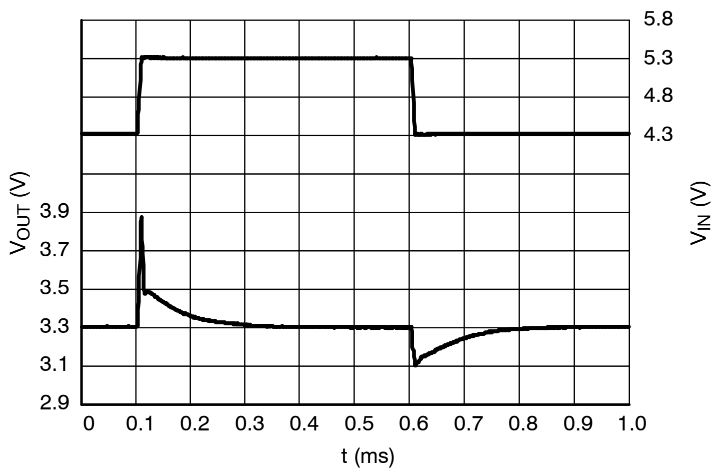


Figure 38. Line Transients, 3.3 V Version, $t_R = t_F = 5\ \mu s$, $I_{OUT} = 30$ mA

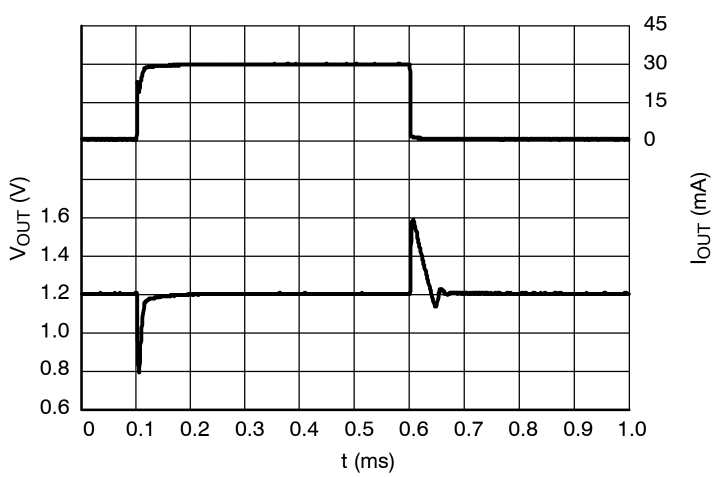


Figure 39. Load Transients, 1.2 V Version, $I_{OUT} = 1 – 30$ mA, $t_R = t_F = 0.5\ \mu s$, $V_{IN} = 2.2$ V

TYPICAL CHARACTERISTICS

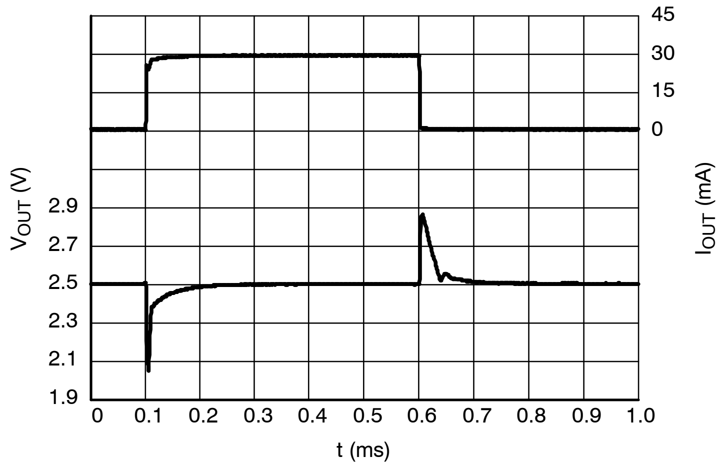


Figure 40. Load Transients, 2.5 V Version, I_{OUT} = 1 – 30 mA, $t_R = t_F$ = 0.5 μs, V_{IN} = 3.5 V

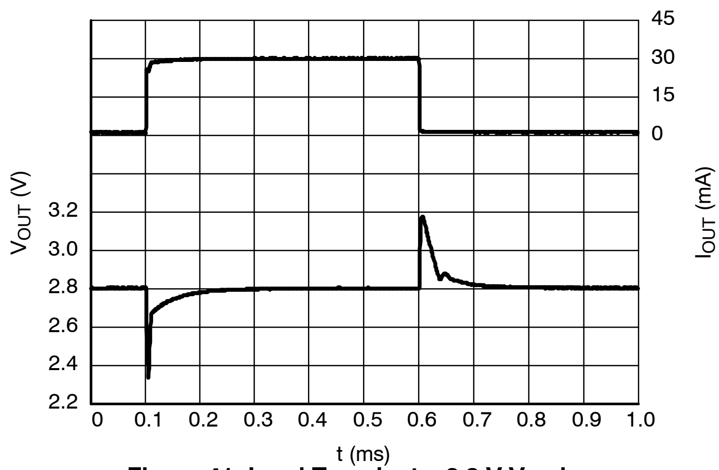


Figure 41. Load Transients, 2.8 V Version, I_{OUT} = 1 – 30 mA, $t_R = t_F$ = 0.5 μs, V_{IN} = 3.8 V

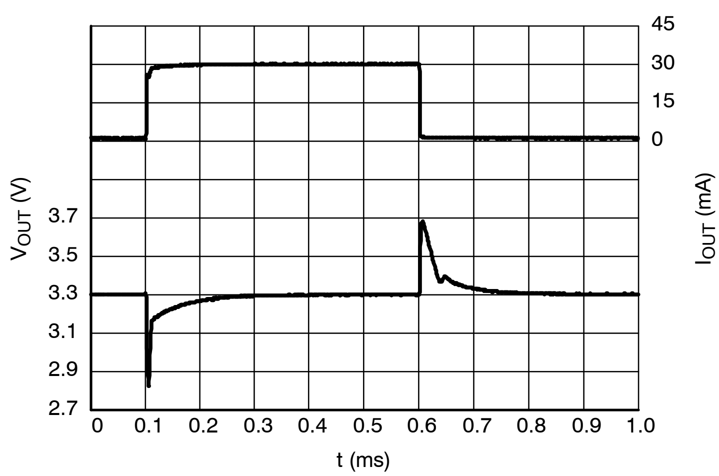


Figure 42. Load Transients, 3.3 V Version, I_{OUT} = 1 – 30 mA, $t_R = t_F$ = 0.5 μs, V_{IN} = 4.3 V

TYPICAL CHARACTERISTICS

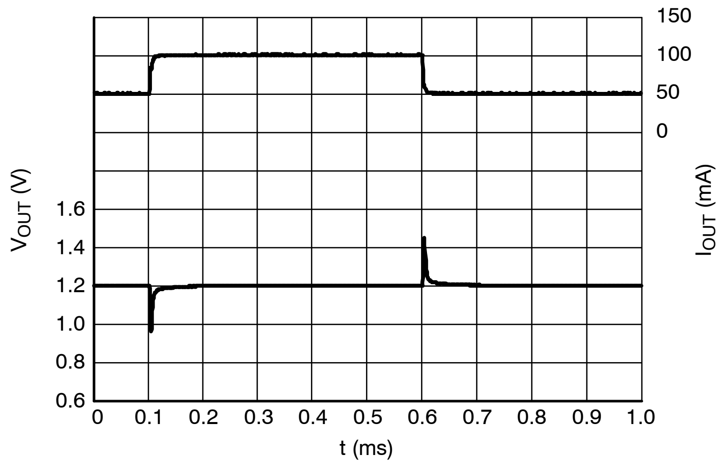


Figure 43. Load Transients, 1.2 V Version, I_{OUT} = 50 – 100 mA, $t_R = t_F$ = 0.5 μs, V_{IN} = 2.2 V

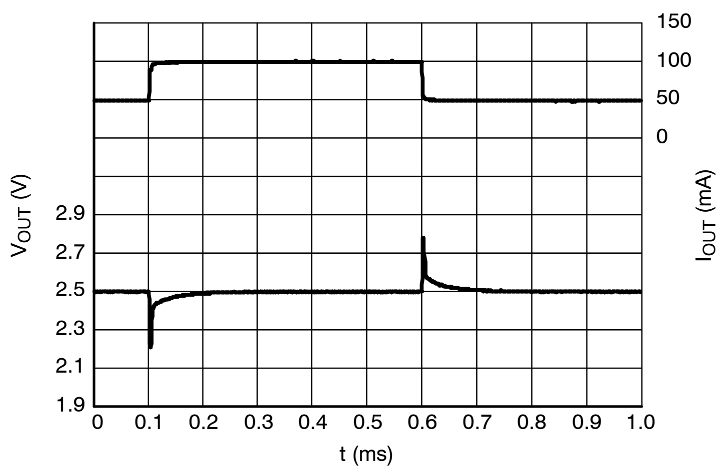


Figure 44. Load Transients, 2.5 V Version, I_{OUT} = 50 – 100 mA, $t_R = t_F$ = 0.5 μs, V_{IN} = 3.5 V

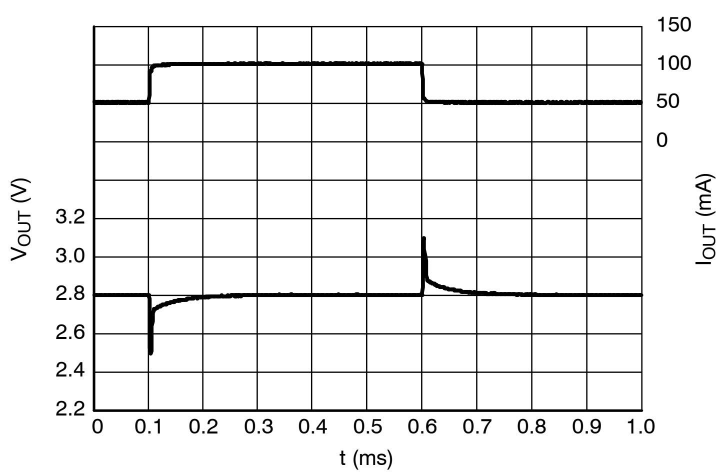


Figure 45. Load Transients, 2.8 V Version, I_{OUT} = 50 – 100 mA, $t_R = t_F$ = 0.5 μs, V_{IN} = 3.8 V

TYPICAL CHARACTERISTICS

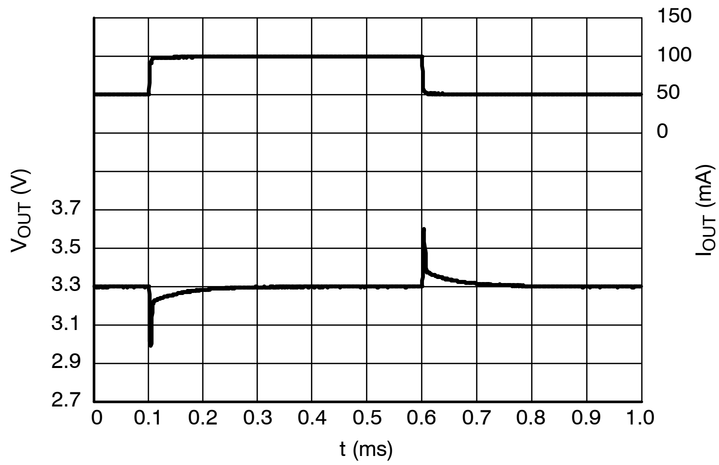


Figure 46. Load Transients, 3.3 V Version, I_{OUT} = 50 – 100 mA, $t_R = t_F$ = 0.5 μs, V_{IN} = 4.3 V

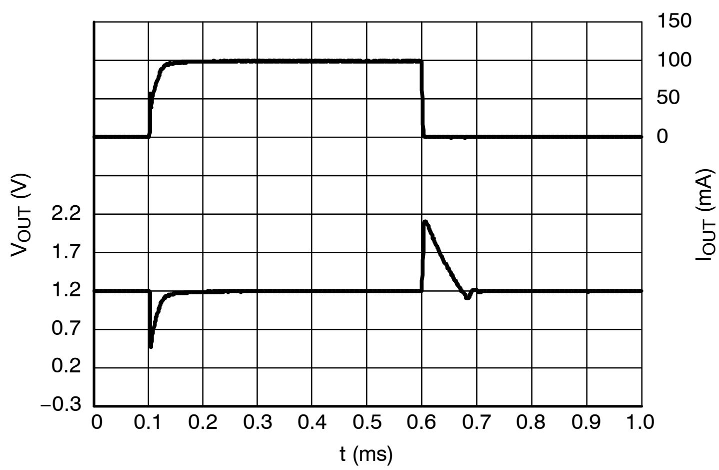


Figure 47. Load transients, 1.2 V Version, I_{OUT} = 1 – 100 mA, $t_R = t_F$ = 0.5 μs, V_{IN} = 2.2 V

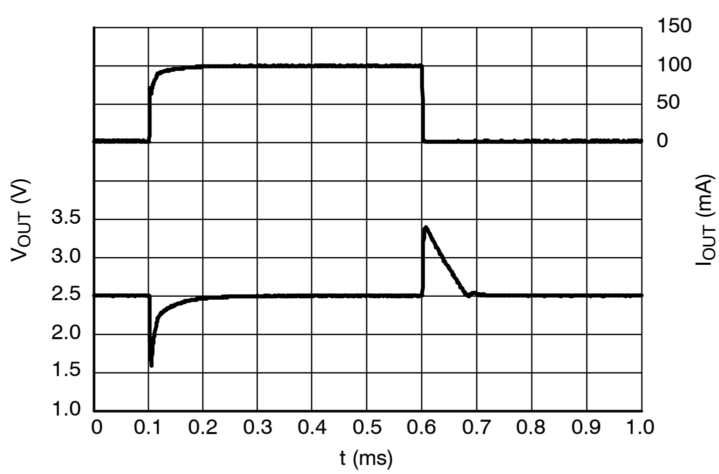


Figure 48. Load Transients, 2.5 V Version, I_{OUT} = 1 – 100 mA, $t_R = t_F$ = 0.5 μs, V_{IN} = 3.5 V

TYPICAL CHARACTERISTICS

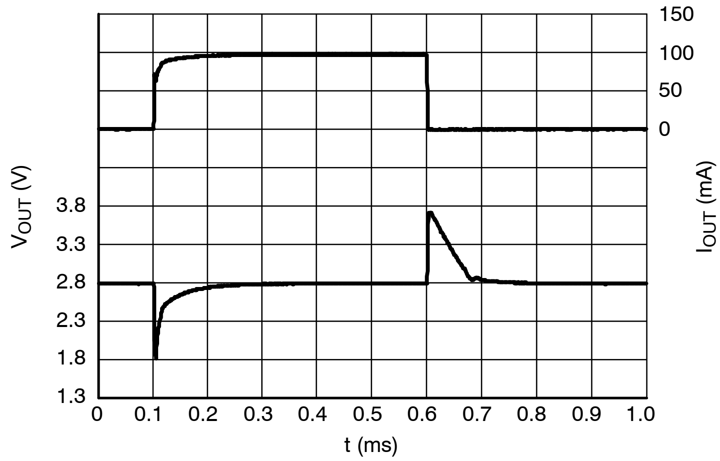


Figure 49. Load Transients, 2.8 V Version, I_{OUT} = 1 – 100 mA, t_R = t_F = 0.5 μs, V_{IN} = 3.8 V

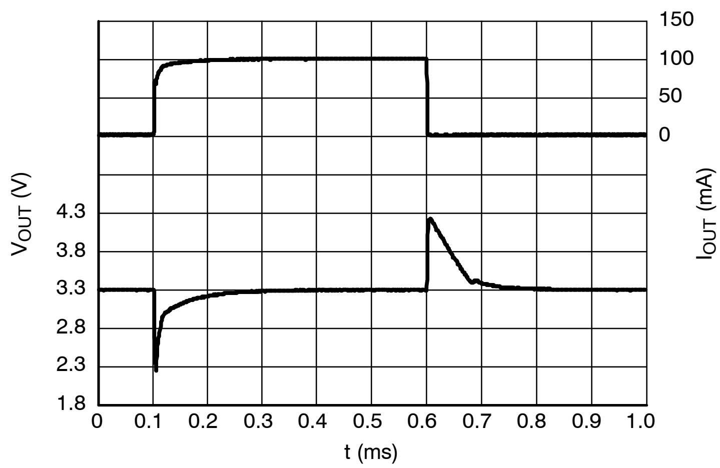


Figure 50. Load Transients, 3.3 V Version, I_{OUT} = 1 – 100 mA, t_R = t_F = 0.5 μs, V_{IN} = 4.3 V

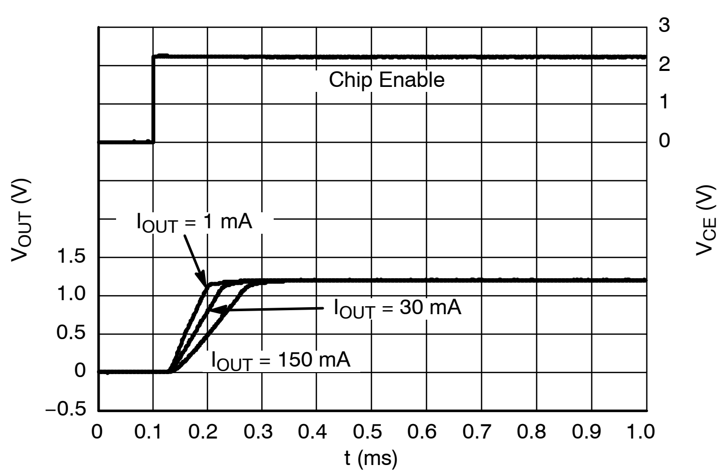


Figure 51. Start−up, NCP4682 1.2 V Version, V_{IN} = 2.2 V

TYPICAL CHARACTERISTICS

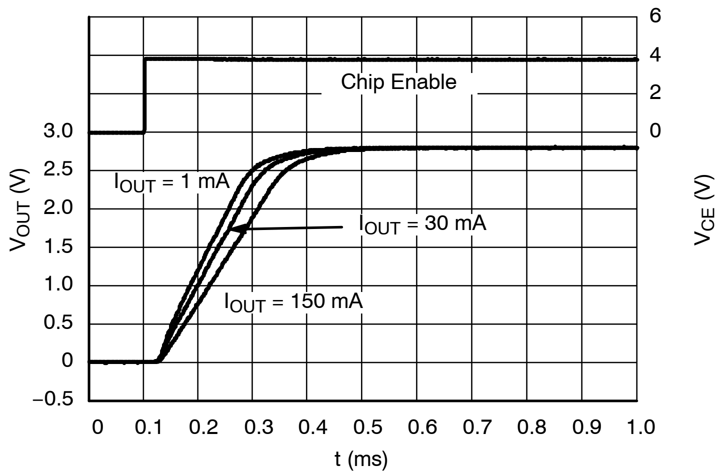


Figure 52. Start−up, NCP4682 2.8 V Version, V_{IN} = 3.8 V

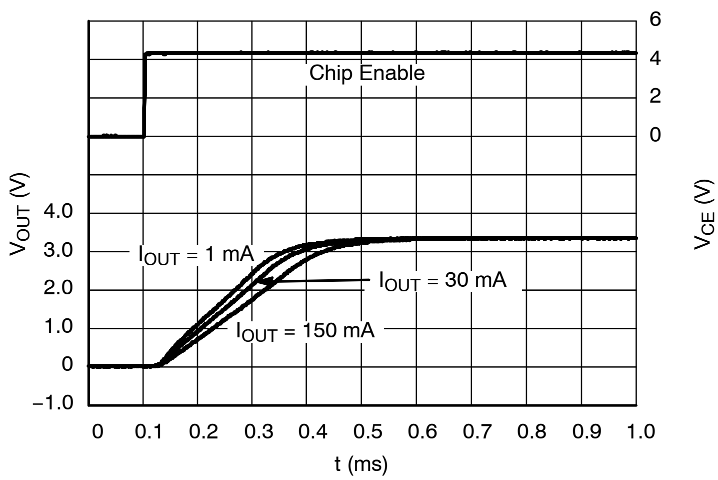


Figure 53. Start−up, NCP4682 3.3 V Version, V_{IN} = 4.3 V

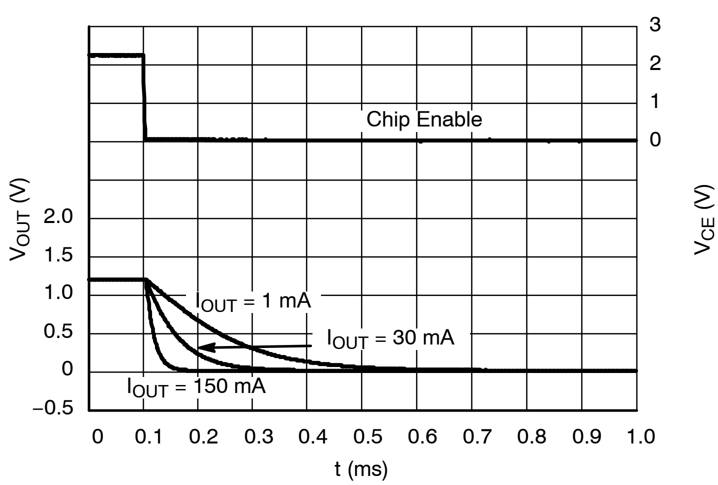


Figure 54. Shutdown, NCP4682 1.2 V Version D, V_{IN} = 2.2 V

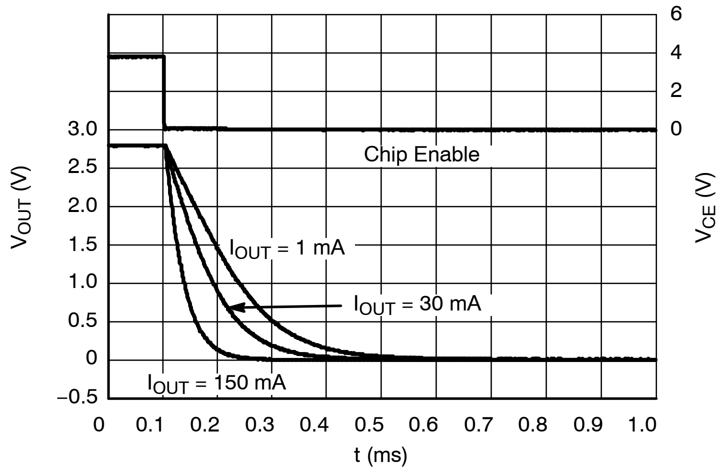


Figure 55. Shutdown, NCP4682 2.8 V Version D, V_{IN} = 3.8 V

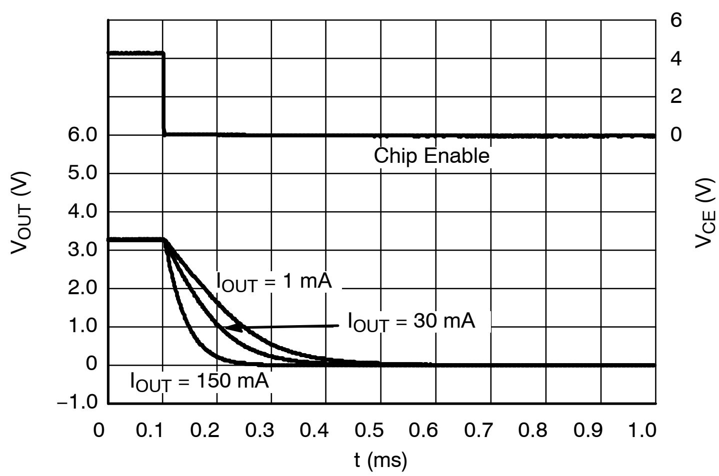


Figure 56. Shutdown, NCP4682 3.3 V Version D, V_{IN} = 4.3 V

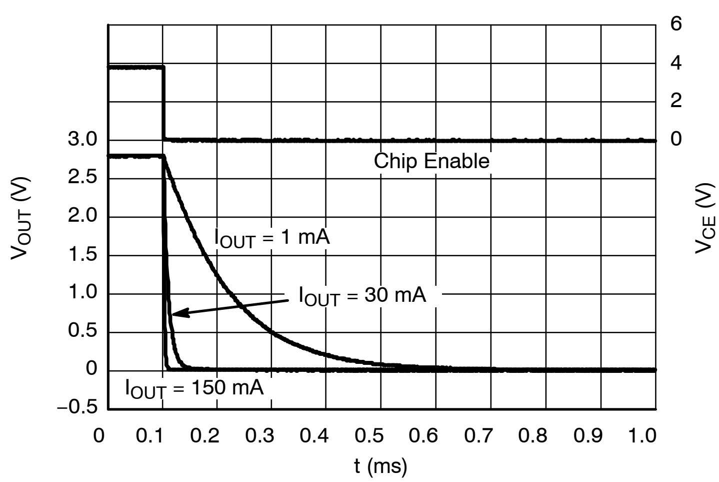


Figure 57. Shutdown, NCP4682 2.8 V Version H, V_{IN} = 3.8 V

APPLICATION INFORMATION

A typical application circuits for NCP4682 and NCP4685 series is shown in Figure 58.

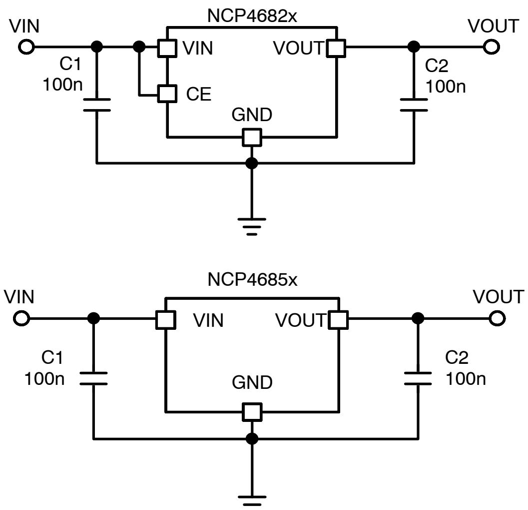


Figure 58. Typical Application Schematic

Input Decoupling Capacitor (C1)

A 0.1 μF ceramic input decoupling capacitor should be connected as close as possible to the input and ground pin of the NCP4682/5. Higher values and lower ESR improves line transient response.

Output Decoupling Capacitor (C2)

A 0.1 μF ceramic output decoupling capacitor is enough to achieve stable operation of the IC. If a tantalum capacitor is used, and its ESR is high, loop oscillation may result. The capacitors should be connected as close as possible to the output and ground pins. Larger values and lower ESR improves dynamic parameters.

Current Limit

This regulator includes a fold−back current limiting circuit. This type of protection doesn't limit output current up to specified current capability in normal operation, but when an over current situation occurs, the output voltage and current decrease until the over current condition ends. Typical characteristics of this protection scheme are shown in the Output voltage versus Output current graphs in the characterization section of this datasheet.

Enable Operation (NCP4682 Only)

The enable pin CE may be used for turning the regulator on and off. The IC is switched on when a high level voltage is applied to the CE pin. The enable pin has an internal pull down current source. If the enable function is not needed, connect CE pin to VIN.

Output Discharger (NCP4682 Only)

The NCP4682D version includes a transistor between VOUT and GND that is used for faster discharging of the output capacitor. This function is activated when the IC goes into disable mode.

Thermals

As a power across the IC increase, it might become necessary to provide some thermal relief. The maximum power dissipation supported by the device is dependent upon board design and layout. Mounting pad configuration on the PCB, the board material, and also the ambient temperature affect the rate of temperature increase for the part. When the device has good thermal conductivity through the PCB the junction temperature will be relatively low in high power dissipation applications.

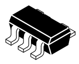
PCB layout

Make the VIN and GND line as large as practical. If their impedance is high, noise pickup or unstable operation may result. Connect capacitors C1 and C2 as close as possible to the IC, and make wiring as short as possible.

ORDERING INFORMATION

Device	Nominal Output Voltage	Description	Marking	Package	Shipping
NCP4682DMU12TCG	1.2 V	Auto discharge	CA	UDFN4 (Pb−Free)	10000 / Tape & Reel
NCP4682DMU15TCG	1.5 V	Auto discharge	CC		
NCP4682DMU18TCG	1.8 V	Auto discharge	CD		
NCP4682DMU19TCG	1.9 V	Auto discharge	CF		
NCP4682DMU25TCG	2.5 V	Auto discharge	CH		
NCP4682DMU28TCG	2.8 V	Auto discharge	CL		
NCP4682DMU30TCG	3.0 V	Auto discharge	CP		
NCP4682DMU33TCG	3.3 V	Auto discharge	CR		
NCP4682HMU18TCG	1.8 V	Enable high	AD		
NCP4682HMU28TCG	2.8 V	Enable high	AL		
NCP4682HMU33TCG	3.3 V	Enable high	AR		
NCP4685EMU30TCG	3.0 V	Without enable	BP		
NCP4682DSN30T1G	3.0 V	Auto discharge	92P	SOT−23−5 (Pb−Free)	3000 / Tape & Reel
NCP4682DSN33T1G	3.3 V	Auto discharge	92R		
NCP4682DSQ12T1G	1.2 V	Auto discharge	R0	SC−82AB (Pb−Free)	3000 / Tape & Reel
NCP4682DSQ15T1G	1.5 V	Auto discharge	R2		
NCP4682DSQ18T1G	1.8 V	Auto discharge	R3		
NCP4682DSQ20T1G	2.0 V	Auto discharge	R6		
NCP4682DSQ25T1G	2.5 V	Auto discharge	R7		
NCP4682DSQ28T1G	2.8 V	Auto discharge	S0		
NCP4682DSQ33T1G	3.3 V	Auto discharge	S5		
NCP4685ESQ15T1G	1.5 V	Without enable	N2		
NCP4685ESQ25T1G	2.5 V	Without enable	N7		
NCP4685ESQ33T1G	3.3 V	Without enable	P5		

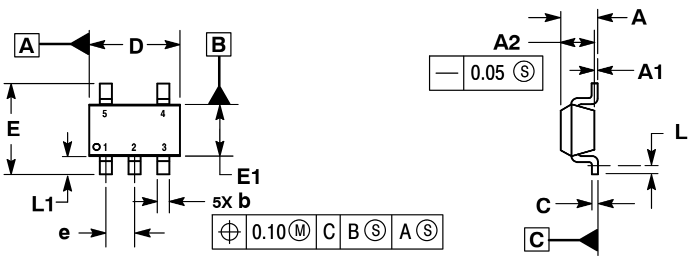
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
*To order other package and voltage variants, please contact your ON Semiconductor sales representative.



SCALE 2:1

SOT−23 5−LEAD
CASE 1212
ISSUE A

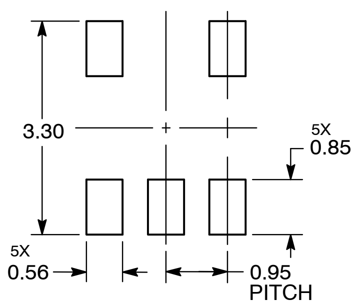
DATE 28 JAN 2011



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSIONS: MILLIMETERS.
3. DATUM C IS THE SEATING PLANE.

	MILLIMETERS	
DIM	MIN	MAX
A	---	1.45
A1	0.00	0.10
A2	1.00	1.30
b	0.30	0.50
c	0.10	0.25
D	2.70	3.10
E	2.50	3.10
E1	1.50	1.80
e	0.95 BSC	
L	0.20	---
L1	0.45	0.75

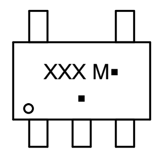
RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

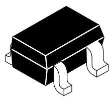
GENERIC MARKING DIAGRAM*



XXX = Specific Device Code
M = Date Code
▪ = Pb−Free Package
(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

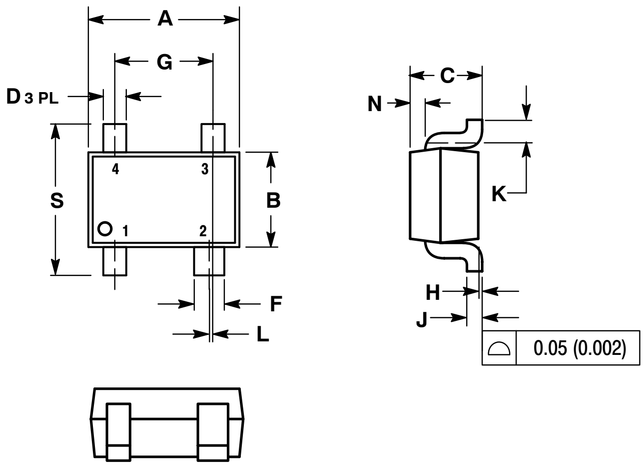
DOCUMENT NUMBER:	98ASH70518A	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	SOT−23 5−LEAD	PAGE 1 OF 1



SCALE 4:1

SC−82AB
CASE 419C−02
ISSUE F

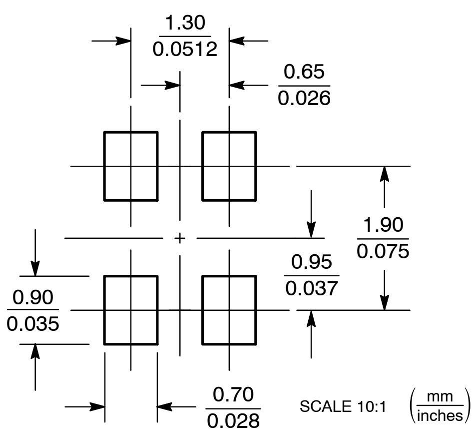
DATE 22 JUN 2012



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. 419C−01 OBSOLETE. NEW STANDARD IS 419C−02.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

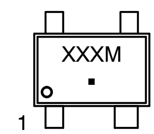
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	1.80	2.20	0.071	0.087
B	1.15	1.35	0.045	0.053
C	0.80	1.10	0.031	0.043
D	0.20	0.40	0.008	0.016
F	0.30	0.50	0.012	0.020
G	1.10	1.50	0.043	0.059
H	0.00	0.10	0.000	0.004
J	0.10	0.26	0.004	0.010
K	0.10	---	0.004	---
L	0.05 BSC		0.002 BSC	
N	0.20 REF		0.008 REF	
S	1.80	2.40	0.07	0.09

SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXX = Specific Device Code
M = Month Code
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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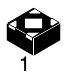
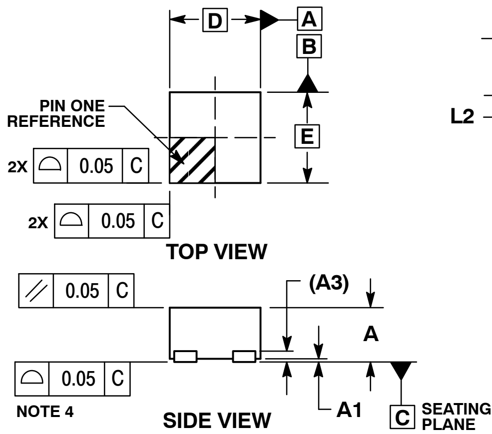
DESCRIPTION:	**SC−82AB**	**PAGE 1 OF 1**

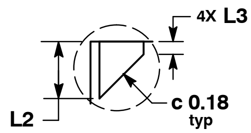


SCALE 4:1

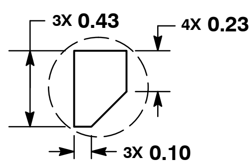
UDFN4 1.0x1.0, 0.65P
CASE 517BR
ISSUE O

DATE 27 OCT 2010

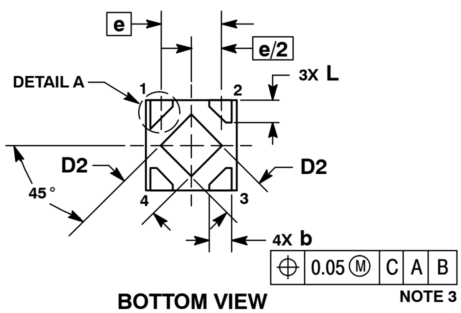




DETAIL A



DETAIL B

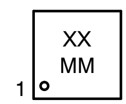


BOTTOM VIEW

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.20 mm FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	---	0.60
A1	0.00	0.05
A3	0.10 REF	
b	0.20	0.30
D	1.00 BSC	
D2	0.43	0.53
E	1.00 BSC	
e	0.65 BSC	
L	0.20	0.30
L2	0.27	0.37
L3	0.02	0.12

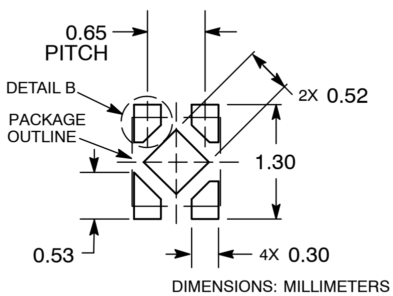
GENERIC MARKING DIAGRAM*



XX = Specific Device Code
MM = Date Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot " ▪", may or may not be present.

RECOMMENDED MOUNTING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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