

## Dual Ultrathin 2A or Single 4A Step-Down DC/DC $\mu$ Module Regulator

### FEATURES

- Complete Solution in  $<1\text{cm}^2$
- Wide Input Voltage Range: 3.6V to 20V
- 1.5V to 12V Output Voltage
- Dual 2A (3A Peak) or Single 4A Output Current
- $\pm 1.5\%$  Maximum Total Output Voltage Regulation Error Over Load, Line, and Temperature
- Current Mode Control, Fast Transient Response
- External Frequency Synchronization
- Multiphase Parallelable with Current Sharing
- Output Voltage Tracking and Soft-Start Capability
- Selectable Burst Mode<sup>®</sup> Operation
- Overvoltage Input and Overtemperature Protection
- Power Good Indicators
- 6.25mm  $\times$  6.25mm  $\times$  1.82mm LGA and 6.25mm  $\times$  6.25mm  $\times$  2.42mm BGA Packages

### APPLICATIONS

- General Purpose Point-of-Load Conversion
- Telecom, Networking, and Industrial Equipment
- Medical Diagnostic Equipment
- Test and Debug Systems

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### DESCRIPTION

The LTM<sup>®</sup>4622A is a complete dual 2A step-down switching mode  $\mu$ Module<sup>®</sup> (micromodule) regulator in a tiny ultrathin 6.25mm  $\times$  6.25mm  $\times$  1.82mm LGA and 2.42mm BGA packages. Included in the package is the switching controller, the power FETs, the inductor, and the supporting components. Operating over an input voltage range of 3.6V to 20V, the LTM4622A supports an output voltage range of 1.5V to 12V, set by a single external resistor. Its high efficiency design delivers dual 2A continuous, 3A peak, output current. Only a few ceramic input and output capacitors are needed.

The LTM4622A supports selectable Burst Mode operation and output voltage tracking for supply rail sequencing. Its high switching frequency and current mode control enable a very fast transient response to line and load changes without sacrificing stability.

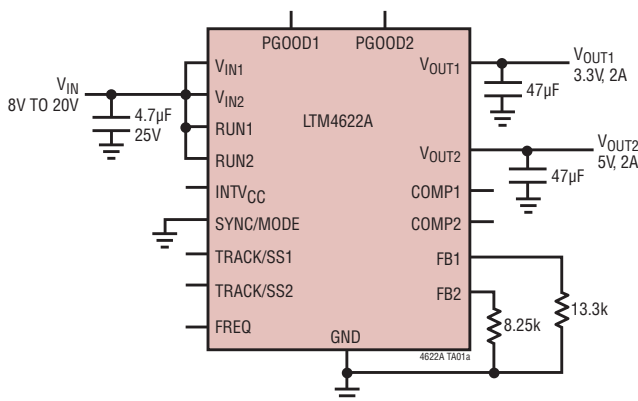
Fault protection features include input overvoltage, output overcurrent and overtemperature protection. The LTM4622A is available with SnPb (BGA) or RoHS-compliant terminal finish.

#### Product Selection Guide

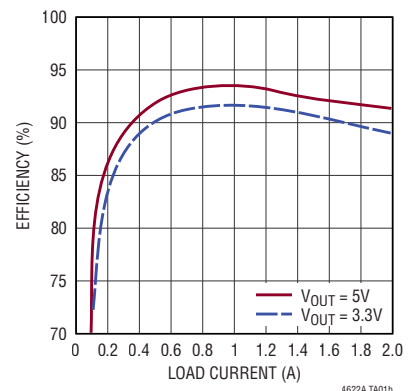
| PART NUMBER | V <sub>IN</sub> RANGE | V <sub>OUT</sub> RANGE | I <sub>OUT</sub>       |
|-------------|-----------------------|------------------------|------------------------|
| LTM4622     | 3.6V to 20V           | 0.6V to 5.5V           | Dual 2.5A or Single 5A |
| LTM4622A    |                       | 1.5V to 12V            | Dual 2A or Single 4A   |

### TYPICAL APPLICATION

#### 3.3V and 5V Dual Output DC/DC Step-Down $\mu$ Module Regulator



#### 12V Input, 3.3V and 5V Output, Efficiency vs Load Current

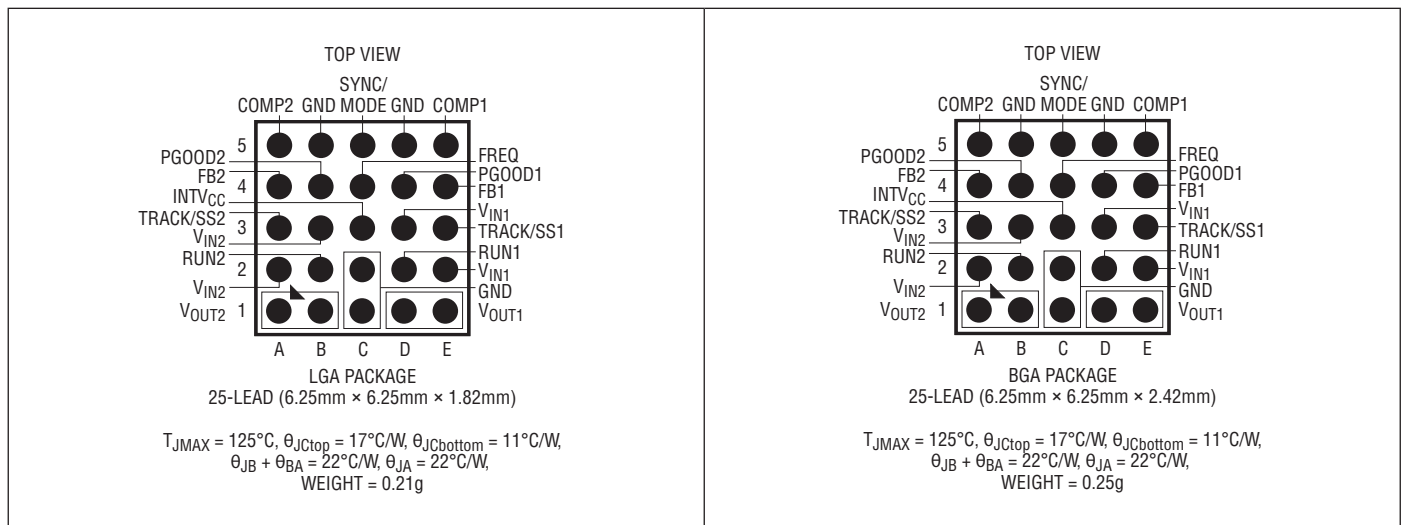


# LTM4622A

## ABSOLUTE MAXIMUM RATINGS (Note 1)

|   |                             |   |                |
|---|-----------------------------|---|----------------|
| $V_{IN1}, V_{IN2}$ .....                        | -0.3V to 22V                | Operating Internal Temperature Range      |                |
| $V_{OUT}$ .....                                 | -0.3V to 16V                | (Note 2) .....                            | -40°C to 125°C |
| PGOOD1, PGOOD2 .....                            | -0.3V to 18V                | Storage Temperature Range .....           | -55°C to 125°C |
| RUN1, RUN2 .....                                | -0.3V to $V_{IN} + 0.3V$    | Peak Solder Reflow Body Temperature ..... | 260°C          |
| INTV <sub>CC</sub> , TRACK/SS1, TRACK/SS2 ..... | -0.3V to 3.6V               |   |                |
| SYNC/MODE, COMP1, COMP2,                        |                             |   |                |
| FB1, FB2 .....                                  | -0.3V to INTV <sub>CC</sub> |   |                |

## PIN CONFIGURATION (See Pin Functions, Pin Configuration Table)



## ORDER INFORMATION

| PART NUMBER    | PAD OR BALL FINISH | PART MARKING* |             | PACKAGE TYPE | MSL RATING | TEMPERATURE RANGE (NOTE 2) |
|----------------|--------------------|---------------|-------------|--------------|------------|----------------------------|
|                |                    | DEVICE        | FINISH CODE |              |            |                            |
| LTM4622AEV#PBF | Au (RoHS)          | LTM4622AV     | e4          | LGA          | 4          | -40°C to 125°C             |
| LTM4622AIV#PBF | Au (RoHS)          | LTM4622AV     | e4          | LGA          | 4          | -40°C to 125°C             |
| LTM4622AEY#PBF | SAC305 (RoHS)      | LTM4622AY     | e1          | BGA          | 4          | -40°C to 125°C             |
| LTM4622AIY#PBF | SAC305 (RoHS)      | LTM4622AY     | e1          | BGA          | 4          | -40°C to 125°C             |
| LTM4622AIY     | SnPb (63/37)       | LTM4622AY     | e0          | BGA          | 4          | -40°C to 125°C             |

- Contact the factory for parts specified with wider operating temperature ranges. \*Pad or ball finish code is per IPC/JEDEC J-STD-609.
- [Recommended LGA and BGA PCB Assembly and Manufacturing Procedures](#)
- [LGA and BGA Package and Tray Drawings](#)

**ELECTRICAL CHARACTERISTICS** The ● denotes the specifications which apply over the specified internal operating temperature range (Note 2). Specified as each individual output channel at  $T_A = 25^\circ\text{C}$ ,  $V_{IN1} = V_{IN2} = 12\text{V}$ , unless otherwise noted per the typical application shown in Figure 27.

| SYMBOL  | PARAMETER  | CONDITIONS   | MIN          | TYP            | MAX          | UNITS                                |
|---|--|--|--------------|----------------|--------------|--------------------------------------|
| <b>Switching Regulator Section: per Channel</b> |  |  |              |                |              |                                      |
| $V_{IN1}$                                       | Input DC Voltage Range                             |  | ● 3.6        |                | 20           | V                                    |
| $V_{IN2}$                                       | Input DC Voltage Range                             | $3.6\text{V} < V_{IN1} < 20\text{V}$   | ● 1.5        |                | 20           | V                                    |
| $V_{OUT(\text{RANGE})}$                         | Output Voltage Range                               | $V_{IN1} = V_{IN2} = 3.6\text{V to } 20\text{V}$   | ● 1.5        |                | 12           | V                                    |
| $V_{OUT(\text{DC})}$                            | Output Voltage, Total Variation with Line and Load | $C_{IN} = 22\mu\text{F}$ , $C_{OUT} = 100\mu\text{F}$ Ceramic, $R_{FB} = 40.2\text{k}$ , $\text{MODE} = \text{INTV}_{\text{CC}}$ , $V_{IN1} = V_{IN2} = 3.6\text{V to } 20\text{V}$ , $I_{OUT} = 0\text{A to } 2\text{A}$                    | ● 1.477      | 1.50           | 1.523        | V                                    |
| $V_{\text{RUN}}$                                | RUN Pin On Threshold                               | RUN Threshold Rising<br>RUN Threshold Falling  | 1.20<br>0.97 | 1.27<br>1.00   | 1.35<br>1.03 | V<br>V                               |
| $I_{Q(\text{VIN})}$                             | Input Supply Bias Current                          | $V_{IN1} = V_{IN2} = 12\text{V}$ , $V_{OUT} = 1.5\text{V}$ , $\text{MODE} = \text{GND}$<br>$V_{IN1} = V_{IN2} = 12\text{V}$ , $V_{OUT} = 1.5\text{V}$ , $\text{MODE} = \text{INTV}_{\text{CC}}$<br>Shutdown, $\text{RUN1} = \text{RUN2} = 0$ |              | 7<br>500<br>45 |              | mA<br>$\mu\text{A}$<br>$\mu\text{A}$ |
| $I_{S(\text{VIN})}$                             | Input Supply Current                               | $V_{IN1} = V_{IN2} = 12\text{V}$ , $V_{OUT} = 1.5\text{V}$ , $I_{OUT} = 2\text{A}$   |              | 0.32           |              | A                                    |
| $I_{OUT(\text{DC})}$                            | Output Continuous Current Range                    | $V_{IN1} = V_{IN2} = 12\text{V}$ , $V_{OUT} = 1.5\text{V}$ (Note 3)  | ● 0          |                | 2            | A                                    |
| $\Delta V_{OUT(\text{Line})}/V_{OUT}$           | Line Regulation Accuracy                           | $V_{OUT} = 1.5\text{V}$ , $V_{IN1} = V_{IN2} = 3.6\text{V to } 20\text{V}$ , $I_{OUT} = 0\text{A}$   | ●            | 0.01           | 0.1          | %/V                                  |
| $\Delta V_{OUT(\text{Load})}/V_{OUT}$           | Load Regulation Accuracy                           | $V_{OUT} = 1.5\text{V}$ , $I_{OUT} = 0\text{A to } 2\text{A}$  | ●            | 0.2            | 1.0          | %                                    |
| $V_{OUT(\text{AC})}$                            | Output Ripple Voltage                              | $I_{OUT} = 0\text{A}$ , $C_{OUT} = 100\mu\text{F}$ Ceramic, $V_{IN1} = V_{IN2} = 12\text{V}$ , $V_{OUT} = 1.5\text{V}$   |              | 5              |              | mV                                   |
| $\Delta V_{OUT(\text{START})}$                  | Turn-On Overshoot                                  | $I_{OUT} = 0\text{A}$ , $C_{OUT} = 100\mu\text{F}$ Ceramic, $V_{IN1} = V_{IN2} = 12\text{V}$ , $V_{OUT} = 1.5\text{V}$   |              | 30             |              | mV                                   |
| $t_{\text{START}}$                              | Turn-On Time                                       | $C_{OUT} = 100\mu\text{F}$ Ceramic, No Load, $\text{TRACK}/\text{SS} = 0.01\mu\text{F}$ , $V_{IN1} = V_{IN2} = 12\text{V}$ , $V_{OUT} = 1.5\text{V}$   |              | 5.5            |              | ms                                   |
| $\Delta V_{OUT\text{LS}}$                       | Peak Deviation for Dynamic Load                    | Load: 0% to 50% to 0% of Full Load, $C_{OUT} = 100\mu\text{F}$ Ceramic, $V_{IN1} = V_{IN2} = 12\text{V}$ , $V_{OUT} = 1.5\text{V}$   |              | 100            |              | mV                                   |
| $t_{\text{SETTLE}}$                             | Settling Time for Dynamic Load Step                | Load: 0% to 50% to 0% of Full Load, $C_{OUT} = 100\mu\text{F}$ Ceramic, $V_{IN1} = V_{IN2} = 12\text{V}$ , $V_{OUT} = 1.5\text{V}$   |              | 20             |              | $\mu\text{s}$                        |
| $I_{OUT\text{PK}}$                              | Output Current Limit                               | $V_{IN1} = V_{IN2} = 12\text{V}$ , $V_{OUT} = 1.5\text{V}$   | 3            | 4              |              | A                                    |
| $V_{\text{FB}}$                                 | Voltage at FB Pin                                  | $I_{OUT} = 0\text{A}$ , $V_{OUT} = 1.5\text{V}$  | ● 0.592      | 0.60           | 0.608        | V                                    |
| $I_{\text{FB}}$                                 | Current at FB Pin                                  | (Note 4)   |              |                | $\pm 30$     | nA                                   |
| $R_{\text{FBHI}}$                               | Resistor Between $V_{OUT}$ and FB Pins             |  | 60.00        | 60.40          | 60.80        | k $\Omega$                           |
| $I_{\text{TRACK}/\text{SS}}$                    | Track Pin Soft-Start Pull-Up Current               | $\text{TRACK}/\text{SS} = 0\text{V}$   |              | 1.2            |              | $\mu\text{A}$                        |
| $t_{\text{SS}}$                                 | Internal Soft-Start Time                           | 10% to 90% Rise Time (Note 4)  |              | 400            | 700          | $\mu\text{s}$                        |
| $t_{\text{ON}(\text{MIN})}$                     | Minimum On-Time                                    | (Note 4)   |              | 20             |              | ns                                   |
| $t_{\text{OFF}(\text{MIN})}$                    | Minimum Off-Time                                   | (Note 4)   |              | 45             |              | ns                                   |
| $V_{\text{PGOOD}}$                              | PGOOD Trip Level                                   | $V_{\text{FB}}$ With Respect to Set Output<br>$V_{\text{FB}}$ Ramping Negative<br>$V_{\text{FB}}$ Ramping Positive   |              | -8<br>8        | -14<br>14    | %<br>%                               |
| $R_{\text{PGOOD}}$                              | PGOOD Pull-Down Resistance                         | 1mA Load   |              | 20             |              | $\Omega$                             |
| $V_{\text{INTV}_{\text{CC}}}$                   | Internal $V_{\text{CC}}$ Voltage                   | $V_{IN1} = V_{IN2} = 3.6\text{V to } 20\text{V}$   | 3.1          | 3.3            | 3.5          | V                                    |
| $V_{\text{INTV}_{\text{CC}}}$ Load Reg          | INTV <sub>CC</sub> Load Regulation                 | $I_{\text{CC}} = 0\text{mA to } 50\text{mA}$   |              | 1.3            |              | %                                    |
| $f_{\text{OSC}}$                                | Oscillator Frequency                               |  |              | 1              |              | MHz                                  |
| $f_{\text{SYNC}}$                               | Frequency Sync Range                               | With Respect to Set Frequency  |              | $\pm 30$       |              | %                                    |
| $I_{\text{MODE}}$                               | MODE Input Current                                 | $\text{MODE} = \text{INTV}_{\text{CC}}$  |              | -1.5           |              | $\mu\text{A}$                        |

## ELECTRICAL CHARACTERISTICS

**Note 1:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

**Note 2:** The LTM4622A is tested under pulsed load conditions such that  $T_J \approx T_A$ . The LTM4622AE is guaranteed to meet performance specifications over the 0°C to 125°C internal operating temperature range. Specifications over the full -40°C to 125°C internal operating temperature range are assured by design, characterization, and correlation with statistical process controls. The LTM4622AI is guaranteed to meet specifications over the full -40°C to 125°C internal operating temperature range. Note that the maximum ambient temperature consistent with

these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal resistance, and other environmental factors.

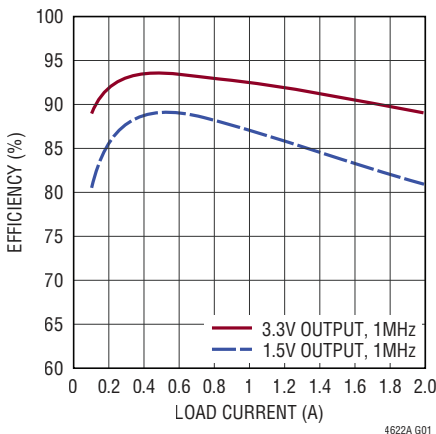
**Note 3:** See the Thermal Considerations and Output Current Derating in the Applications Information section for different  $V_{IN}$ ,  $V_{OUT}$ , and  $T_A$ .

**Note 4:** 100% tested at wafer level.

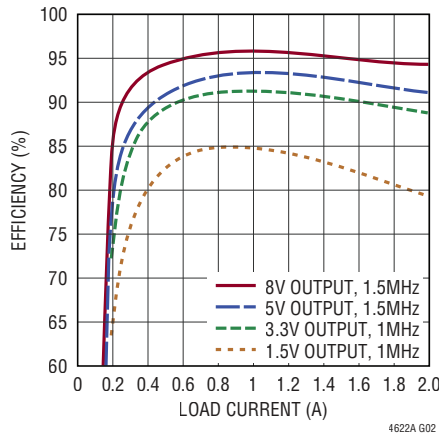
**Note 5:** This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed 125°C when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

## TYPICAL PERFORMANCE CHARACTERISTICS

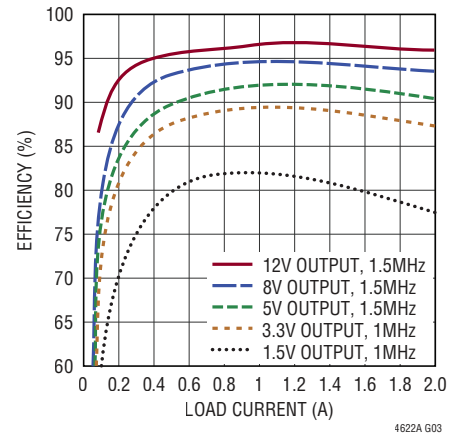
**Efficiency vs Load Current at 5V<sub>IN</sub>**



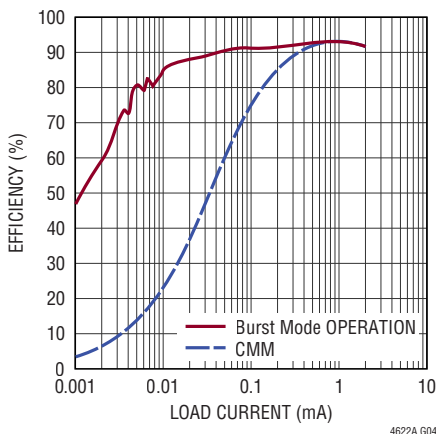
**Efficiency vs Load Current at 12V<sub>IN</sub>**



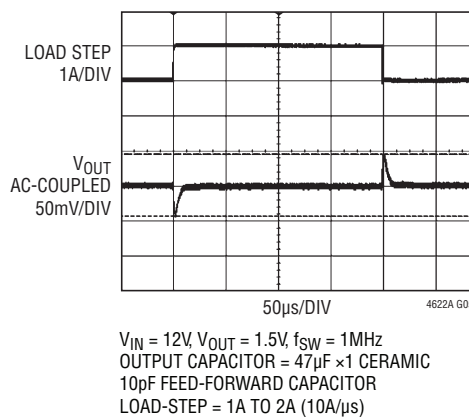
**Efficiency vs Load Current at 16V<sub>IN</sub>**



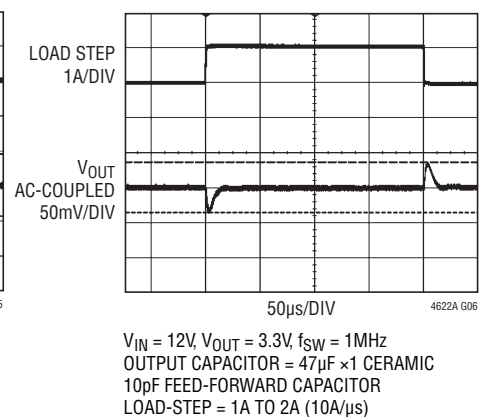
**Burst Mode Efficiency, 12V<sub>IN</sub>, 1.5V<sub>OUT</sub>**



**1.5V Output Transient Response**

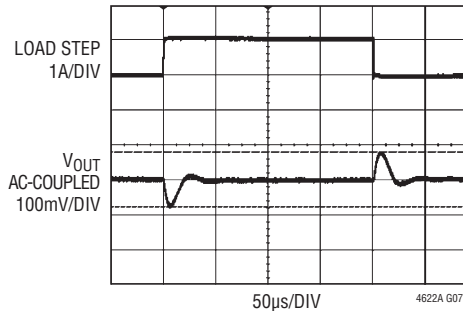


**3.3V Output Transient Response**



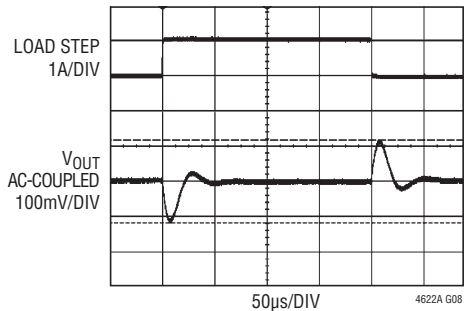
# TYPICAL PERFORMANCE CHARACTERISTICS

**5V Output Transient Response**



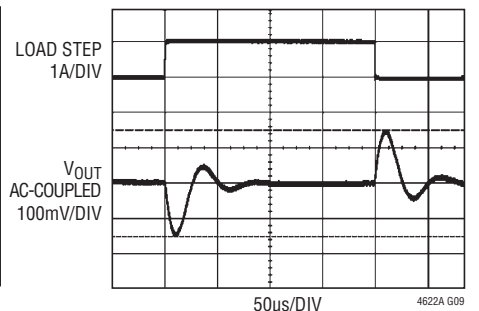
$V_{IN} = 12V$ ,  $V_{OUT} = 5V$ ,  $f_{SW} = 1MHz$   
 OUTPUT CAPACITOR =  $47\mu F \times 2$  CERAMIC  
 10pF FEED-FORWARD CAPACITOR  
 LOAD-STEP = 1A TO 2A (10A/µs)

**8V Output Transient Response**



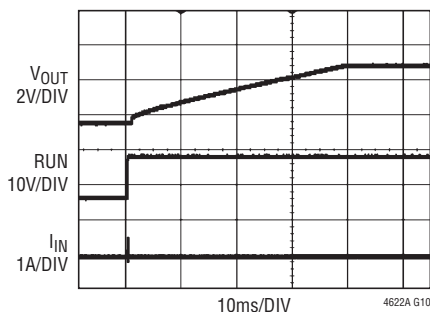
$V_{IN} = 12V$ ,  $V_{OUT} = 8V$ ,  $f_{SW} = 1.5MHz$   
 OUTPUT CAPACITOR =  $47\mu F \times 2$  CERAMIC  
 10pF FEED-FORWARD CAPACITOR  
 LOAD-STEP = 1A TO 2A (10A/µs)

**12V Output Transient Response**



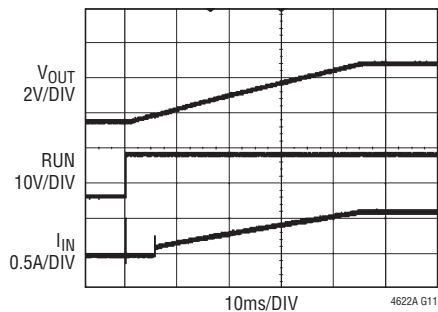
$V_{IN} = 16V$ ,  $V_{OUT} = 12V$ ,  $f_{SW} = 1.5MHz$   
 OUTPUT CAPACITOR =  $47\mu F \times 2$  CERAMIC  
 10pF FEED-FORWARD CAPACITOR  
 LOAD-STEP = 1A TO 2A (10A/µs)

**Start-Up with No Load Current Applied**



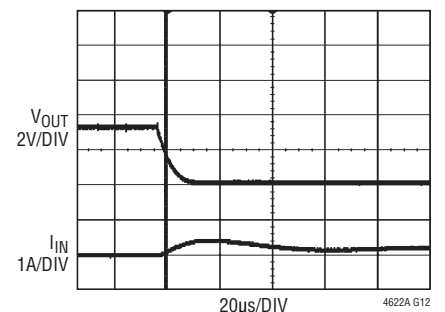
$V_{IN} = 12V$ ,  $V_{OUT} = 3.3V$ ,  $f_{SW} = 1MHz$   
 OUTPUT CAPACITOR = 10µF CERAMIC  
 + 47µF POSCAP  
 SOFT-START CAP = 0.1µF

**Start-Up with 2A Load Current Applied**



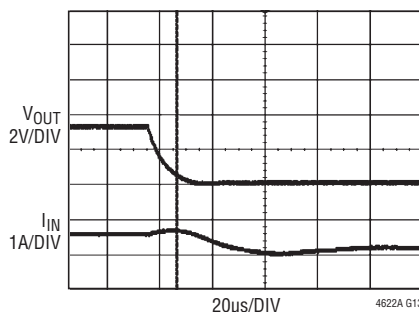
$V_{IN} = 12V$ ,  $V_{OUT} = 3.3V$ ,  $f_{SW} = 1MHz$   
 OUTPUT CAPACITOR = 10µF CERAMIC  
 + 47µF POSCAP  
 SOFT-START CAP = 0.1µF

**Short-Circuit with No Load Current Applied**



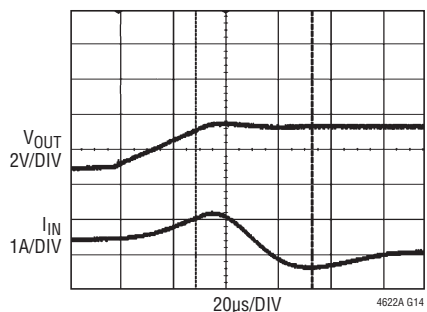
$V_{IN} = 12V$ ,  $V_{OUT} = 3.3V$ ,  $f_{SW} = 1MHz$   
 OUTPUT CAPACITOR = 10µF CERAMIC  
 + 47µF POSCAP

**Short-Circuit with 2A Load Current Applied**



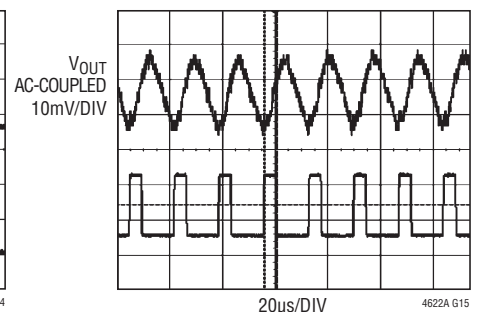
$V_{IN} = 12V$ ,  $V_{OUT} = 3.3V$ ,  $f_{SW} = 1MHz$   
 OUTPUT CAPACITOR = 10µF + 47µF POSCAP

**Recover from Short-Circuit with No Load Current Applied**



$V_{IN} = 12V$ ,  $V_{OUT} = 3.3V$ ,  $f_{SW} = 1MHz$   
 OUTPUT CAPACITOR = 10µF + 47µF POSCAP

**Steady-State Output Voltage Ripple**



$V_{IN} = 12V$ ,  $V_{OUT} = 3.3V$ ,  $f_{SW} = 1MHz$   
 OUTPUT CAPACITOR = 10µF + 47µF POSCAP

## PIN FUNCTIONS



PACKAGE ROW AND COLUMN LABELING MAY VARY AMONG  $\mu$ Module PRODUCTS. REVIEW EACH PACKAGE LAYOUT CAREFULLY.

**GND (Pins C1, C2, B5, D5):** Power Ground Pins for Both Input and Output Returns.

**INTV<sub>CC</sub> (Pin C3):** Internal 3.3V Regulator Output. The internal power drivers and control circuits are powered from this voltage. This pin is internally decoupled to GND with a 2.2 $\mu$ F low ESR ceramic capacitor. No additional external decoupling capacitor needed.

**FREQ (Pin C4):** Frequency is set internally to 1MHz. An external resistor can be placed from this pin to GND to increase frequency, or from this pin to INTV<sub>CC</sub> to reduce frequency. See the Applications Information section for frequency adjustment.

**SYNC/MODE (Pin C5):** Mode Select and External Synchronization Input. Tie this pin to ground to force continuous synchronous operation at all output loads. Floating this pin or tying it to INTV<sub>CC</sub> enables high efficiency Burst Mode operation at light loads. Drive this pin with a clock to synchronize the LTM4622A switching frequency. An internal phase-locked loop will force the bottom power NMOS's turn on signal to be synchronized with the rising edge of the clock signal. When this pin is driven with a clock, forced continuous mode is automatically selected.

**V<sub>OUT1</sub> (Pins D1, E1), V<sub>OUT2</sub> (Pins A1, B1):** Power Output Pins of Each Switching Mode Regulator. Apply output load between these pins and GND pins. Recommend placing output decoupling capacitance directly between these pins and GND pins.

**RUN1 (Pin D2), RUN2 (Pin B2):** Run Control Input of Each Switching Mode Regulator Channel. Enables chip operation by tying RUN above 1.27V. Tying this pin below 1V shuts down the specific regulator channel. Do not float this pin.

**V<sub>IN1</sub> (Pins D3, E2), V<sub>IN2</sub> (Pins A2, B3):** Power Input Pins. Apply input voltage between these pins and GND pins. Recommend placing input decoupling capacitance directly between BOTH V<sub>IN1</sub> and V<sub>IN2</sub> pins and GND pins. Please note the module internal control circuitry is running off V<sub>IN1</sub>. Channel 2 will not work without a voltage higher than 3.6V presents at V<sub>IN1</sub>.

**PGOOD1 (Pin D4), PGOOD2 (Pin B4):** Output Power Good with Open-Drain Logic of Each Switching Mode Regulator Channel. PGOOD is pulled to ground when the voltage on the FB pin is not within  $\pm 8\%$  (typical) of the internal 0.6V reference.

**TRACK/SS1 (Pin E3), TRACK/SS2 (Pin A3):** Output Tracking and Soft-Start Pin of Each Switching Mode Regulator Channel. It allows the user to control the rise time of the output voltage. Putting a voltage below 0.6V on this pin bypasses the internal reference input to the error amplifier, instead it servos the FB pin to the TRACK voltage. Above 0.6V, the tracking function stops and the internal reference resumes control of the error amplifier. There's an internal 1.2 $\mu$ A pull-up current from INTV<sub>CC</sub> on this pin, so putting a capacitor here provides soft-start function. A default internal soft-start ramp forces a minimum soft-start time of 400 $\mu$ s.

**FB1 (Pin E4), FB2 (Pin A4):** The Negative Input of the Error Amplifier for Each Switching Mode Regulator Channel. Internally, this pin is connected to V<sub>OUT</sub> with a 60.4k precision resistor. Different output voltages can be programmed with an additional resistor between FB and GND pins. In PolyPhase<sup>®</sup> operation, tying the FB pins together allows for parallel operation. See the Applications Information section for details.

**COMP1 (Pin E5), COMP2 (Pin A5):** Current Control Threshold and Error Amplifier Compensation Point of Each Switching Mode Regulator Channel. The current comparator's trip threshold is linearly proportional to this voltage, whose normal range is from 0.3V to 1.8V. Tie the COMP pins together for parallel operation. The device is internal compensated. Do not drive this pin.

## BLOCK DIAGRAM

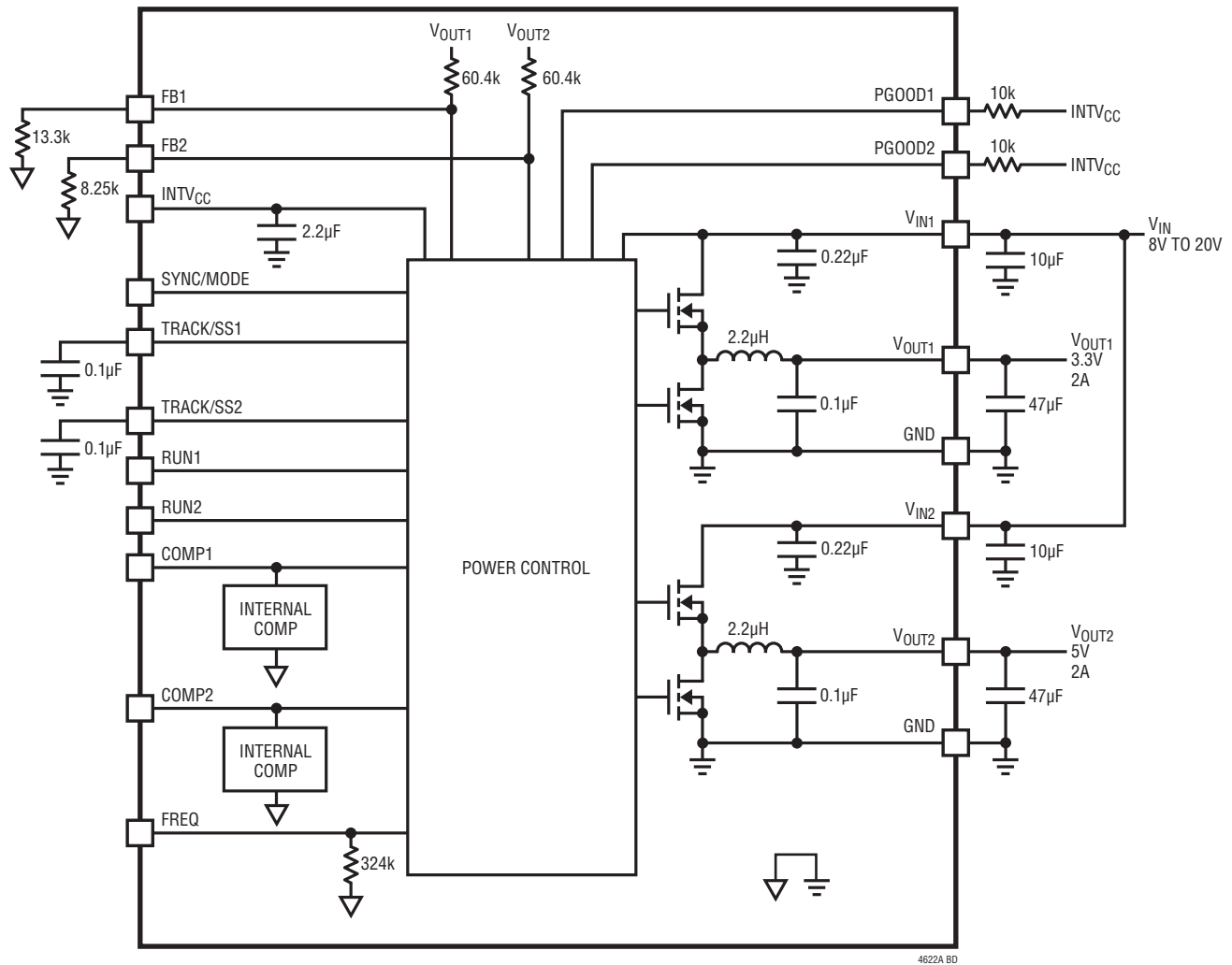


Figure 1. Simplified LTM4622A Block Diagram

## DECOUPLING REQUIREMENTS

| SYMBOL    | PARAMETER   | CONDITIONS     | MIN | TYP | MAX | UNITS   |
|-----------|---|----------------|-----|-----|-----|---------|
| $C_{IN}$  | External Input Capacitor Requirement ( $V_{IN} = 3.6V$ to $20V$ , $V_{OUT} = 1.5V$ )  | $I_{OUT} = 2A$ | 4.7 | 10  |     | $\mu F$ |
| $C_{OUT}$ | External Output Capacitor Requirement ( $V_{IN} = 3.6V$ to $20V$ , $V_{OUT} = 1.5V$ ) | $I_{OUT} = 2A$ | 22  | 47  |     | $\mu F$ |



## OPERATION

The LTM4622A is a dual output standalone non-isolated switch mode DC/DC power supply. It can deliver two 2A DC, 3A peak output current with few external input and output ceramic capacitors. This module provides dual precisely regulated output voltage programmable via two external resistor from 1.5V to 12V over 3.6V to 20V input voltage range. The typical application schematic is shown in Figure 27.

The LTM4622A contains an integrated controlled on-time valley current mode regulator, power MOSFETs, inductors, and other supporting discrete components. The default switching frequency is 1MHz. For output voltages above 3.3V, an external resistor is required between **FREQ** and **GND** pins to set the operating frequency to 1.5MHz to 2MHz to optimize inductor current ripple. For switching noise-sensitive applications, the switching frequency can be adjusted by external resistors and the  $\mu$ Module regulator can be externally synchronized to a clock within  $\pm 30\%$  of the set frequency. See the Applications Information section.

With current mode control and internal feedback loop compensation, the LTM4622A module has sufficient

stability margins and good transient performance with a wide range of output capacitors, even with all ceramic output capacitors.

Current mode control provides cycle-by-cycle fast current limiting. An internal overvoltage and undervoltage comparators pull the open-drain **PGOOD** output low if the output feedback voltage exits a  $\pm 8\%$  window around the regulation point. Furthermore, an input overvoltage protection been utilized by shutting down both power MOSFETs when  $V_{IN}$  rises above 22.5V to protect internal devices.

Multiphase operation can be easily employed by connecting **SYNC** pin to an external oscillator. Up to 6 phases can be paralleled to run simultaneously a good current sharing guaranteed by current mode control loop.

Pulling the **RUN** pin below 1V forces the controller into its shutdown state, turning off both power MOSFETs and most of the internal control circuitry. At light load currents, Burst Mode operation can be enabled to achieve higher efficiency compared to continuous mode (CCM) by setting **MODE** pin to **INTV<sub>CC</sub>**. The **TRACK/SS** pin is used for power supply tracking and soft-start programming. See the Applications Information section.

## APPLICATIONS INFORMATION

The typical LTM4622A application circuit is shown in Figure 27. External component selection is primarily determined by the input voltage, the output voltage and the maximum load current. See Table 7 for specific external capacitor requirements for a particular application.

### **V<sub>IN</sub> to V<sub>OUT</sub> Step-Down Ratios**

There are restrictions in the maximum  $V_{IN}$  and  $V_{OUT}$  step down ratio that can be achieved for a given input voltage due to the minimum off-time and minimum on-time limits of the regulator. The minimum off-time limit imposes a maximum duty cycle which can be calculated as:

$$DC_{(MAX)} = 1 - t_{OFF(MIN)} \cdot f_{SW}$$

where  $t_{OFF(MIN)}$  is the minimum off-time, 45ns typical for LTM4622A, and  $f_{SW}$  is the switching frequency. Conversely the minimum on-time limit imposes a minimum duty cycle of the converter which can be calculated as:

$$DC_{(MIN)} = t_{ON(MIN)} \cdot f_{SW}$$

where  $t_{ON(MIN)}$  is the minimum on-time, 20ns typical for LTM4622A. In the rare cases where the minimum duty cycle is surpassed, the output voltage will still remain in regulation, but the switching frequency will decrease from its programmed value. Note that additional thermal derating may be applied. See the Thermal Considerations and Output Current Derating section in this data sheet.



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### Output Voltage Programming

The PWM controller has an internal 0.6V reference voltage. As shown in the Block Diagram, a 60.4k 0.5% internal feedback resistor connects  $V_{OUT}$  and FB pins together. Adding a resistor  $R_{FB}$  from FB pin to GND programs the output voltage:

$$R_{FB} = \frac{0.6V}{V_{OUT} - 0.6V} \cdot 60.4k$$

**Table 1.  $V_{FB}$  Resistor Table vs Various Output Voltages (1% Resistor)**

| $V_{OUT}$ (V) | 1.5  | 1.8  | 2.5  | 3.3  | 5.0  | 8.0  | 10.0 | 12.0 |
|---------------|------|------|------|------|------|------|------|------|
| $R_{FB}$ (k)  | 40.2 | 30.1 | 19.1 | 13.3 | 8.25 | 4.87 | 3.83 | 3.16 |

Please note that for output above 3.3V, a higher operating frequency is required to optimize inductor current ripple. See Operating Frequency section.

For parallel operation of N-channels LTM4622A, the following equation can be used to solve for  $R_{FB}$ :

$$R_{FB} = \frac{0.6V}{V_{OUT} - 0.6V} \cdot \frac{60.4k}{N}$$

### Input Decoupling Capacitors

The LTM4622A module should be connected to a low AC-impedance DC source. For each regulator channel, one piece 4.7 $\mu$ F input ceramic capacitor is required for RMS ripple current decoupling. Bulk input capacitor is only needed when the input source impedance is compromised by long inductive leads, traces or not enough source capacitance. The bulk capacitor can be an electrolytic aluminum capacitor and polymer capacitor.

Without considering the inductor current ripple, for each output, the RMS current of the input capacitor can be estimated as:

$$I_{CIN(RMS)} = \frac{I_{OUT(MAX)}}{\eta\%} \cdot \sqrt{D \cdot (1-D)}$$

where  $\eta$  is the estimated efficiency of the power module.

### Output Decoupling Capacitors

With an optimized high frequency, high bandwidth design, only single piece of 47 $\mu$ F low ESR output ceramic capacitor is required for each LTM4622A output to achieve low output voltage ripple and very good transient response. Additional output filtering may be required by the system designer, if further reduction of output ripples or dynamic transient spikes is required. Table 7 shows a matrix of different output voltages and output capacitors to minimize the voltage droop and overshoot during a 1A (50%) load step transient. Multiphase operation will reduce effective output ripple as a function of the number of phases. The [Application Note 77](#) discusses this noise reduction versus output ripple current cancellation, but the output capacitance will be more a function of stability and transient response. The Analog Devices [LTpowerCAD](#)<sup>®</sup> design tool is available to download online for output ripple, stability and transient response analysis and calculating the output ripple reduction as the number of phases implemented increases by N times.

### Burst Mode Operation

In applications where high efficiency at intermediate current are more important than output voltage ripple, Burst Mode operation could be used by connecting SYNC/MODE pin to INTV<sub>CC</sub> to improve light load efficiency. In Burst Mode operation, a current reversal comparator ( $I_{REV}$ ) detects the negative inductor current and shuts off the bottom power MOSFET, resulting in discontinuous operation and increased efficiency. Both power MOSFETs will remain off and the output capacitor will supply the load current until the COMP voltage rises above the zero current level to initiate another cycle.

### Forced Continuous Mode (FCM) Operation

In applications where fixed frequency operation is more critical than low current efficiency, and where the lowest output ripple is desired, FCM operation should be used. The FCM operation can be enabled by tying the SYNC/MODE pin to GND. In this mode, inductor current is allowed to reverse during low output loads, the COMP voltage is in control of the current comparator threshold throughout, and the top MOSFET always turns on with

## APPLICATIONS INFORMATION

each oscillator pulse. During start-up, FCM is disabled and inductor current is prevented from reversing until the LTM4622A's output voltage is in regulation.

### Operating Frequency

The operating frequency of the LTM4622A is optimized to achieve the compact package size and the minimum output ripple voltage while still keeping high efficiency. The default operating frequency is internally set to 1MHz.

If any operating frequency other than 1MHz is required by application, the operating frequency can be increased by adding a resistor,  $R_{FSET}$ , between the FREQ pin and GND, as shown in Figure 29. The operating frequency can be calculated as:

$$f(\text{Hz}) = \frac{3.2e11}{324k \parallel R_{FSET}(\Omega)}$$

Please note a minimum switching frequency is required for given  $V_{IN}$ ,  $V_{OUT}$  operating conditions to keep a maximum peak-to-peak inductor ripple current below 1.2A for the LTM4622A.

The peak-to-peak inductor ripple current can be calculated as:

$$\Delta I_{P-P} = \frac{V_{OUT}}{2.2} \left( 1 - \frac{V_{OUT}}{V_{IN}} \right) \cdot \frac{1}{f_{SW}(\text{MHz})}$$

The maximum 1.2A peak-to-peak inductor ripple current is enforced due to the nature of the valley current mode control to maintain output voltage regulation at no load.

To reduce switching current ripple, 1.5MHz to 2MHz operating frequency is suggested for 5V and above output with  $R_{FSET}$  to GND.

| $V_{OUT}$ | 1.5V to 3.3V | 5V, 8V | 12V            |
|-----------|--------------|--------|----------------|
| $f_{SW}$  | 1MHz         | 1.5MHz | 1.5MHz to 2MHz |

The operating frequency can also be decreased by adding a resistor between the FREQ pin and  $INTV_{CC}$ , calculated as:

$$f(\text{Hz}) = 1\text{MHz} - \frac{5.67e11}{R_{FSET}(\Omega)}$$

The programmable operating frequency range is from 800kHz to 4MHz.

### Frequency Synchronization

The power module has a phase-locked loop comprised of an internal voltage controlled oscillator and a phase detector. This allows the internal top MOSFET turn-on to be locked to the rising edge of the external clock. The external clock frequency range must be within  $\pm 30\%$  around the set operating frequency. A pulse detection circuit is used to detect a clock on the SYNC/MODE pin to turn on the phase-locked loop. The pulse width of the clock has to be at least 100ns. The clock high level must be above 2V and clock low level below 0.3V. The presence of an external clock will place both regulator channels into FCM operation. During the start-up of the regulator, the phase-locked loop function is disabled.

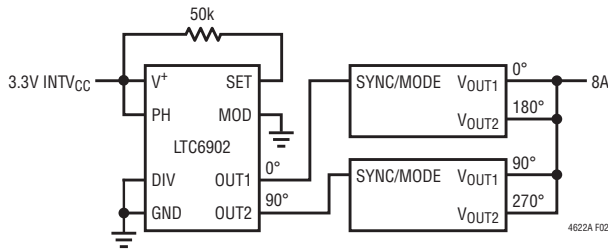
### Multiphase Operation

For output loads that demand more than 2A of current, two outputs in the LTM4622A or even multiple LTM4622As can be paralleled to run out of phase to provide more output current without increasing input and output voltage ripples.

A multiphase power supply significantly reduces the amount of ripple current in both the input and output capacitors. The RMS input ripple current is reduced by, and the effective ripple frequency is multiplied by, the number of phases used (assuming that the input voltage is greater than the number of phases used times the output voltage). The output ripple amplitude is also reduced by the number of phases used when all of the outputs are tied together to achieve a single high output current design.

The two switching mode regulator channels inside the LTM4622A are internally set to operate 180° out of phase. Multiple LTM4622As could easily operate 90 degrees, 60 degrees or 45 degrees shift which corresponds to 4-phase, 6-phase or 8-phase operation by letting SYNC/MODE of the LTM4622A synchronize to an external multiphase oscillator like the LTC®6902. Figure 2 shows a 4-phase design example for clock phasing.

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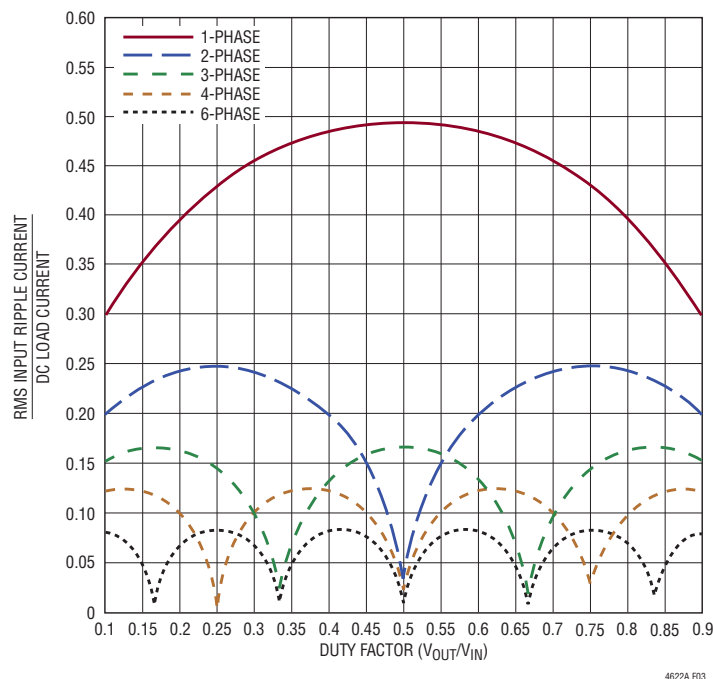


**Figure 2. Example of Clock Phasing for 4-Phase Operation with LTC6902**

The LTM4622A device is an inherently current mode controlled device, so parallel modules will have very good current sharing. This will balance the thermals on the design. Please tie RUN, TRACK/SS, FB and COMP pin of each paralleling channel together. Figure 31 shows an example of parallel operation and pin connection.

### Input RMS Ripple Current Cancellation

The [Application Note 77](#) provides a detailed explanation of multiphase operation. The input RMS ripple current cancellation mathematical derivations are presented, and a graph is displayed representing the RMS ripple current reduction as a function of the number of interleaved phases. Figure 3 shows this graph.



**Figure 3. Input RMS Current Ratios to DC Load Current as a Function of Duty Cycle**

### Soft-Start and Output Voltage Tracking

The TRACK/SS pin provides a means to either soft-start the regulator or track it to a different power supply. A capacitor on the TRACK/SS pin will program the ramp rate of the output voltage. An internal 1.2μA current source will charge up the external soft-start capacitor towards INTV<sub>CC</sub> voltage. When the TRACK/SS voltage is below 0.6V, it will take over the internal 0.6V reference voltage to control the output voltage. The total soft-start time can be calculated as:

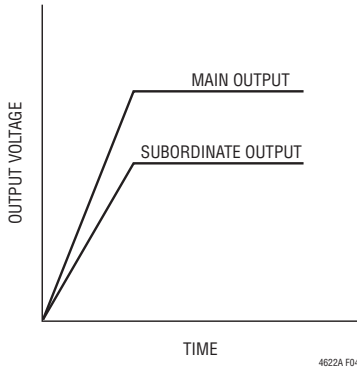
$$t_{SS} = 0.6 \cdot \frac{C_{SS}}{1.2\mu A}$$

where  $C_{SS}$  is the capacitance on the TRACK/SS pin. Current foldback and FCM are disabled during the soft-start process.

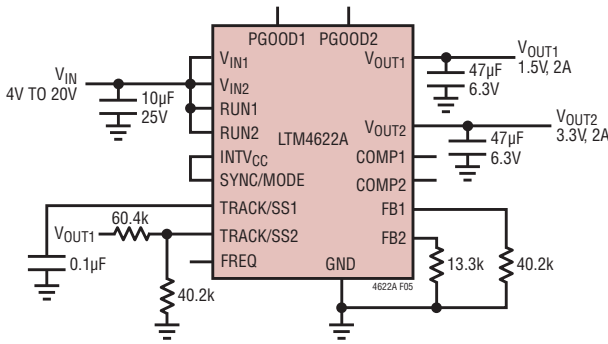
The LTM4622A has internal 400μs soft-start time when TRACK/SS leave floating.

Output voltage tracking can also be programmed externally using the TRACK/SS pin. The output can be tracked up and down with another regulator. Figure 4 and Figure 5 show an example waveform and schematic of a

## APPLICATIONS INFORMATION



**Figure 4. Output Ratiometric Tracking Waveform**



**Figure 5. Example Schematic of Ratiometric Output Voltage Tracking**

Ratiometric tracking where the subordinate regulator's output slew rate is proportional to the main's.

Since the subordinate regulator's TRACK/SS is connected to the main's output through a  $R_{TR(TOP)}/R_{TR(BOT)}$  resistor divider and its voltage used to regulate the subordinate output voltage when TRACK/SS voltage is below 0.6V, the subordinate output voltage and the main output voltage should satisfy the following equation during the start-up.

$$V_{OUT(SL)} \cdot \frac{R_{FB(SL)}}{R_{FB(SL)} + 60.4k} = V_{OUT(MA)} \cdot \frac{R_{TR(BOT)}}{R_{TR(TOP)} + R_{TR(BOT)}}$$

The  $R_{FB(SL)}$  is the feedback resistor and the  $R_{TR(TOP)}/R_{TR(BOT)}$  is the resistor divider on the TRACK/SS pin of the subordinate regulator, as shown in Figure 5.

Following the upper equation, the main's output slew rate (MR) and the subordinate's output slew rate (SR) in Volts/Time is determined by:

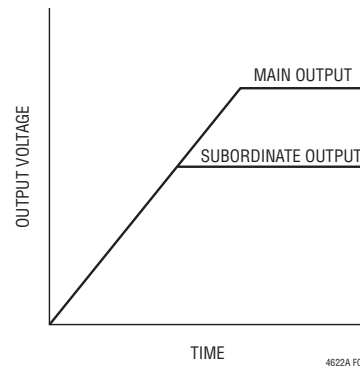
$$\frac{MR}{SR} = \frac{\frac{R_{FB(SL)}}{R_{FB(SL)} + 60.4k}}{R_{TR(TOP)} + R_{TR(BOT)}}$$

For example,  $V_{OUT(MA)} = 1.5V$ ,  $MR = 1.5V/ms$  and  $V_{OUT(SL)} = 3.3V$ ,  $SR = 3.3V/ms$ . From the equation, we could solve out that  $R_{TR(TOP)} = 60.4k$  and  $R_{TR(BOT)} = 40.2k$  is a good combination for the Ratiometric tracking.

The TRACK pins will have the 1.2µA current source on when a resistive divider is used to implement tracking on that specific channel. This will impose an offset on the TRACK pin input. Smaller values resistors with the same ratios as the resistor values calculated from the above equation can be used. For example, where the 60.4k is used then a 6.04k can be used to reduce the TRACK pin offset to a negligible value.

The Coincident output tracking can be recognized as a special Ratiometric output tracking which the main's output slew rate (MR) is the same as the subordinate's output slew rate (SR), as waveform shown in Figure 6.

From the following equation, we could easily find out that, in the coincident tracking, the subordinate regulator's TRACK/SS pin resistor divider is always the same as its feedback divider.



**Figure 6. Output Coincident Tracking Waveform**

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$$\frac{R_{FB(SL)}}{R_{FB(SL)} + 60.4k} = \frac{R_{TR(BOT)}}{R_{TR(TOP)} + R_{TR(BOT)}}$$

For example,  $R_{TR(TOP)} = 60.4k$  and  $R_{TR(BOT)} = 13.3k$  is a good combination for coincident tracking for  $V_{OUT(MAX)} = 1.5V$  and  $V_{OUT(SL)} = 3.3V$  application.

### Power Good

The PGOOD pins are open drain pins that can be used to monitor valid output voltage regulation. This pin monitors a  $\pm 8\%$  window around the regulation point. A resistor can be pulled up to a particular supply voltage for monitoring. To prevent unwanted PGOOD glitches during transients or dynamic  $V_{OUT}$  changes, the LTM4622A's PGOOD falling edge includes a blanking delay of approximately  $40\mu s$ .

### Stability compensation

The LTM4622A module internal compensation loop is designed and optimized for low ESR ceramic output capacitors only application. Table 7 is provided for most application requirements. The LTpowerCAD Design Tool is available to download for control loop optimization.

### RUN Enable

Pulling the RUN pin to ground forces the LTM4622A into its shutdown state, turning off both power MOSFETs and most of its internal control circuitry. Tying the RUN pin voltage above  $1.27V$  will turn on the entire chip.

### Pre-Biased Output Start-Up

There may be situations that require the power supply to start up with a pre-bias on the output capacitors. In this case, it is desirable to start up without discharging that output pre-bias. The LTM4622A can safely power up into a pre-biased output without discharging it.

The LTM4622A accomplishes this by forcing discontinuous mode (DCM) operation until the TRACK/SS pin voltage reaches  $0.6V$  reference voltage. This will prevent the

BG from turning on during the pre-biased output start-up which would discharge the output.

### Overtemperature Protection

The internal overtemperature protection monitors the junction temperature of the module. If the junction temperature reaches approximately  $160^{\circ}C$ , both power switches will be turned off until the temperature drops about  $15^{\circ}C$  cooler.

### Input Overvoltage Protection

In order to protect the internal power MOSFET devices against transient voltage spikes, the LTM4622A constantly monitors each  $V_{IN}$  pin for an overvoltage condition. When  $V_{IN}$  rises above  $22.5V$ , the regulator suspends operation by shutting off both power MOSFETs on the corresponding channel. Once  $V_{IN}$  drops below  $21.5V$ , the regulator immediately resumes normal operation. The regulator executes its soft-start function when exiting an overvoltage condition.

### Thermal Considerations and Output Current Derating

The thermal resistances reported in the Pin Configuration section of the data sheet are consistent with those parameters defined by JESD51-9 and are intended for use with finite element analysis (FEA) software modeling tools that leverage the outcome of thermal modeling, simulation, and correlation to hardware evaluation performed on a  $\mu$ Module package mounted to a hardware test board—also defined by JESD51-9 (Test Boards for Area Array Surface Mount Package Thermal Measurements). The motivation for providing these thermal coefficients is found in JESD51-12 (Guidelines for Reporting and Using Electronic Package Thermal Information).

Many designers may opt to use laboratory equipment and a test vehicle such as the demo board to anticipate the  $\mu$ Module regulator's thermal performance in their application at various electrical and environmental operating conditions to compliment any FEA activities. Without





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operating conditions of a  $\mu$ Module. For example, in normal board-mounted applications, never does 100% of the device's total power loss (heat) thermally conduct exclusively through the top or exclusively through bottom of the  $\mu$ Module—as the standard defines for  $\theta_{JCtop}$  and  $\theta_{JCbottom}$ , respectively. In practice, power loss is thermally dissipated in both directions away from the package—granted, in the absence of a heat sink and airflow, a majority of the heat flow is into the board.

Within a SIP (system-in-package) module, be aware there are multiple power devices and components dissipating power, with a consequence that the thermal resistances relative to different junctions of components or die are not exactly linear with respect to total package power loss. To reconcile this complication without sacrificing modeling simplicity—but also, not ignoring practical realities—an approach has been taken using FEA software modeling along with laboratory testing in a controlled-environment chamber to reasonably define and correlate the thermal resistance values supplied in this data sheet: (1) Initially, FEA software is used to accurately build the mechanical geometry of the  $\mu$ Module and the specified PCB with all of the correct material coefficients along with accurate power loss source definitions; (2) this model simulates a software-defined JEDEC environment consistent with JESD51-12 to predict power loss heat flow and temperature readings at different interfaces that enable the calculation of the JEDEC-defined thermal resistance values; (3) the model and FEA software is used to evaluate the  $\mu$ Module with heat sink and airflow; (4) having solved for and analyzed these thermal resistance values and simulated various operating conditions in the software model, a thorough laboratory evaluation replicates the simulated conditions with thermocouples within a controlled-environment chamber while operating the device at the same power loss as that which was simulated. An outcome of this process and due-diligence yields a set of derating curves provided in other sections of this data sheet. After these laboratory test have been performed and correlated to the  $\mu$ Module model, then the  $\theta_{JB}$  and  $\theta_{BA}$  are summed together to correlate quite well with the  $\mu$ Module model with no airflow or heat sinking in a properly define chamber. This  $\theta_{JB} + \theta_{BA}$  value is shown in the Pin Configuration section and should accurately equal the  $\theta_{JA}$  value because

approximately 100% of power loss flows from the junction through the board into ambient with no airflow or top mounted heat sink.

The 1.5V, 3.3V, 5V, 8V and 12V power loss curves in Figure 8 to Figure 12 can be used in coordination with the load current derating curves in Figure 13 to Figure 23 for calculating an approximate  $\theta_{JA}$  thermal resistance for the LTM4622A (in two-phase single output operation) with no heat sinking and various airflow conditions. The power loss curves are taken at room temperature, and are increased with multiplicative factors of 1.35 assuming junction temperature at 120°C. The derating curves are plotted with the output current starting at 4A and the ambient temperature at 30°C. These output voltages are chosen to include the lower and higher output voltage ranges for correlating the thermal resistance. Thermal models are derived from several temperature measurements in a controlled temperature chamber along with thermal modeling analysis. The junction temperatures are monitored while ambient temperature is increased with and without airflow. The power loss increase with ambient temperature change is factored into the derating curves. The junctions are maintained at 120°C maximum while lowering output current or power with increasing ambient temperature. The decreased output current will decrease the internal module loss as ambient temperature is increased. The monitored junction temperature of 120°C minus the ambient operating temperature specifies how much module temperature rise can be allowed. As an example in Figure 16, the load current is derated to ~3A at ~100°C with 200LFM air but not heat sink and the power loss for the 5V to 3.3V at 3A output is about 1.15W. The 1.15W loss is calculated with the ~0.85W room temperature loss from the 5V to 3.3V power loss curve at 3A, and the 1.35 multiplying factor. If the 100°C ambient temperature is subtracted from the 120°C junction temperature, then the difference of 20°C divided by 1.15W equals a 17.5°C/W  $\theta_{JA}$  thermal resistance. Table 3 specifies a 17°C/W – 18°C/W value which is very close. Table 2 to Table 6 provide equivalent thermal resistances for 1.5V, 3.3V, 5V, 8V and 12V outputs with and without airflow. The derived thermal resistances in Table 2 to Table 6 for the various conditions can be multiplied by the calculated power loss as a function of ambient



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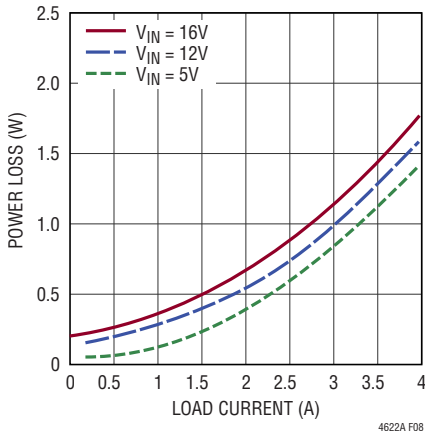


Figure 8. 1.5V Output Power Loss

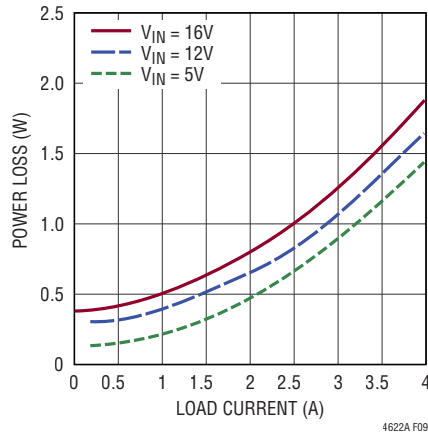


Figure 9. 3.3V Output Power Loss

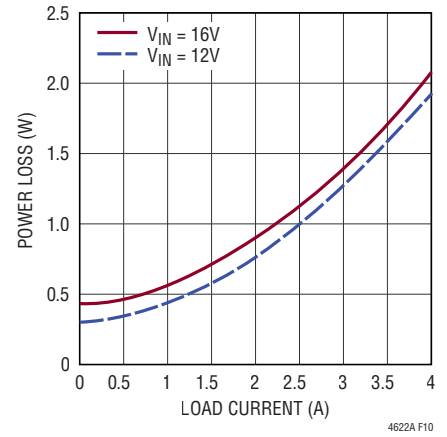


Figure 10. 5V Output Power Loss

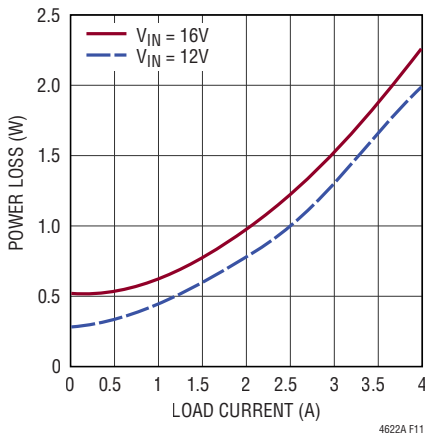


Figure 11. 8V Output Power Loss

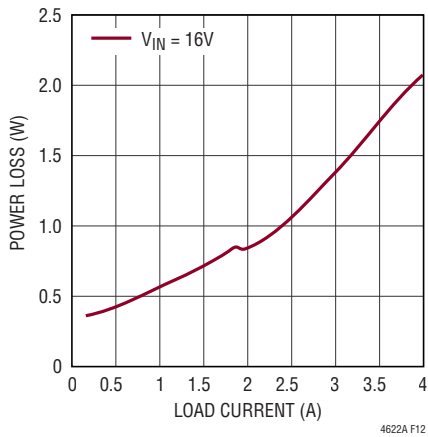


Figure 12. 12V Output Power Loss

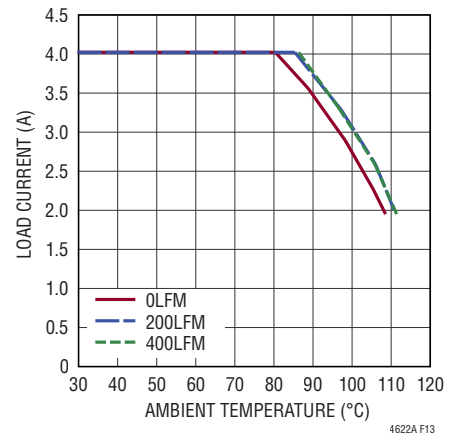


Figure 13. 5V Input to 1.5V Output Derating Curve, No Heat Sink

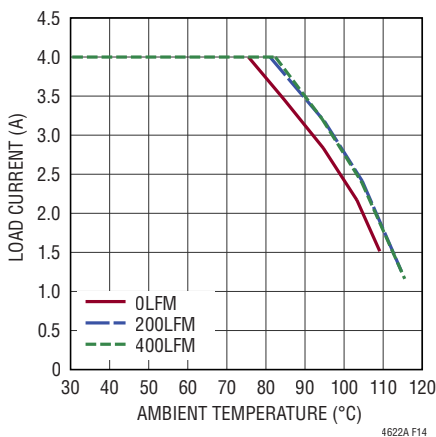


Figure 14. 12V Input to 1.5V Output Derating Curve, No Heat Sink

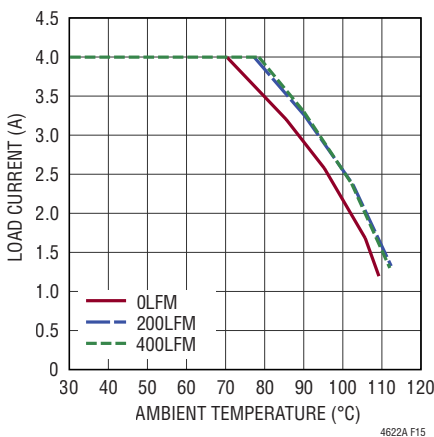


Figure 15. 16V Input to 1.5V Output Derating Curve, No Heat Sink

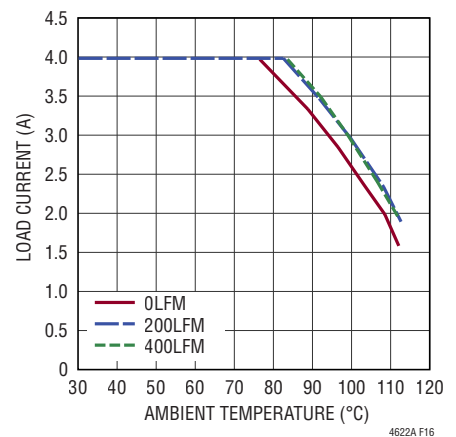
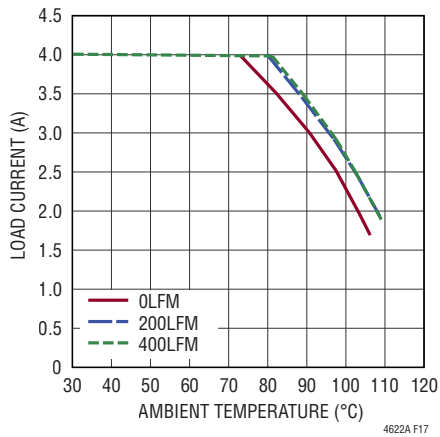
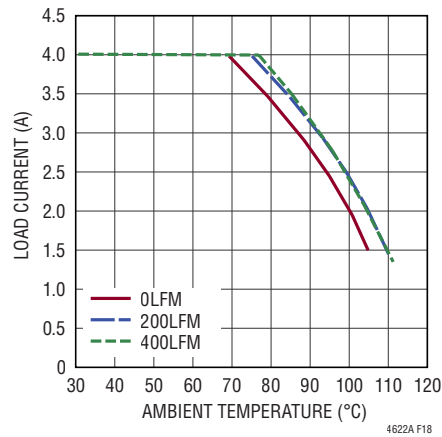


Figure 16. 5V Input to 3.3V Output Derating Curve, No Heat Sink

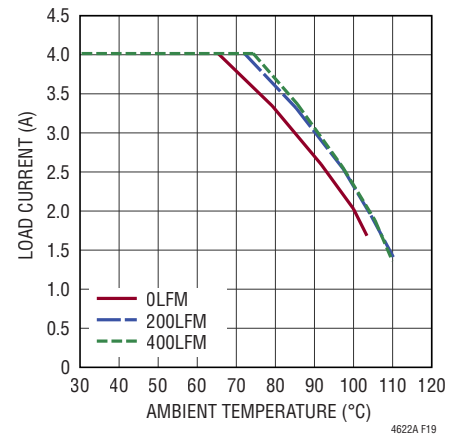
## APPLICATIONS INFORMATION



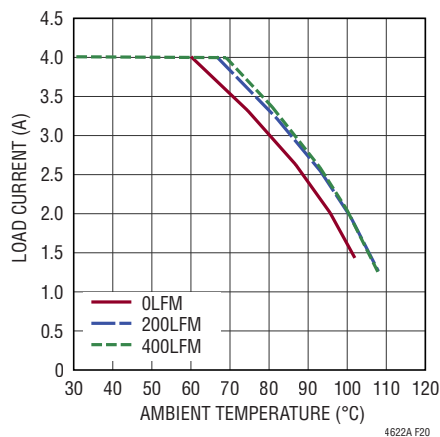
**Figure 17. 12V Input to 3.3V Output Derating Curve, No Heat Sink**



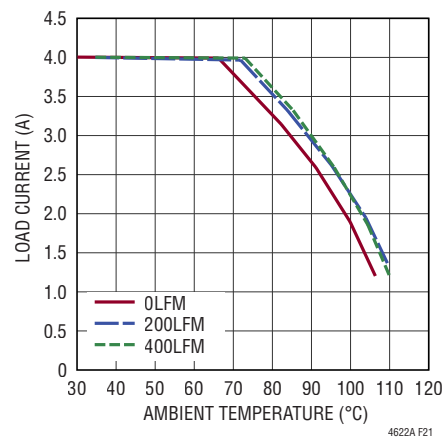
**Figure 18. 16V Input to 3.3V Output Derating Curve, No Heat Sink**



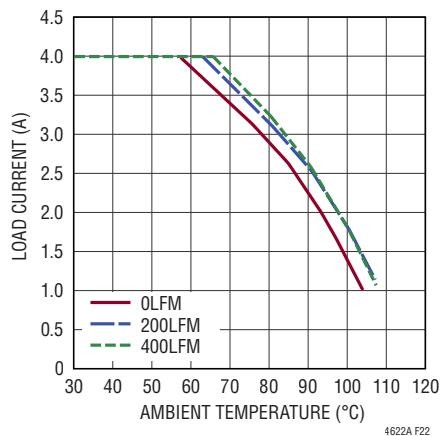
**Figure 19. 12V Input to 5V Output Derating Curve, No Heat Sink**



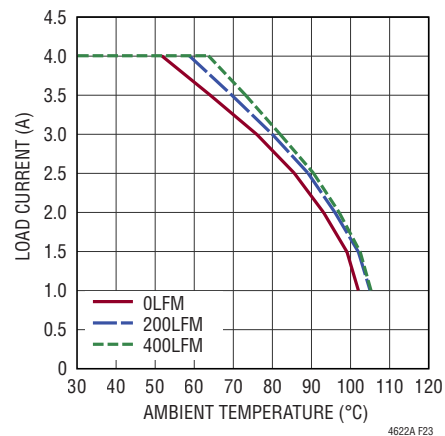
**Figure 20. 16V Input to 5V Output Derating Curve, No Heat Sink**



**Figure 21. 12V Input to 8V Output Derating Curve, No Heat Sink**



**Figure 22. 16V Input to 8V Derating Curve, No Heat Sink**



**Figure 23. 16V Input to 12V Output Derating Curve, No Heat Sink**

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**Table 2. 1.5V Output**

| DERATING CURVE                  | V <sub>IN</sub> (V) | POWER LOSS CURVE | AIRFLOW (LFM) | HEAT SINK | θ <sub>JA</sub> (°C/W) |
|---------------------------------|---------------------|------------------|---------------|-----------|------------------------|
| Figure 13, Figure 14, Figure 15 | 5, 12, 16           | Figure 8         | 0             | None      | 19 to 20               |
| Figure 13, Figure 14, Figure 15 | 5, 12, 16           | Figure 8         | 200           | None      | 17 to 18               |
| Figure 13, Figure 14, Figure 15 | 5, 12, 16           | Figure 8         | 400           | None      | 17 to 18               |

**Table 3. 3.3V Output**

| DERATING CURVE                  | V <sub>IN</sub> (V) | POWER LOSS CURVE | AIRFLOW (LFM) | HEAT SINK | θ <sub>JA</sub> (°C/W) |
|---------------------------------|---------------------|------------------|---------------|-----------|------------------------|
| Figure 16, Figure 17, Figure 18 | 5, 12, 16           | Figure 9         | 0             | None      | 19 to 20               |
| Figure 16, Figure 17, Figure 18 | 5, 12, 16           | Figure 9         | 200           | None      | 17 to 18               |
| Figure 16, Figure 17, Figure 18 | 5, 12, 16           | Figure 9         | 400           | None      | 17 to 18               |

**Table 4. 5V Output**

| DERATING CURVE       | V <sub>IN</sub> (V) | POWER LOSS CURVE | AIRFLOW (LFM) | HEAT SINK | θ <sub>JA</sub> (°C/W) |
|----------------------|---------------------|------------------|---------------|-----------|------------------------|
| Figure 19, Figure 20 | 12, 16              | Figure 10        | 0             | None      | 19 to 20               |
| Figure 19, Figure 20 | 12, 16              | Figure 10        | 200           | None      | 17 to 18               |
| Figure 19, Figure 20 | 12, 16              | Figure 10        | 400           | None      | 17 to 18               |

**Table 5. 8V Output**

| DERATING CURVE       | V <sub>IN</sub> (V) | POWER LOSS CURVE | AIRFLOW (LFM) | HEAT SINK | θ <sub>JA</sub> (°C/W) |
|----------------------|---------------------|------------------|---------------|-----------|------------------------|
| Figure 21, Figure 22 | 12, 16              | Figure 11        | 0             | None      | 19 to 20               |
| Figure 21, Figure 22 | 12, 16              | Figure 11        | 200           | None      | 17 to 18               |
| Figure 21, Figure 22 | 12, 16              | Figure 11        | 400           | None      | 17 to 18               |

**Table 6. 12V Output**

| DERATING CURVE | V <sub>IN</sub> (V) | POWER LOSS CURVE | AIRFLOW (LFM) | HEAT SINK | θ <sub>JA</sub> (°C/W) |
|----------------|---------------------|------------------|---------------|-----------|------------------------|
| Figure 23      | 16                  | Figure 12        | 0             | None      | 19 to 20               |
| Figure 23      | 16                  | Figure 12        | 200           | None      | 17 to 18               |
| Figure 23      | 16                  | Figure 12        | 400           | None      | 17 to 18               |

## APPLICATIONS INFORMATION

**Table 7. Output Voltage Response for Each Regulator Channel vs Component Matrix (See Figure 24)**  
**1.0A Load Step Typical Measured Values**

| C <sub>IN</sub><br>(CERAMIC) | PART NUMBER        | VALUE                 | C <sub>OUT1</sub><br>(CERAMIC) | PART NUMBER        | VALUE                 | C <sub>OUT2</sub><br>(BULK) | PART NUMBER | VALUE                         |
|------------------------------|--------------------|-----------------------|--------------------------------|--------------------|-----------------------|-----------------------------|-------------|-------------------------------|
| Murata                       | GRM188R61E475KE11# | 4.7μF, 25V, 0603, X5R | Murata                         | GRM21R60J476ME15#  | 47μF, 6.3V, 0805, X5R | Panasonic                   | 6TPC150M    | 150μF, 6.3V 3.5 × 2.8 × 1.4mm |
| Murata                       | GRM188R61E106MA73# | 10μF, 25V, 0603, X5R  | Murata                         | GRM188R60J226MEA0# | 22μF, 6.3V, 0603, X5R |                             |             |                               |
| Taiyo Yuden                  | TMK212BJ475KG-T    | 4.7μF, 25V, 0805, X5R | Taiyo Yuden                    | JMK212BJ476MG-T    | 47μF, 6.3V, 0805, X5R |                             |             |                               |

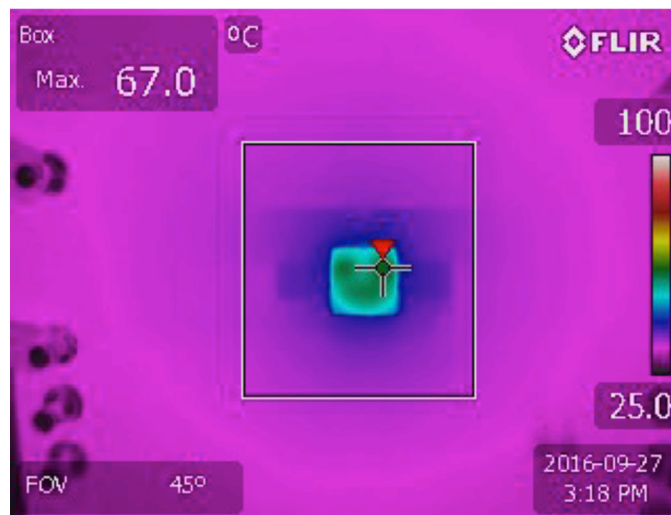
| V <sub>OUT</sub><br>(V) | C <sub>IN</sub><br>(CERAMIC)<br>(μF) | C <sub>IN</sub><br>(BULK) | C <sub>OUT1</sub><br>(CERAMIC)<br>(μF) | C <sub>OUT2</sub><br>(BULK)<br>(μF) | C <sub>FF</sub><br>(pF) | V <sub>IN</sub> (V) | DROOP<br>(mV) | P-P<br>DERIVATION<br>(mV) | RECOVERY<br>TIME (μs) | LOAD<br>STEP (A) | LOAD STEP<br>SLEW RATE<br>(A/μs) | R <sub>FB</sub><br>(kΩ) |
|-------------------------|--------------------------------------|---------------------------|--|-------------------------------------|-------------------------|---------------------|---------------|---------------------------|-----------------------|------------------|----------------------------------|-------------------------|
| 1.5                     | 10                                   | 0                         | 1 × 47                                 | 0                                   | 10                      | 5, 12               | 0             | 89                        | 10                    | 1.0              | 10                               | 40.2                    |
| 1.5                     | 10                                   | 0                         | 1 × 4.7                                | 150                                 | 0                       | 5, 12               | 0             | 75                        | 20                    | 1.0              | 10                               | 40.2                    |
| 2.5                     | 10                                   | 0                         | 1 × 47                                 | 0                                   | 10                      | 5, 12               | 0             | 112                       | 10                    | 1.0              | 10                               | 19.1                    |
| 2.5                     | 10                                   | 0                         | 1 × 4.7                                | 150                                 | 0                       | 5, 12               | 0             | 92                        | 25                    | 1.0              | 10                               | 19.1                    |
| 3.3                     | 10                                   | 0                         | 1 × 47                                 | 0                                   | 10                      | 5, 12               | 0             | 144                       | 15                    | 1.0              | 10                               | 13.3                    |
| 3.3                     | 10                                   | 0                         | 1 × 4.7                                | 150                                 | 0                       | 5, 12               | 0             | 104                       | 30                    | 1.0              | 10                               | 13.3                    |
| 5                       | 10                                   | 0                         | 2 × 47                                 | 0                                   | 10                      | 12                  | 0             | 157                       | 25                    | 1.0              | 10                               | 8.25                    |
| 5                       | 10                                   | 0                         | 1 × 4.7                                | 150                                 | 0                       | 12                  | 0             | 137                       | 50                    | 1.0              | 10                               | 8.25                    |
| 8                       | 10                                   | 0                         | 2 × 47                                 | 0                                   | 10                      | 12                  | 0             | 234                       | 50                    | 1.0              | 10                               | 4.87                    |
| 8                       | 10                                   | 0                         | 2 × 4.7                                | 150                                 | 0                       | 12                  | 0             | 149                       | 70                    | 1.0              | 10                               | 4.87                    |
| 12                      | 10                                   | 0                         | 3 × 47                                 | 0                                   | 10                      | 16                  | 0             | 301                       | 50                    | 1.0              | 10                               | 3.16                    |
| 12                      | 10                                   | 0                         | 3 × 4.7                                | 150                                 | 0                       | 16                  | 0             | 177                       | 80                    | 1.0              | 10                               | 3.16                    |

## APPLICATIONS INFORMATION

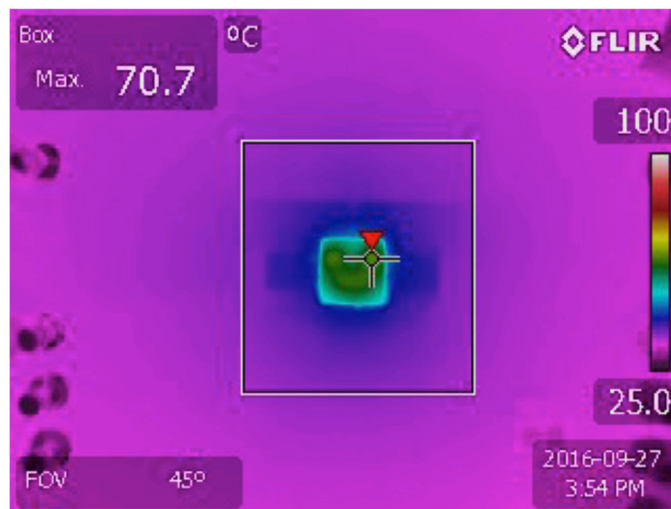
temperature to derive temperature rise above ambient, thus maximum junction temperature. Room temperature power loss can be derived from the efficiency curves in the Typical Performance Characteristics section and adjusted with the above ambient temperature multiplicative factors. The PCB is a 1.6mm thick four-layer board with two-ounce copper for the two outer layers and one

ounce-copper for the two inner layers. The PCB dimensions are 95mm × 76mm.

Figure 24 and Figure 25 show measured temperature picture of the LTM4622A with no heat sink from 12V input down to 3.3V and 5V output with 2A DC current on each and from 12V down to 5V and 8V output with 2A DC current on each. Both without heat sink and airflow.



**Figure 24. Thermal Image, 12V Input, 3.3V and 5V Output, 2A Each, No Airflow and No Heat Sink**



**Figure 25. Thermal Image, 12V Input, 5V and 8V Output, 2A Each, No Airflow and No Heat Sink**

## APPLICATIONS INFORMATION

### SAFETY CONSIDERATIONS

The LTM4622A modules do not provide galvanic isolation from  $V_{IN}$  to  $V_{OUT}$ . There is no internal fuse. If required, a slow blow fuse with a rating twice the maximum input current needs to be provided to protect each unit from catastrophic failure. The device does support thermal shutdown and over current protection.

### LAYOUT CHECKLIST/EXAMPLE

The high integration of LTM4622A makes the PCB board layout very simple and easy. However, to optimize its electrical and thermal performance, some layout considerations are still necessary.

- Use large PCB copper areas for high current paths, including  $V_{IN1}$ ,  $V_{IN2}$ , GND,  $V_{OUT1}$ , and  $V_{OUT2}$ . It helps to minimize the PCB conduction loss and thermal stress.
- Place high frequency ceramic input and output capacitors next to the  $V_{IN}$ , PGND, and  $V_{OUT}$  pins to minimize high frequency noise.
- Place a dedicated power ground layer underneath the unit.
- The two dedicated input decoupling capacitors, one for each  $V_{IN}$ , closely placed on each side of the module.
- To minimize the via conduction loss and reduce module thermal stress, use multiple vias for interconnection between top layer and other power layers.
- Do not put the via directly on the pad, unless they are capped or plated over.
- Use a separated SGND ground copper area for components connected to signal pins. Connect the SGND to GND underneath the unit.
- For parallel modules, tie the  $V_{OUT}$ ,  $V_{FB}$ , and COMP pins together. Use an internal layer to closely connect these pins together. The TRACK pin can be tied a common capacitor for regulator soft-start.
- Bring out test points on the signal pins for monitoring.

Figure 26 gives a good example of the recommended layout.

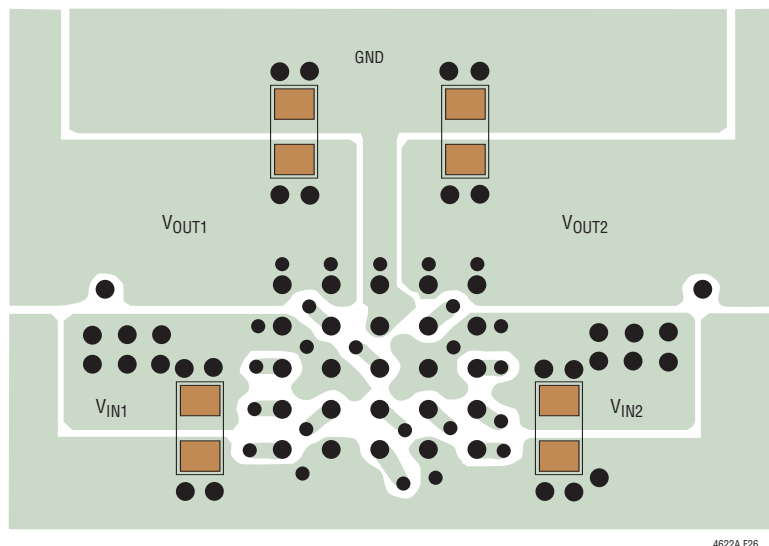


Figure 26. Recommended PCB Layout

## TYPICAL APPLICATIONS

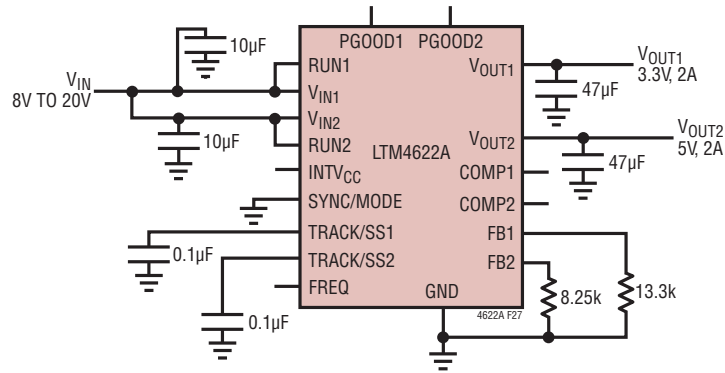


Figure 27. 8V<sub>IN</sub> to 20V<sub>IN</sub>, 3.3V and 5V Output at 2A Design

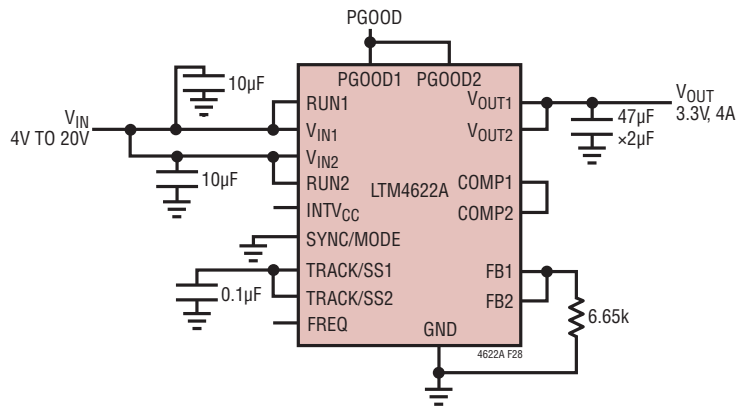


Figure 28. 4V<sub>IN</sub> to 20V<sub>IN</sub>, 3.3V Two Phase in Parallel 4A Design

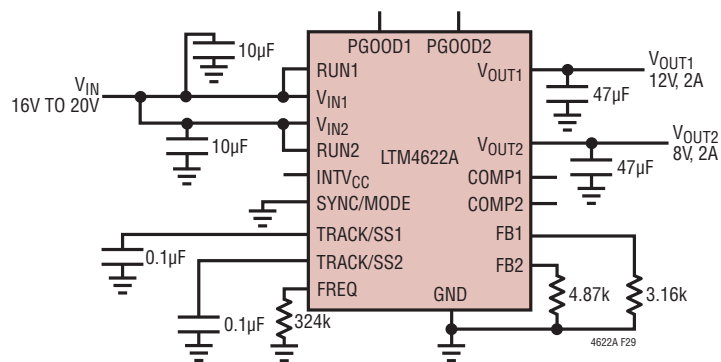


Figure 29. 16V<sub>IN</sub> to 20V<sub>IN</sub>, 12V and 8V Output at 2A with 2MHz Switching Frequency



TYPICAL APPLICATIONS

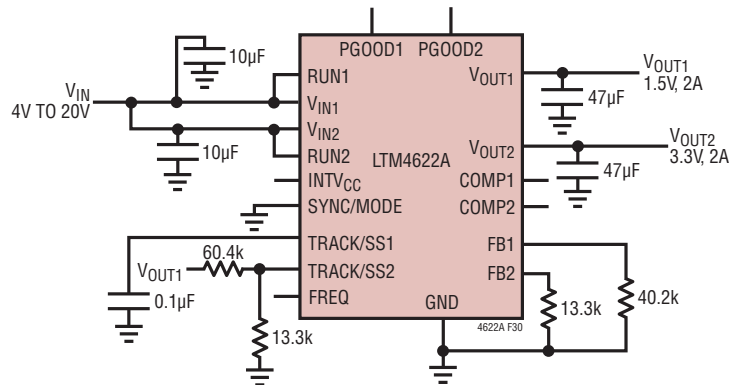


Figure 30. 4VIN to 20VIN, 1.5V and 3.3V Output at 2A Design with Output Coincident Tracking

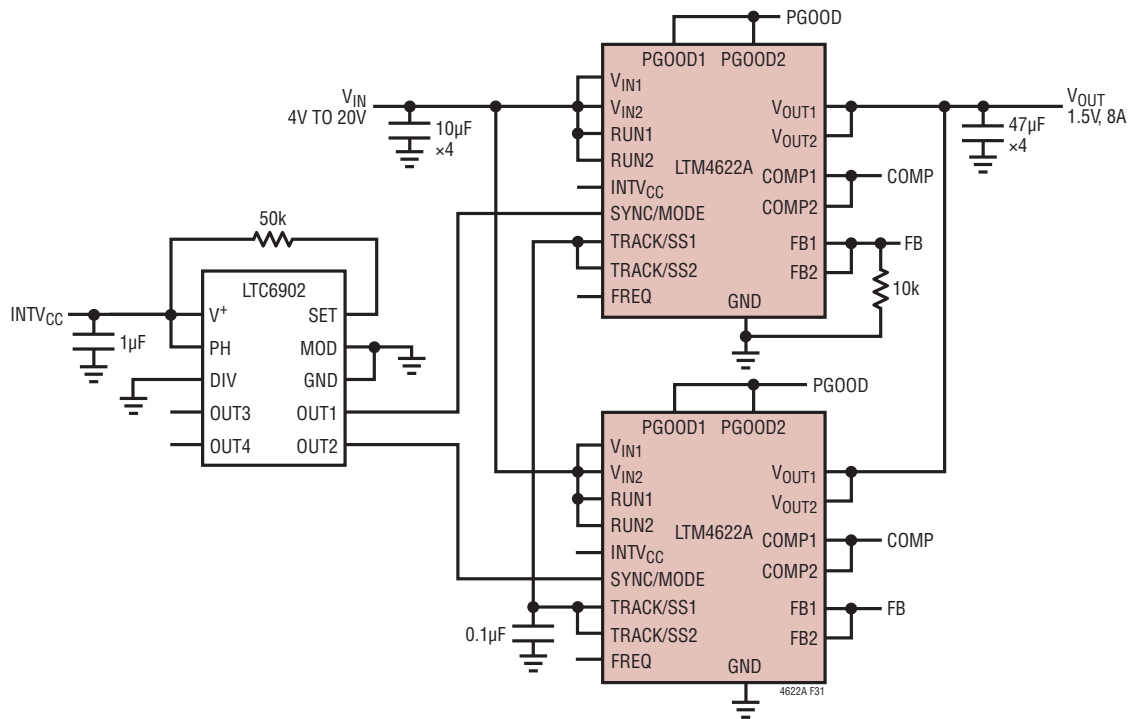


Figure 31. 4 Phase, 1.5V Output at 8A Design with LTC6902

## PACKAGE DESCRIPTION



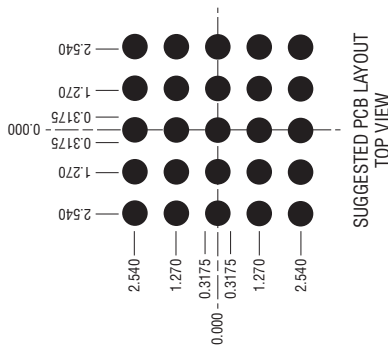
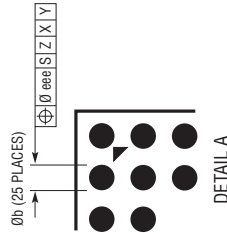
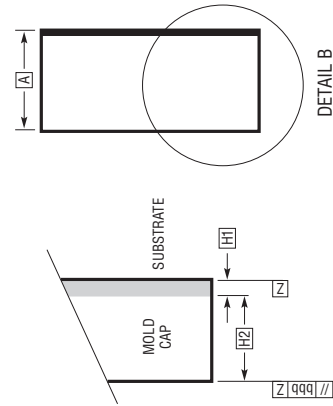
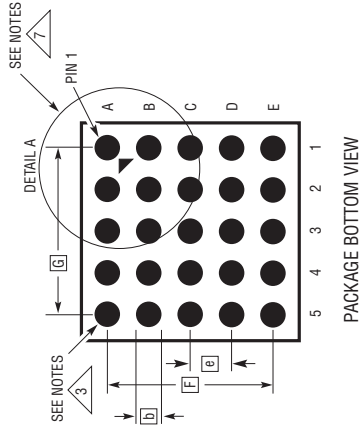
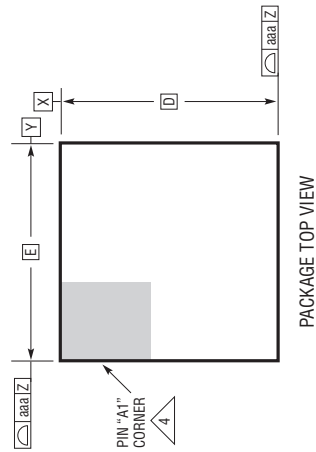
PACKAGE ROW AND COLUMN LABELING MAY VARY  
AMONG  $\mu$ Module PRODUCTS. REVIEW EACH PACKAGE  
LAYOUT CAREFULLY.

LTM4622A Component LGA and BGA Pinout

| PIN ID | FUNCTION   | PIN ID | FUNCTION  | PIN ID | FUNCTION           | PIN ID | FUNCTION | PIN ID | FUNCTION  |
|--------|------------|--------|-----------|--------|--------------------|--------|----------|--------|-----------|
| A1     | $V_{OUT2}$ | A2     | $V_{IN2}$ | A3     | TRACK/SS2          | A4     | FB2      | A5     | COMP2     |
| B1     | $V_{OUT2}$ | B2     | RUN2      | B3     | $V_{IN2}$          | B4     | PGOOD2   | B5     | GND       |
| C1     | GND        | C2     | GND       | C3     | INTV <sub>CC</sub> | C4     | FREQ     | C5     | SYNC/MODE |
| D1     | $V_{OUT1}$ | D2     | RUN1      | D3     | $V_{IN1}$          | D4     | PGOOD1   | D5     | GND       |
| E1     | $V_{OUT1}$ | E2     | $V_{IN1}$ | E3     | TRACK/SS1          | E4     | FB1      | E5     | COMP1     |

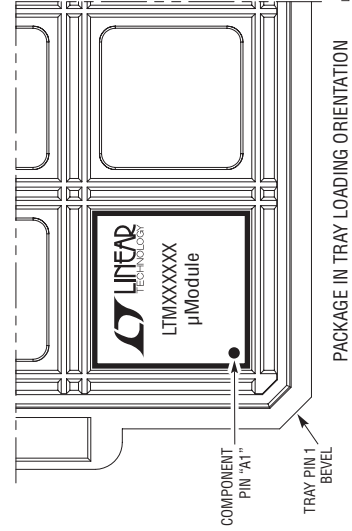
# PACKAGE DESCRIPTION

**LGA Package**  
**25-Lead (6.25mm × 6.25mm × 1.82mm)**  
 (Reference LTC DWG # 05-08-1949 Rev 0)



- NOTES:**
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
  2. ALL DIMENSIONS ARE IN MILLIMETERS
  - 3 LAND DESIGNATION PER JEDEC MO-222, SPP-010
  - 4 DETAILS OF PAD #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE PAD #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE
  5. PRIMARY DATUM -Z- IS SEATING PLANE
  6. THE TOTAL NUMBER OF PADS: 25

**!** PACKAGE ROW AND COLUMN LABELING MAY VARY AMONG  $\mu$ Module PRODUCTS. REVIEW EACH PACKAGE LAYOUT CAREFULLY

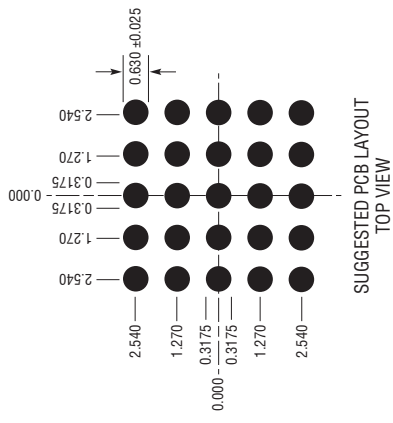
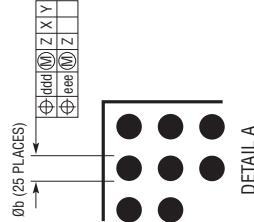
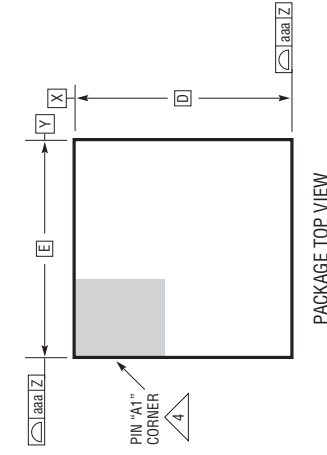
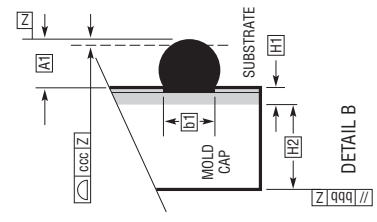
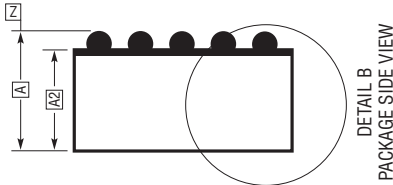
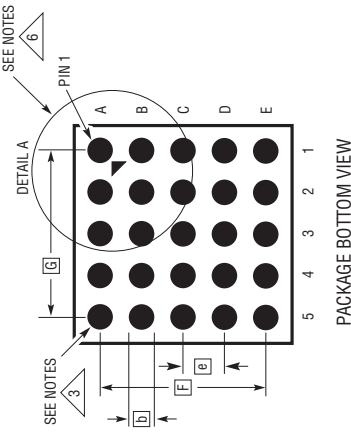


| DIMENSIONS                   |      |      |      |       |
|------------------------------|------|------|------|-------|
| SYMBOL                       | MIN  | NOM  | MAX  | NOTES |
| A                            | 1.72 | 1.82 | 1.92 |       |
| b                            | 0.60 | 0.63 | 0.66 |       |
| D                            |      | 6.25 |      |       |
| E                            |      | 6.25 |      |       |
| e                            |      | 1.27 |      |       |
| F                            |      | 5.08 |      |       |
| G                            |      | 5.08 |      |       |
| H1                           | 0.27 | 0.32 | 0.37 |       |
| H2                           | 1.45 | 1.50 | 1.55 |       |
| aaa                          |      |      | 0.15 |       |
| bbb                          |      |      | 0.10 |       |
| eee                          |      |      | 0.15 |       |
| TOTAL NUMBER OF LGA PADS: 25 |      |      |      |       |

LGA-25 (613 REV. 0)

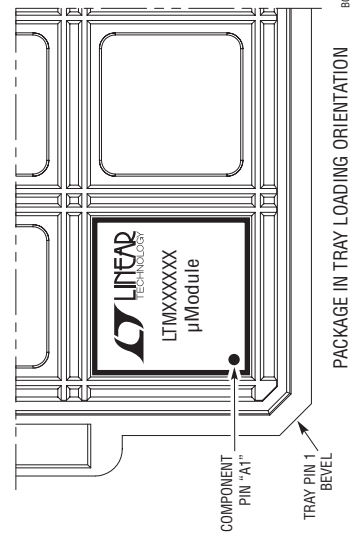
# PACKAGE DESCRIPTION

## BGA Package 25-Lead (6.25mm × 6.25mm × 2.42mm) (Reference LTC DWG # 05-08-1502 Rev A)



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
  2. ALL DIMENSIONS ARE IN MILLIMETERS
  3. BALL DESIGNATION PER JEDEC MS-028 AND JEP95
  4. DETAILS OF PIN #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE PIN #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE
  5. PRIMARY DATUM - Z - IS SEATING PLANE
  6. PACKAGE ROW AND COLUMN LABELING MAY VARY AMONG  $\mu$ Module PRODUCTS. REVIEW EACH PACKAGE LAYOUT CAREFULLY

| DIMENSIONS                |      |      |      |                |
|---------------------------|------|------|------|----------------|
| SYMBOL                    | MIN  | NOM  | MAX  | NOTES          |
| A                         | 2.22 | 2.42 | 2.62 |                |
| A1                        | 0.50 | 0.60 | 0.70 | BALL HT        |
| A2                        | 1.72 | 1.82 | 1.92 |                |
| b                         | 0.60 | 0.75 | 0.90 | BALL DIMENSION |
| b1                        | 0.60 | 0.63 | 0.66 | PAD DIMENSION  |
| D                         | 6.25 |      |      |                |
| E                         | 6.25 |      |      |                |
| e                         | 1.27 |      |      |                |
| F                         | 5.08 |      |      |                |
| G                         | 5.08 |      |      |                |
| H1                        | 0.27 | 0.32 | 0.37 | SUBSTRATE THK  |
| H2                        | 1.45 | 1.50 | 1.55 | MOLD CAP HT    |
| aaa                       |      |      |      | 0.15           |
| bbb                       |      |      |      | 0.10           |
| ccc                       |      |      |      | 0.20           |
| ddd                       |      |      |      | 0.30           |
| eee                       |      |      |      | 0.15           |
| TOTAL NUMBER OF BALLS: 25 |      |      |      |                |



86A 25/05/17 REV A

## REVISION HISTORY

| REV | DATE  | DESCRIPTION  | PAGE NUMBER                         |
|-----|-------|--|-------------------------------------|
| A   | 11/17 | Corrected Pin Configuration. Swapped $V_{IN1}$ and $V_{IN2}$ .   | 2                                   |
| B   | 4/18  | Corrected $R_{FSET}$ to GND.   | 8, 10                               |
| C   | 05/22 | Changed pin connection and Synchronization Frequency of LTC6902.<br>Corrected Output Voltage Tracking formulas.<br>Updated $V_{IN}$ in Table 5, Table 6.<br>Added ink marking statement to package photos.   | 11, 24<br>12<br>18<br>28            |
| D   | 08/24 | Corrected Turn-On Time and Track Pin Soft-Start Pull-Up Current to 1.2 $\mu$ A in Electrical Characteristics table.<br>Updated Electrical Characteristics notes.<br>Corrected Track Pin Soft-Start Pull-Up Current to 1.2 $\mu$ A in Pin Functions section.<br>Corrected Track Pin Soft-Start Pull-Up Current to 1.2 $\mu$ A in Soft-Start and Output Voltage Tracking section.<br>Changed master to main and slave to subordinate.<br>Fixed major formatting issues (repagination, cross references). | 3<br>4<br>6,<br>11, 12<br>12<br>All |

# LTM4622A

## PACKAGE PHOTOS Part marking is either ink mark or laser mark



## DESIGN RESOURCES

| SUBJECT  | DESCRIPTION   |
|--|---|
| <a href="#">µModule Design and Manufacturing Resources</a> | <p>Design:</p> <ul style="list-style-type: none"> <li>• Selector Guides</li> <li>• Demo Boards and Gerber Files</li> <li>• Free Simulation Tools</li> </ul> <p>Manufacturing:</p> <ul style="list-style-type: none"> <li>• Quick Start Guide</li> <li>• PCB Design, Assembly and Manufacturing Guidelines</li> <li>• Package and Board Level Reliability</li> </ul>   |
| <a href="#">µModule Regulator Products Search</a>          | <ol style="list-style-type: none"> <li>Sort table of products by parameters and download the result as a spreadsheet.</li> <li>Search using the Quick Power Search parametric table.</li> </ol> <div style="border: 1px solid #ccc; padding: 10px; margin-top: 10px;"> <p><b>Quick Power Search</b></p> <p>INPUT   <math>V_{in}(\text{Min})</math> <input type="text"/> V <math>V_{in}(\text{Max})</math> <input type="text"/> V</p> <p>OUTPUT   <math>V_{out}</math> <input type="text"/> V <math>I_{out}</math> <input type="text"/> A</p> <p>FEATURES   <input type="checkbox"/> Low EMI <input type="checkbox"/> Ultrathin <input type="checkbox"/> Internal Heat Sink</p> <p style="text-align: center;"><a href="#">Multiple Outputs</a> <span style="float: right;"><a href="#">Search</a></span></p> </div> |
| <a href="#">Digital Power System Management</a>            | Analog Devices' family of digital power supply management ICs are highly integrated solutions that offer essential functions, including power supply monitoring, supervision, margining and sequencing, and feature EEPROM for storing user configurations and fault logging.   |

## RELATED PARTS

| PART NUMBER             | DESCRIPTION   | COMMENTS  |
|-------------------------|---|---|
| <a href="#">LTM4614</a> | Dual 5V, 4A µModule Regulator                                   | $2.375V \leq V_{IN} \leq 5.5V$ , $0.8V \leq V_{OUT} \leq 5V$ , 15mm × 15mm × 2.82mm LGA   |
| <a href="#">LTM4618</a> | 26V <sub>IN</sub> , 6A Step-Down µModule Regulator              | $4.5V \leq V_{IN} \leq 26.5V$ , $0.8V \leq V_{OUT} \leq 5V$ , PLL Input, V <sub>OUT</sub> Tracking, 9mm × 15mm × 4.32mm LGA                   |
| <a href="#">LTM4619</a> | Dual 26V, 4A Step-Down µModule Regulator                        | $4.5V \leq V_{IN} \leq 26.5V$ , $0.8V \leq V_{OUT} \leq 5V$ , PLL Input, V <sub>OUT</sub> Tracking, PGOOD, 15mm × 15mm × 2.82mm LGA           |
| <a href="#">LTM4622</a> | Lower V <sub>OUT</sub> than LTM4622A                            | $3.6V \leq V_{IN} \leq 20V$ , $0.6V \leq V_{OUT} \leq 5.5V$ , Pin Compatible with LTM4622A  |
| <a href="#">LTM4623</a> | 20V <sub>IN</sub> , 3A Step-Down µModule Regulator              | $4V \leq V_{IN} \leq 20V$ , $0.6V \leq V_{OUT} \leq 5.5V$ , PLL Input, CLKOUT, V <sub>OUT</sub> Tracking, PGOOD, 6.25mm × 6.25mm × 1.82mm LGA |
| <a href="#">LTM4624</a> | 14V <sub>IN</sub> , 4A Step-Down µModule Regulator              | $4V \leq V_{IN} \leq 14V$ , $0.6V \leq V_{OUT} \leq 5.5V$ , V <sub>OUT</sub> Tracking, PGOOD, 6.25mm × 6.25mm × 5.01mm BGA                    |
| <a href="#">LTM4625</a> | 20V <sub>IN</sub> , 5A Step-Down µModule Regulator              | $4V \leq V_{IN} \leq 20V$ , $0.6V \leq V_{OUT} \leq 5.5V$ , PLL Input, CLKOUT, V <sub>OUT</sub> Tracking, PGOOD, 6.25mm × 6.25mm × 5.01mm BGA |
| <a href="#">LTM4631</a> | Ultrathin, Dual 10A Step-Down µModule Regulator                 | $4.5V \leq V_{IN} \leq 15V$ , $0.6V \leq V_{OUT} \leq 1.8V$ , 16mm × 16mm × 1.91mm LGA  |
| <a href="#">LTM4642</a> | 20V <sub>IN</sub> , Dual 4A, Step-Down µModule Regulator        | $4.5V \leq V_{IN} \leq 20V$ , $0.6V \leq V_{OUT} \leq 5.5V$ , 9mm × 11.25mm × 4.92mm BGA  |
| <a href="#">LTM4643</a> | Ultrathin, Quad 3A, Step-Down µModule Regulator                 | $4V \leq V_{IN} \leq 20V$ , $0.6V \leq V_{OUT} \leq 3.3V$ , 9mm × 15mm × 1.82mm LGA   |
| <a href="#">LTM4644</a> | Quad 4A, Step-Down µModule Regulator                            | $4V \leq V_{IN} \leq 14V$ , $0.6V$ to $5.5V$ , 9mm × 15mm × 5.01mm BGA  |
| <a href="#">LTC6902</a> | Multiphase Oscillator with Spread Spectrum Frequency Modulation | 1-, 3-, or 4-Phase Outputs; to 20MHz Frequency  |