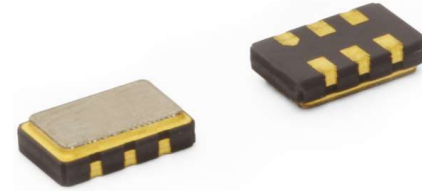


Model 655

Ultra Low Jitter LVPECL or LVDS Clock

Features

- Ceramic Surface Mount Package
- Ultra Low Phase Jitter Performance, 100fs Typical
- Fundamental or 3rd Overtone Crystal Design
- Frequency Range 80 – 170MHz *
- +2.5V or +3.3V Operation [+1.8V LVDS only]
- Output Enable Standard
- Tape and Reel Packaging, EIA-481



Part Dimensions:
5.0 × 3.2 × 1.2mm • 62.00mg

Standard Frequencies

* See Page 8 for common frequencies.
Check with factory for availability of frequencies not listed.

Applications

- SerDes
- Storage Area Networking
- Broadband Access
- SONET/SDH/DWDM
- PON
- Ethernet/Gbe/SyncE
- Fiber Channel
- Medical Electronics
- Test and Measurement

Description

CTS Model 655 is a low cost, high performance clock oscillator supporting differential LVPECL or LVDS outputs. Employing the latest IC technology, M655 has excellent stability and very low jitter/phase noise performance.

Ordering Information

| Model | Output Type | Frequency Code [MHz] | Frequency Stability | Temperature Range | Supply Voltage | Packaging |
|-------|------------------------------------------------------------------------------------------------------------------------------------|----------------------------------------------------------|------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------|--------------------------------------|
| 655 | P | XXX or XXXX | 3 | G | 3 | T |
| | | Code Frequency Product Frequency Code ¹ | | Code Temp. Range C -20°C to +70°C I -40°C to +85°C G -40°C to +105°C ³ | Code Voltage M +1.8Vdc ⁴ 2 +2.5Vdc 3 +3.3Vdc | Code Packing T 1k pcs./reel |
| | Code Output P LVPECL - Pin 1 Enable L LVDS - Pin 1 Enable E LVPECL - Pin 2 Enable V LVDS - Pin 2 Enable | | Code Stability Code Stability 6 ±20ppm ² 4 ±30ppm 5 ±25ppm 3 ±50ppm | | | |

Notes:

- 1] Refer to document 016-1454-0, Frequency Code Tables. 3-digits for frequencies <100MHz, 4-digits for frequencies 100MHz or greater.
- 2] Check factory for availability. Temperature code C only.
- 3] Check factory for availability. Stability code 3 only.
- 4] LVDS output only. Consult factory for availability.

**Not all performance combinations and frequencies may be available.
Contact your local CTS Representative or CTS Customer Service for availability.**

This product is specified for use only in standard commercial applications. Supplier disclaims all express and implied warranties and liability in connection with any use of this product in any non-commercial applications or in any application that may expose the product to conditions that are outside of the tolerances provided in its specification.



Electrical Specifications

Operating Conditions

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNIT |
|----------------------------|------------------|--------------|-------------------------|-------------------|-------------------------|------|
| Maximum Supply Voltage | V _{CC} | - | -0.5 | - | 5.0 | V |
| Supply Voltage [Note 1] | V _{CC} | ±5% | 1.710 2.375 3.135 | 1.8 2.5 3.3 | 1.890 2.625 3.465 | V |
| Supply Current | | | | | | |
| LVPECL | I _{CC} | Maximum Load | - | 55 | 88 | mA |
| LVDS | | | - | 45 | 66 | |
| Operating Temperature | T _A | - | -20 -40 -40 | +25 | +70 +85 +105 | °C |
| Storage Temperature | T _{STG} | - | -50 | - | +125 | °C |

Frequency Stability

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNIT |
|---------------------------------|--------------------|---------------------------------------------|-----|----------------|-----|------|
| Frequency Range | | | | | | |
| LVPECL | f _O | - | | 80 - 170 | | MHz |
| LVDS | | | | 80 - 170 | | |
| Frequency Stability [Note 2] | Δf/f _O | - | | 20, 25, 30, 50 | | ±ppm |
| Aging | Δf/f ₂₅ | First Year @ +25°C, nominal V _{CC} | -3 | - | 3 | ppm |

1.] LVDS output only for +1.8V option.

2.] Inclusive of initial tolerance at time of shipment, changes in supply voltage, load, temperature and 1st year aging.

Output Parameters

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNIT |
|-----------------------------|------------------------------------|---------------------------------------------|----------------------------------------------------|--------------|----------------------------------------------------|------|
| Output Type | - | - | | LVPECL | | - |
| Output Load | R _L | Terminated to V _{CC} - 2.0V | - | 50 | - | Ohms |
| Output Voltage Levels | V _{OH} V _{OL} | PECL Load, -20°C to +70°C | V _{CC} - 1.025 V _{CC} - 1.810 | - - | V _{CC} - 0.880 V _{CC} - 1.620 | V |
| | V _{OH} V _{OL} | PECL Load, -40°C to +85°C | V _{CC} - 1.085 V _{CC} - 1.830 | - - | V _{CC} - 0.880 V _{CC} - 1.555 | V |
| Output Duty Cycle | SYM | @ V _{CC} - 1.3V | 45 | - | 55 | % |
| Rise and Fall Time | T _R , T _F | @ 20%/80% Levels, R _L = 50 Ohms | - | 0.3 | 0.7 | ns |
| Output Type | - | - | | LVDS | | - |
| Output Load | R _L | Between Outputs | - | 100 | - | Ohms |
| Output Voltage Levels | V _{OH} V _{OL} | LVDS Load | - 0.90 | 1.43 1.10 | 1.60 - | V |
| Output Duty Cycle | SYM | @ 1.25V | 45 | - | 55 | % |
| Differential Output Voltage | V _{OD} | R _L = 100 Ohms | 247 | 330 | 454 | mV |
| Offset Voltage | V _{OS} | LVDS Load | 1.125 | 1.25 | 1.375 | V |
| Rise and Fall Time | T _R , T _F | @ 20%/80% Levels, R _L = 100 Ohms | - | 0.4 | 0.7 | ns |

Electrical Specifications

Output Parameters

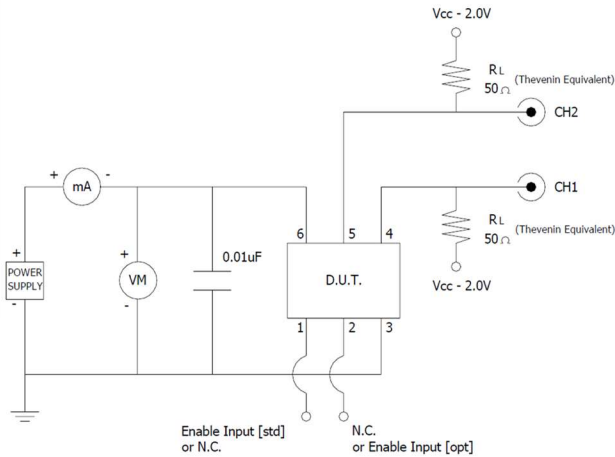
| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNIT |
|----------------------------------|--------------|------------------------------------------|-------------|-----|-------------|------|
| Start Up Time | T_S | Application of V_{CC} | - | 2 | 5 | ms |
| Enable Function [Standby] | | | | | | |
| Enable Input Voltage | V_{IH} | Pin 1 or 2 Logic '1', Output Enabled | $0.7V_{CC}$ | - | - | V |
| Disable Input Voltage | V_{IL} | Pin 1 or 2 Logic '0', Output Disabled | - | - | $0.3V_{CC}$ | V |
| Disable Time | T_{PLZ} | Pin 1 or 2 Logic '0', Output Disabled | - | - | 200 | ns |
| Enable Time | T_{PLZ} | Pin 1 or 2 Logic '1', Output Enabled | - | - | 2 | ms |
| Phase Jitter, RMS | | | | | | |
| | t_{jrms} | 80 - 124.9MHz, Bandwidth 12 kHz - 20 MHz | - | - | 200 | fs |
| | | 125 - 170MHz, Bandwidth 12 kHz - 20 MHz | - | - | 100 | |
| Period Jitter, RMS | p_{jrms} | - | - | 2.6 | - | ps |
| Period Jitter, pk-pk | p_{jpk-pk} | - | - | 25 | - | ps |

Enable Truth Table

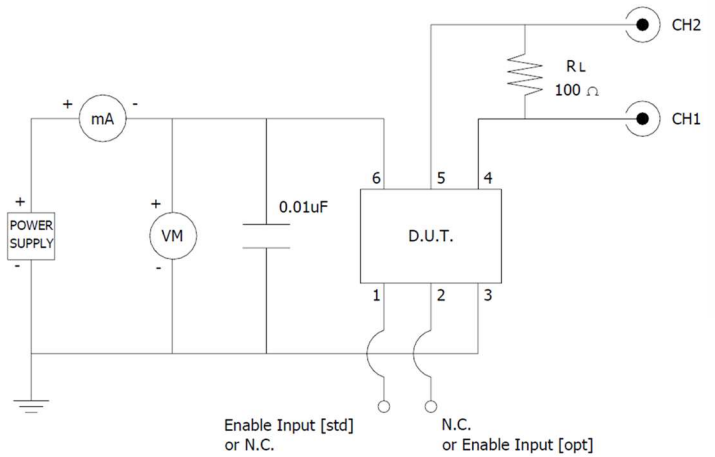
| Pin 1 or Pin 2 | Pin 4 & Pin 5 |
|----------------|------------------------------------|
| Logic '1' | Output Enabled |
| Open | Output Enabled |
| Logic '0' | Output Disabled, High Impedance |

Test Circuit

LVPECL

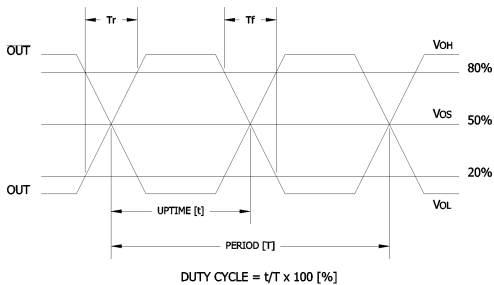


LVDS



Output Waveform

LVPECL or LVDS

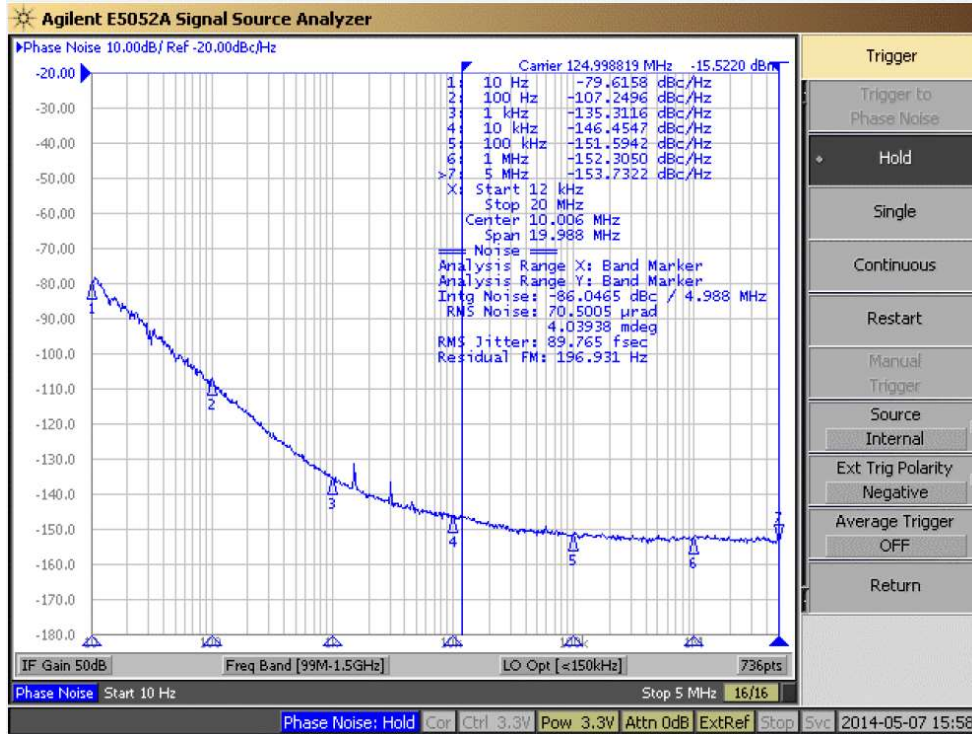


Electrical Specifications

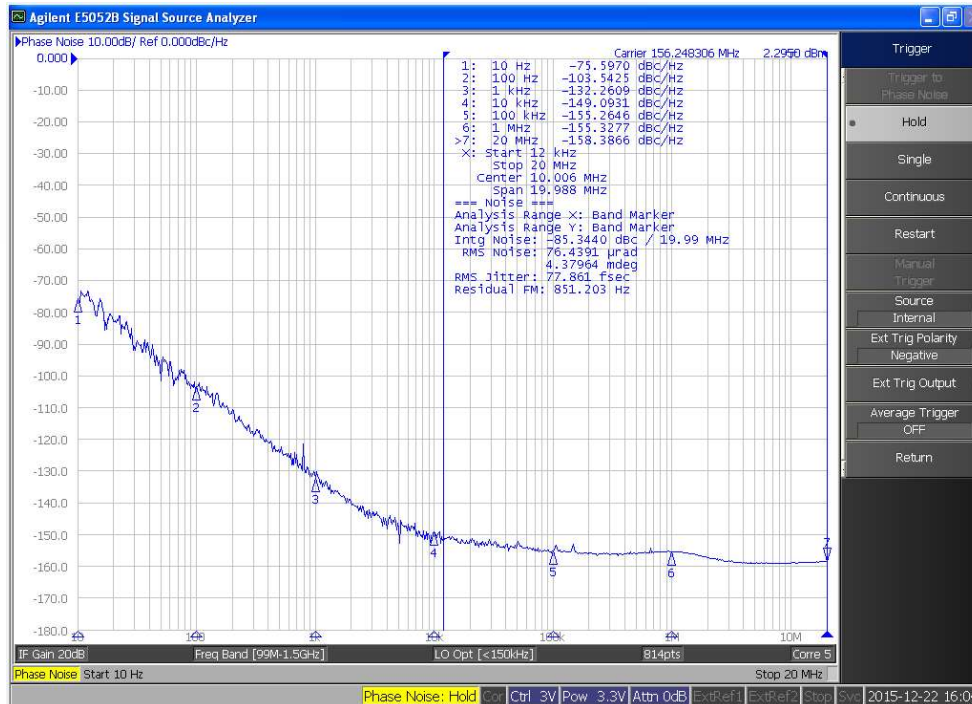
Performance Data

Phase Noise [typical]

125.00MHz, LVPECL, $V_{CC} = 3.3V$, $T_A = +25^\circ C$



156.25MHz, LVPECL, $V_{CC} = 3.3V$, $T_A = +25^\circ C$

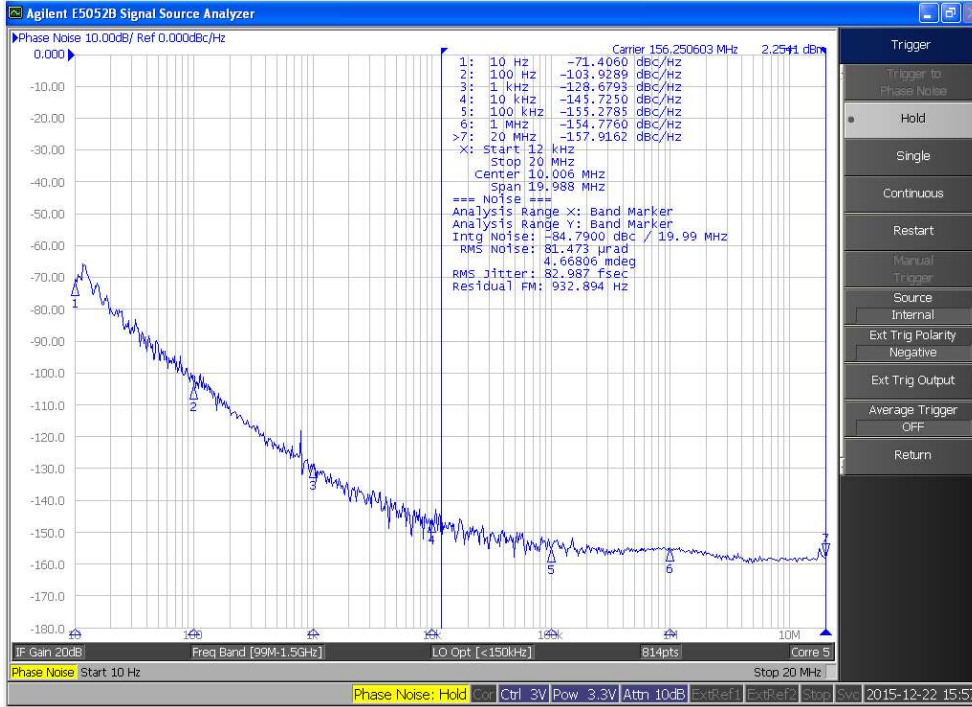


Electrical Specifications

Performance Data

Phase Noise [typical]

156.25MHz, LVDS, $V_{CC} = 3.3V$, $T_A = +25^\circ C$



Phase Noise Tabulated

Typical, $V_{CC} = 3.3V$, $T_A = +25^\circ C$

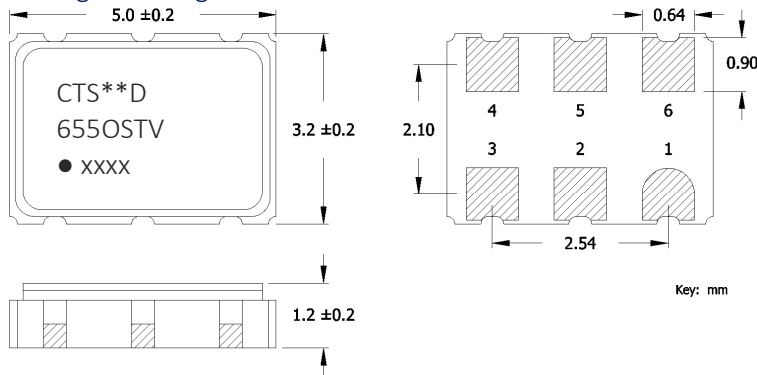
| PARAMETER | SYMBOL | CONDITIONS | TYP | UNIT |
|---------------------------|--------|-------------------------------------|---------|--------|
| LVPECL @ 125.00MHz | | | | |
| Phase Noise | | Single Side Band | | |
| | | @ 10Hz | -79.62 | |
| | | @ 100Hz | -107.25 | |
| | | @ 1kHz | -135.31 | dBc/Hz |
| | | @ 10kHz | -146.45 | |
| | | @ 100kHz | -151.59 | |
| | | @ 1MHz | -152.31 | |
| | | @ 5MHz | -153.73 | |
| Phase Jitter, RMS | tjrms | Integration Bandwidth 12kHz - 20MHz | 89.77 | fs |

| PARAMETER | SYMBOL | CONDITIONS | TYP | UNIT |
|---------------------------|--------|-------------------------------------|---------|--------|
| LVPECL @ 156.25MHz | | | | |
| Phase Noise | | Single Side Band | | |
| | | @ 10Hz | -75.60 | |
| | | @ 100Hz | -103.54 | |
| | | @ 1kHz | -132.26 | dBc/Hz |
| | | @ 10kHz | -149.09 | |
| | | @ 100kHz | -155.26 | |
| | | @ 1MHz | -155.33 | |
| | | @ 20MHz | -158.39 | |
| Phase Jitter, RMS | tjrms | Integration Bandwidth 12kHz - 20MHz | 77.86 | fs |

| PARAMETER | SYMBOL | CONDITIONS | TYP | UNIT |
|-------------------------|--------|-------------------------------------|---------|--------|
| LVDS @ 156.25MHz | | | | |
| Phase Noise | | Single Side Band | | |
| | | @ 10Hz | -71.41 | |
| | | @ 100Hz | -103.93 | |
| | | @ 1kHz | -128.68 | dBc/Hz |
| | | @ 10kHz | -145.73 | |
| | | @ 100kHz | -155.28 | |
| | | @ 1MHz | -154.78 | |
| | | @ 20MHz | -157.92 | |
| Phase Jitter, RMS | tjrms | Integration Bandwidth 12kHz - 20MHz | 82.99 | fs |

Mechanical Specifications

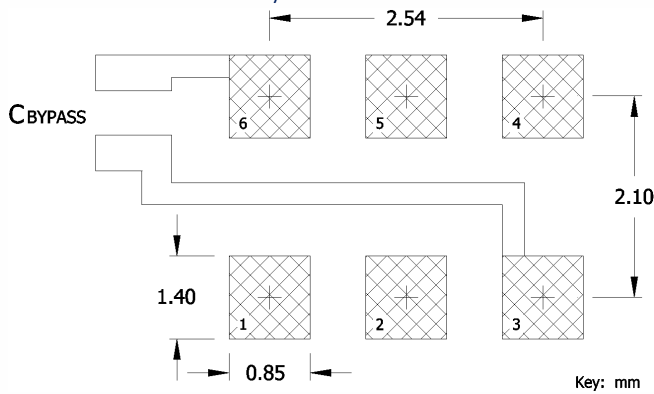
Package Drawing



Marking Information

1. ** - Manufacturing Site Code.
2. D – Date Code. See Table I for codes.
3. O – Output Type; P or E = LVPECL, L or V = LVDS.
[Refer to Ordering Information]
3. ST – Frequency Stability/Temperature Code.
4. V – Voltage Code; 3 = 3.3V, 2 = 2.5V.
5. xxxx – Frequency Code.
3-digits, frequencies below 100MHz
4-digits, frequencies 100MHz or greater
[See document 016-1454-0, Frequency Code Tables.]

Recommended Pad Layout



Notes

1. JEDEC termination code (e4). Barrier-plating is nickel [Ni] with gold [Au] flash plate.
2. Reflow conditions per JEDEC J-STD-020; +260°C maximum, 20 seconds.
3. MSL = 1.

Pin Assignments

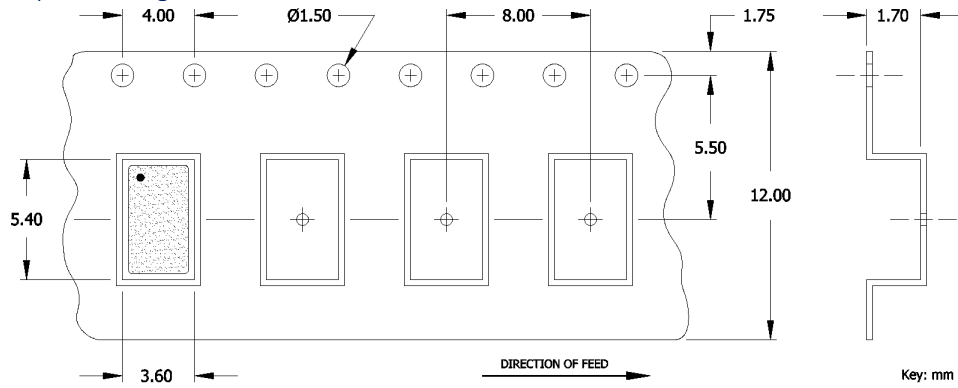
| Pin | Symbol | Function |
|-----|-----------------|----------------------------|
| 1 | EOH or N.C. | Enable [std] or No Connect |
| 2 | N.C. or EOH | No Connect or Enable [opt] |
| 3 | GND | Circuit & Package Ground |
| 4 | Output | RF Output |
| 5 | Output | Complimentary RF Output |
| 6 | V _{CC} | Supply Voltage |

Table I - Date Code, Beginning year 2021

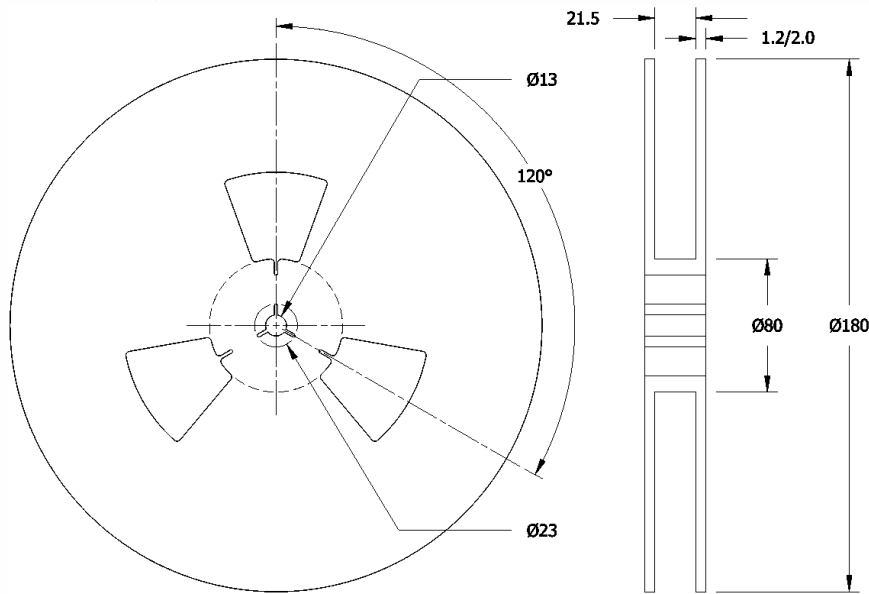
| | | MONTH | | | | | | | | | | | | | | |
|------|------|-------|------|------|-----|-----|-----|-----|-----|-----|-----|-----|-----|---|---|---|
| | | JAN | FEB | MAR | APR | MAY | JUN | JUL | AUG | SEP | OCT | NOV | DEC | | | |
| YEAR | | | | | | | | | | | | | | | | |
| 2021 | 2025 | 2029 | 2033 | 2037 | A | B | C | D | E | F | G | H | J | K | L | M |
| 2022 | 2026 | 2030 | 2034 | 2038 | N | P | Q | R | S | T | U | V | W | X | Y | Z |
| 2023 | 2027 | 2031 | 2035 | 2039 | a | b | c | d | e | f | g | h | j | k | l | m |
| 2024 | 2028 | 2032 | 2036 | 2040 | n | p | q | r | s | t | u | v | w | x | y | z |

Packaging - Tape and Reel

Tape Drawing



Reel Drawing



Notes

1. Device quantity is 1k pieces minimum 3k pieces maximum per 180mm reel.
2. Complete CTS part number, frequency value and date code information must appear on reel and carton labels.



Addendum

Common Frequencies Available – MHz

| FREQUENCY | FREQUENCY CODE | FREQUENCY | FREQUENCY CODE | FREQUENCY | FREQUENCY CODE | FREQUENCY | FREQUENCY CODE |
|------------|----------------|------------|----------------|-----------|----------------|-----------|----------------|
| 80.000000 | 800 | 156.250000 | 1562 | | | | |
| 100.000000 | 1000 | 156.253900 | 156E | | | | |
| 120.000000 | 1200 | 156.253906 | 156A | | | | |
| 125.000000 | 1250 | 161.132800 | 1611 | | | | |
| 133.000000 | 1330 | 167.372800 | 167A | | | | |
| 148.351600 | 148A | | | | | | |
| 148.500000 | 1485 | | | | | | |
| 150.000000 | 1500 | | | | | | |
| 153.600000 | 1536 | | | | | | |
| 155.520000 | 1555 | | | | | | |