TCXO
Specification
Models TL602 and TVL602

CONNOR WINFIELD

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Description:

The Connor-Winfield TL602 and TVL602 are surface mount 5x7mm, 3.3V, LVCMOS Temperature Compensated Crystal Oscillators (TCXO) designed for application compliance to Telcordia Stratum 3, ITU-T G.813 Option 2, and ITU-T G.8262 Option 2.

Features:

- 3.3 Vdc Operation
- Frequency Stability: ± 0.14 ppm
- Temperature Range: -40 to 85°C
- LVCMOS Output
- Ceramic Surface Mount Package
- Tape and Reel Packaging
- RoHS Compliant / Pb Free

Absolute Maximum Ratings

Parameter	Minimum	Nominal	Maximum	Units	Notes
Storage Temperature	-55	-	85	°C	
Supply Voltage (Vcc)	-0.5	-	4.6	Vdc	
Input Voltage	-0.5	-	Vcc+0.5		

Operating Specifications

Parameter	Minimum	Nominal	Maximum	Units	Notes
Nominal Frequency (Fo)	-	20.0 and 24.576M	-	MHz	
Frequency Calibration @ 25 °C	-1.0	-	1.0	ppm	1
Frequency Stability vs. Temperature	-140	-	140	ppb	2
Frequency vs. Load Stability	-50	-	50	ppb	±5%
Frequency vs. Voltage Stability	-50	-	50	ppb	±5%
Static Temperature Hysteresis	-	-	0.40	ppm	3
Short Term Allan Variance (1 second)	-	1.0E-10	-		
Constant Temperature Stability	-40	-	40	ppb	24 Hours
Aging 1st Year	-1.0	-	1.0	ppm	
Total Tolerance	-4.6	-	4.6	ppm	
Operating Temperature Range:	-40	-	85	°C	
Supply Voltage (Vcc)	3.135	3.3	3.465	Vdc	±5%
Supply Current (Icc)	-	-	6	mA	
Period Jitter	-	3	5	ps rms	
Integrated Phase Jitter	-	0.5	1.0	ps rms	4
SSB Phase Noise (Fo=20MHz)					
SSB Phase Noise at 10Hz offset	-	-100	-	dBc/Hz	
SSB Phase Noise at 100Hz offset	-	-130	-	dBc/Hz	
SSB Phase Noise at 1KHz offset	-	-150	-	dBc/Hz	
SSB Phase Noise at 10KHz offset	-	-158	-	dBc/Hz	
SSB Phase Noise at 100KHz offset	-	-160	-	dBc/Hz	
Start-up Time	-	-	1	ms	

Enable / Disable Input Characteristics (TL602 only)

Parameter	Minimum	Nominal	Maximum	Units	Notes
Enable Voltage (High)	70%Vcc		-	Vdc	5
Disable Voltage (Low)	-	-	30%Vcc	Vdc	5

LVCMOS Output Characteristics

Parameter	Minimum	Nominal	Maximum	Units	Notes
Load	-	15	-	pF	
Voltage (High) (Voh)	90%Vcc	-	-	Vdc	
(Low) (Vol)	-	-	10%Vcc	Vdc	
Duty Cycle at 50% of Vcc	45	50	55	%	
Rise / Fall Time 10% to 90%	-	4	8	ns	

Package Characteristics

Package	Hermetically sealed crystal mounted on a ceramic package
Moisture Sensitivity Level	MSL-1

Environmental Characteristics

Vibration:	Vibration per Mil Std 883E Method 2007.3 Test Condition A
Shock:	Mechanical Shock per Mil Std 883E Method 2002.4 Test Condition B.
Soldering Process;	RoHS compliant lead free. See soldering profile on page 2.

** Not all options available at Digi-Key

Ordering Information

TL602-020.0M, TL602-024.576M, TVL602-020.0M, TVL602-024.576M

RoHS COMPLIANT

Notes:

1. *Frequency referenced to Fo. @ 25°C. Specification at time of shipment after 48 hours operation*
2. *Frequency stability vs. change in temperature. [±(Fmax - Fmin)/2.Fo].*
3. *Frequency change after reciprocal temperature ramped over the operating range. Frequency measured before and after at 25°C.*
4. *Bandwidth = 12KHz to Fo/2 MHz.*
5. *Output is enabled with no connection on pad 8 (for TL602 only).*

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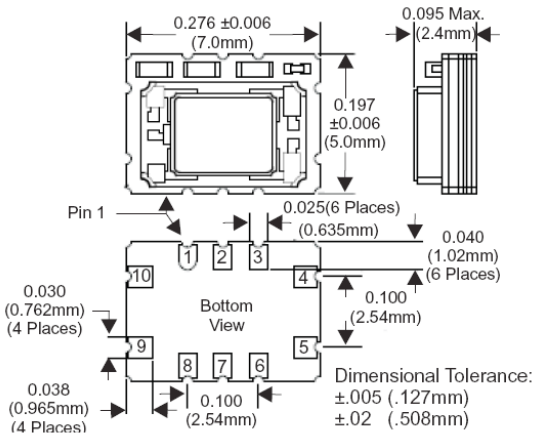
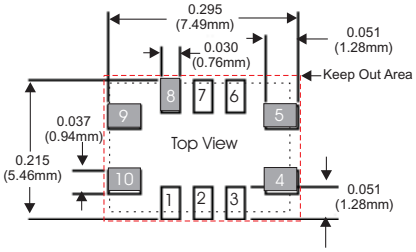
TL602 Package Layout



TL602 Suggested Pad Layout

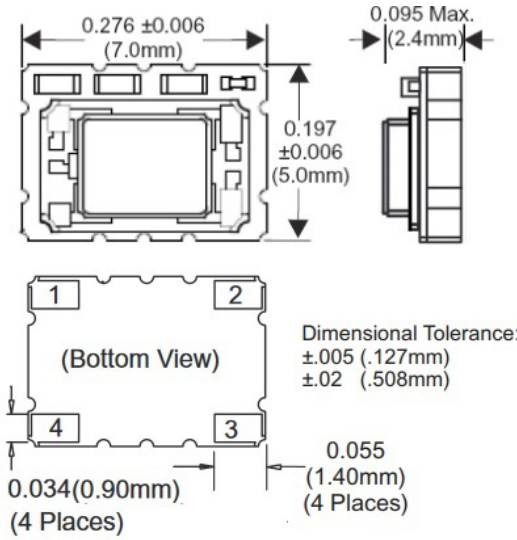


* Do not route any traces in the keep out area. It is recommended the next layer under the keep out area is to be ground plane.

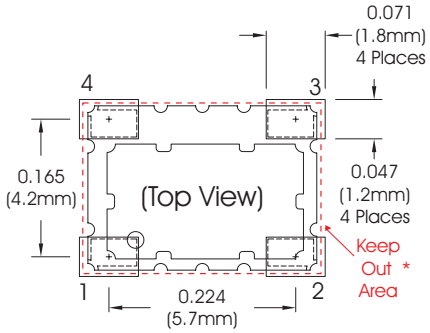
TL602 Pad Connections

Pad	Connection
1:	Do Not Connect
2:	Do Not Connect
3:	Do Not Connect
4:	Ground
5:	Output
6:	Do Not Connect
7:	Do Not Connect
8:	Tri-State Enable / Disable
9:	Supply Voltage Vcc
10:	N/C

TVL602 Package Layout



TVL602 Suggested Pad Layout

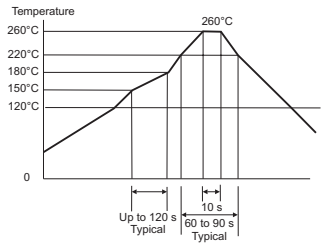


* Do not route any traces in the keep out area. It is recommended the next layer under the keep out area is to be ground plane.

TVL602 Pad Connections

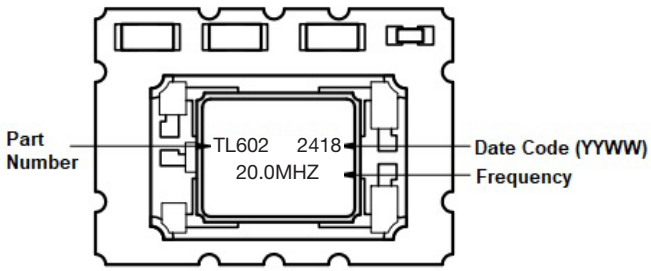
Pad	Connection
1:	N/C
2:	Ground
3:	Output
4:	Supply Voltage Vcc

Solder Profile

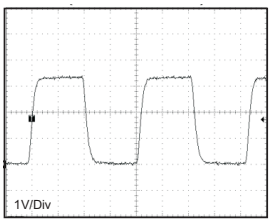


Meets IPC/JEDEC J-STD-020C

Marking Information



Output Waveform



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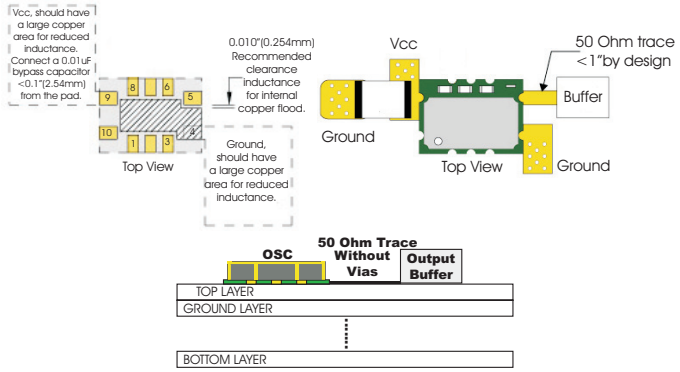
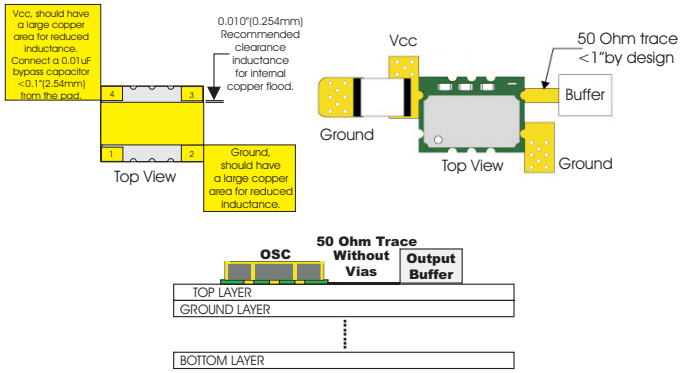
TL602 Design Recommendations

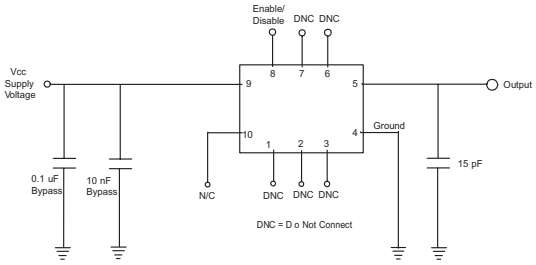


TVL602 Design Recommendations

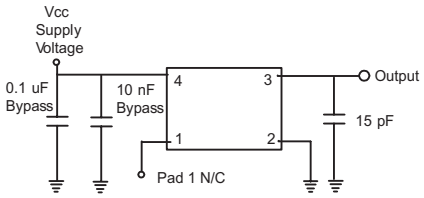


Attention: To achieve optimal frequency stability, and in some cases to meet the specification stated on this data sheet, it is required that the circuit connected to this TCXO output must have the equivalent input capacitance that is specified by the nominal load capacitance. Deviations from the nominal load capacitance will have a graduated effect on the stability of approximately 20 ppb per pF load difference.

TL602 Test Circuit

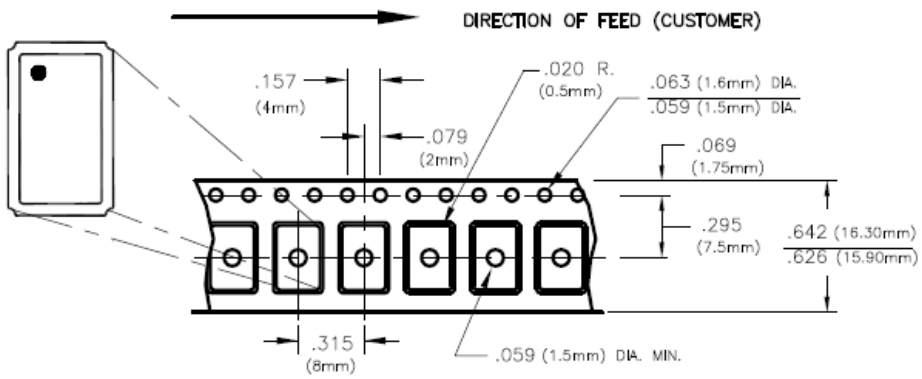


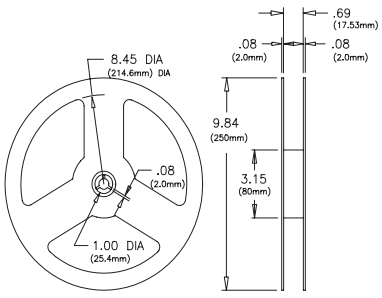
TVL602 Test Circuit



Tape and Reel Dimensions

MEETS EIA-481A AND EIAJ-1009B
700 PCS/REEL MAXIMUM.





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